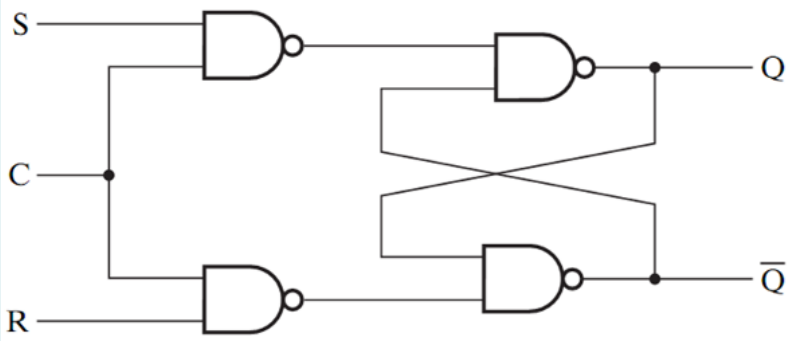
| | |
|---|---|
| **Started on** | Monday, 29 January 2024, 6:03 PM |
| **State** | Finished |
| **Completed on** | Monday, 29 January 2024, 6:31 PM |
| **Time taken** | 28 mins 11 secs |
| **Grade** | **12.00** out of 12.00 (**100**%) |

Question **1**

Correct

Mark 1.00 out of 1.00

In the following circuit, the present state is 0, and S=R=0. When the clock is its positive level, then Q̄ (Q') has the value of:




a. 0

b. Cannot determine from the given information

c. X

d. Z

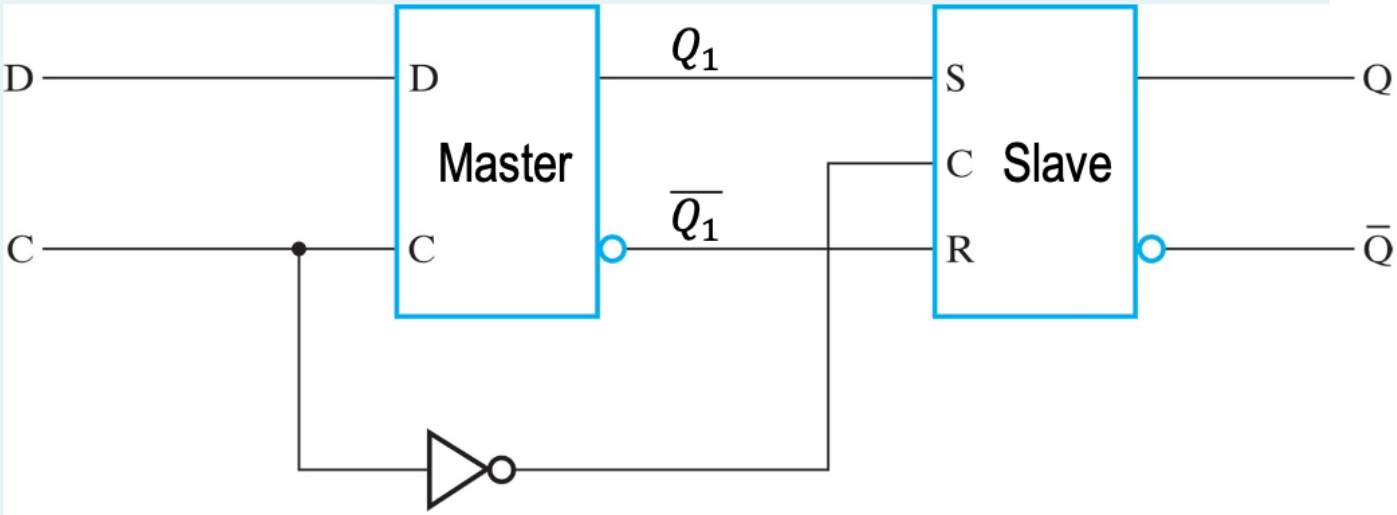
e. 1 ✔

Question **2**

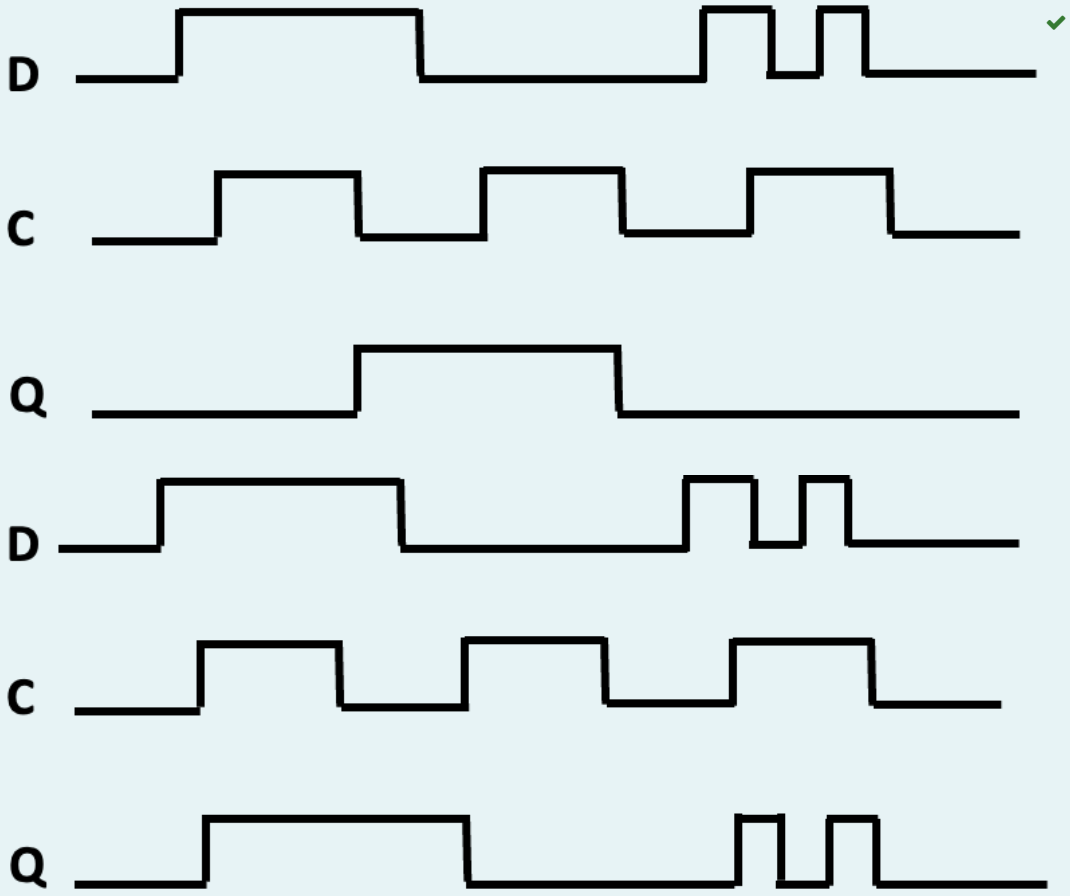
Correct

Mark 1.00 out of 1.00

What is the correct output waveform of the below circuit:

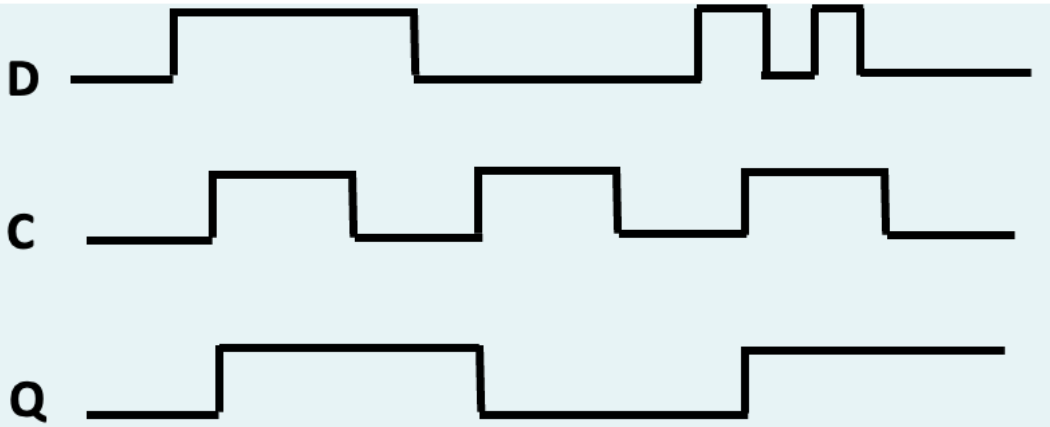



a. None

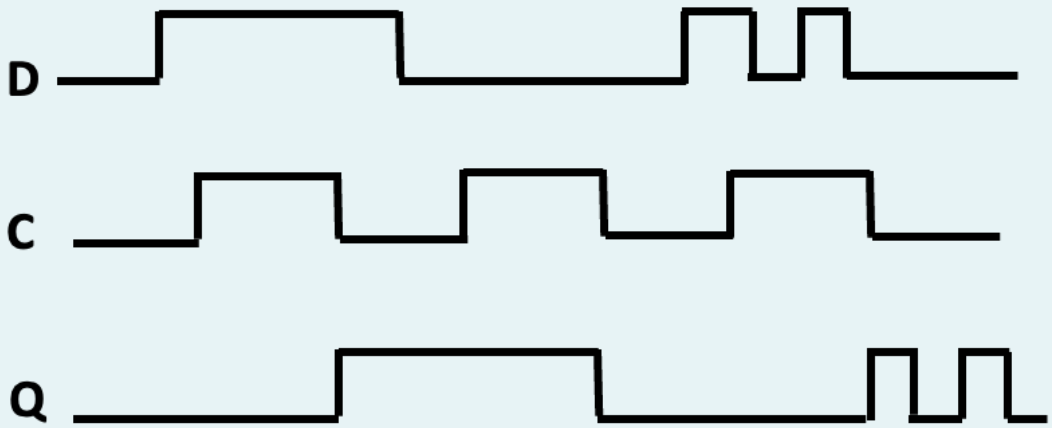
b. 


c. 

d.




e.




Question **3**

Correct

Mark 1.00 out of 1.00

A positive edge-triggered D flip-flop will store a 0 when _____

a. The D input is HIGH and the clock transitions from HIGH to LOW

b. The D input is HIGH and the clock is LOW

c. The D input is LOW and the clock is HIGH

d. The D input is LOW and the clock transitions from LOW to HIGH ✔

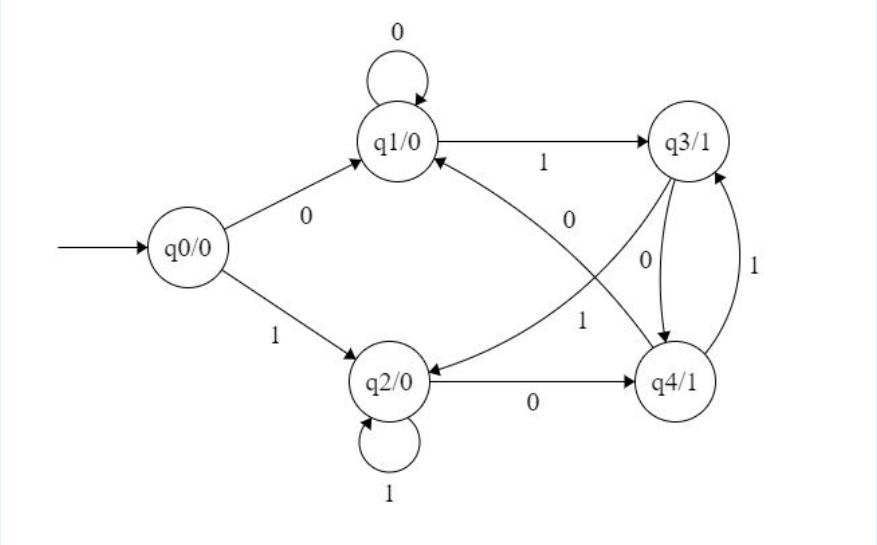
e. The D input is LOW and the clock transitions from HIGH to LOW

Question **4**

Correct

Mark 1.00 out of 1.00

The minimum number of Flip Flops required to implement the below machine is _____




a. 3 ✔

b. 4

c. 5

d. 2

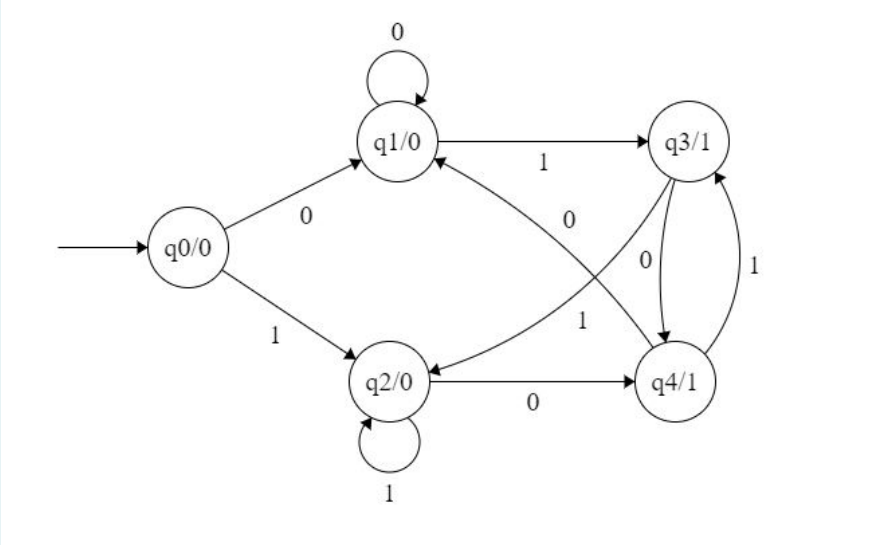
e. $2^5$

Question **5**

Correct

Mark 1.00 out of 1.00

What is true about the below schematic?




a. The machine can be implemented using a combinational logic circuit

b. The machine has no outputs

c. q1 is unreachable state

d. q2 and q3 are equivalent states

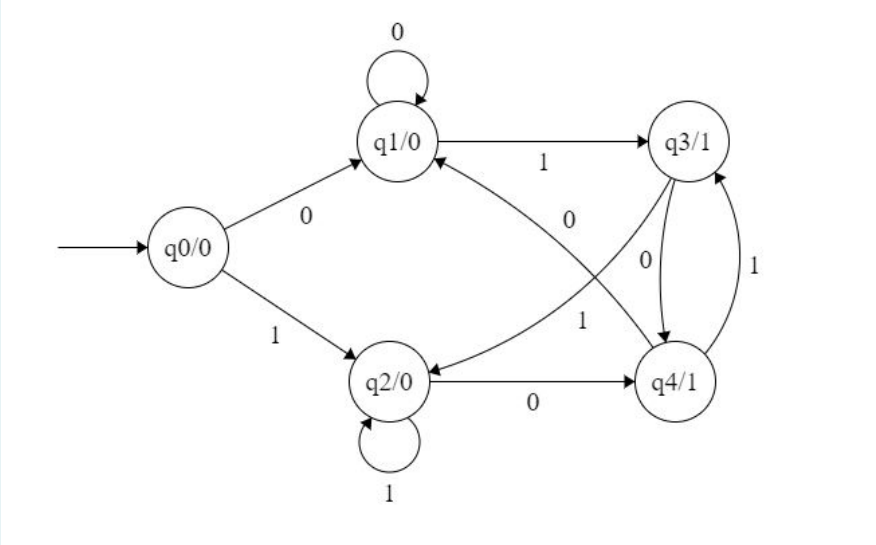
e. The machine has 1 input and 1 output ✔

Question **6**

Correct

Mark 1.00 out of 1.00

The below schematic represents




a. Q Flip Flop state machine

b. State table

c. Mealy state machine

d. None

e. Moore state machine ✔

Question **7**

Correct

Mark 1.00 out of 1.00

In synchronous sequential circuit, changes in the memory elements can happen at any instance of time.

a. True

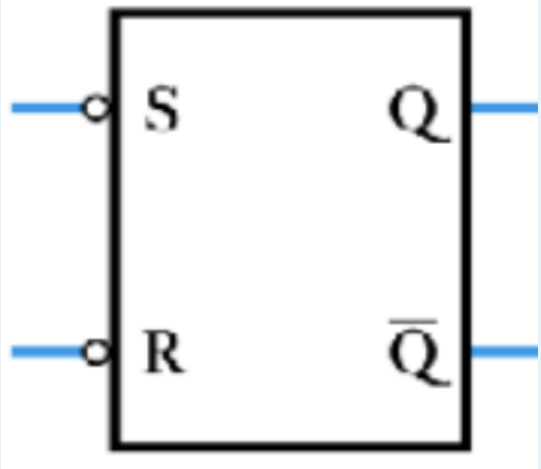
b. False ✔

Question **8**

Correct

Mark 1.00 out of 1.00

The below schematic represents:




a. Active low SR Flip Flop

b. Active high Flip Flop

c. Active low SR latch ✔

d. Master-Slave latch configuration

e. Active high SR latch

Question **9**

Correct

Mark 1.00 out of 1.00

Given the following state table, the following states are equivalent

| | Next State | | Output | |
|---|---|---|---|---|
| **Present State** | **Input = 0** | **Input = 1** | **Input = 0** | **Input = 1** |
| A | B | B | 1 | 1 |
| B | A | A | 1 | 0 |
| C | A | B | 0 | 1 |
| D | B | B | 1 | 1 |
| E | A | A | 0 | 1 |

- a. A and D ✔
- b. A and D, B and E
- c. A, D, and E
- d. B and E
- e. None

Question **10**

Correct

Mark 1.00 out of 1.00

If a sequential circuit is designed using three T flip flops. Assume the current state is abc = 001. To transition to the next state 110, then the values of Ta Tb Tc is:

- a. 001
- b. 110
- c. 000
- d. 111 ✔
- e. 110

Question **11**

Correct

Mark 1.00 out of 1.00

Choose the most correct answer. To design a synchronous sequential circuit that counts even numbers from 0 to 10. When it reaches the value of 10, it restarts counting from zero, then it has

a. None

b. 10 states

c. 6 states

d. 6 used states, 10 unused states ✔

e. 16 states

Question **12**

Correct

Mark 1.00 out of 1.00

How is a J-K flip-flop made to toggle?

a. Connect J input to XOR gate such that $J = K' \oplus Q$

b. Connect J and K inputs to 1 ✔

c. Connect J input to XOR gate such that $J = K \oplus Q'$

d. Connect K input to XOR gate such that $K = J \oplus Q$

e. Connect J and K inputs to 0