Experiment #8

Pre Lab

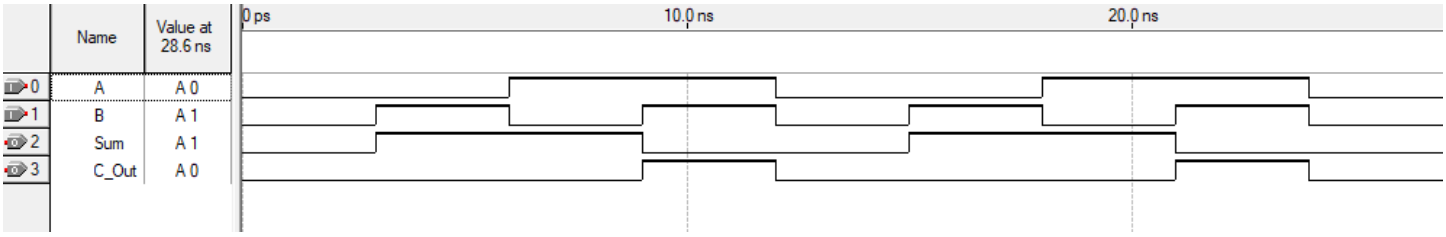
Name : Mohammed Jamil Saada Number : 1221972

A) Build half adder on data flow.

Code :

```
1  module Half_Adder(input A,B, output Sum, C_Out);
2
3  //Mohammed Jamil Saada - 1221972
4  //Half Adder on Data Flow
5
6  assign Sum = A^B;
7  assign C_Out = A&B;
8
9  endmodule
```

Wave form :

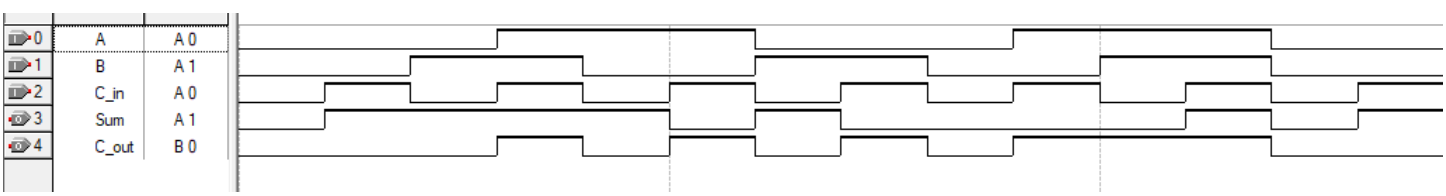


B) Build full adder using half adder structural.

Code :

```
1  module Full_Adder(input A, B, C_in, output Sum, C_out);
2
3  //Mohammed Jamil Saada - 1221972
4  //Full Adder using Half Adder Structural
5
6  wire w1, w2, w3;
7  Half_Adder(A,B,w1,w2);
8  Half_Adder(C_in,w1,Sum,w3);
9  or gate(C_out,w2,w3);
10
11 endmodule
```

Wave form :

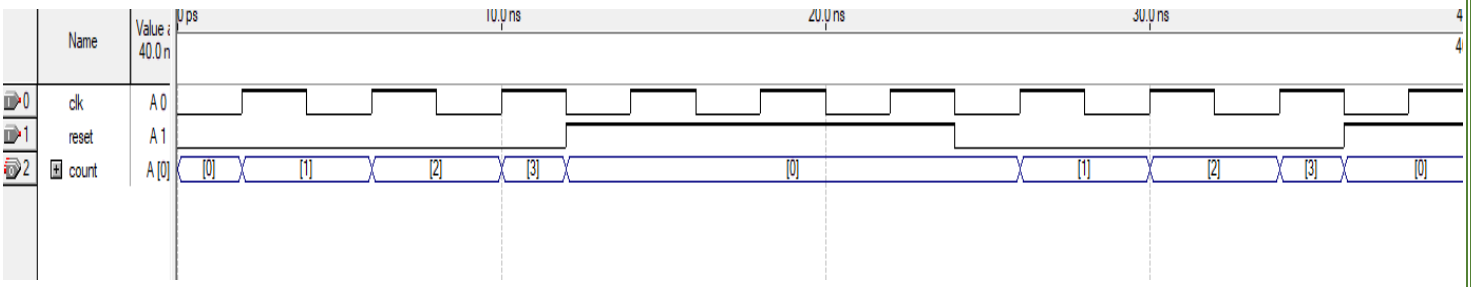


C) Build a 2-bit counter on behavioral.

Code :

```
1  module TowBit_Counter(output reg[1:0]count, input clk, reset);
2
3   //Mohammed Jamil Saada - 1221972
4   // 2-bit counter on behavioral
5
6  always @(posedge clk, posedge reset) begin
7  if(reset)
8  count = 2'b00;
9  else
10 count = count+1;
11 end
12
13 endmodule
```

Wave form :

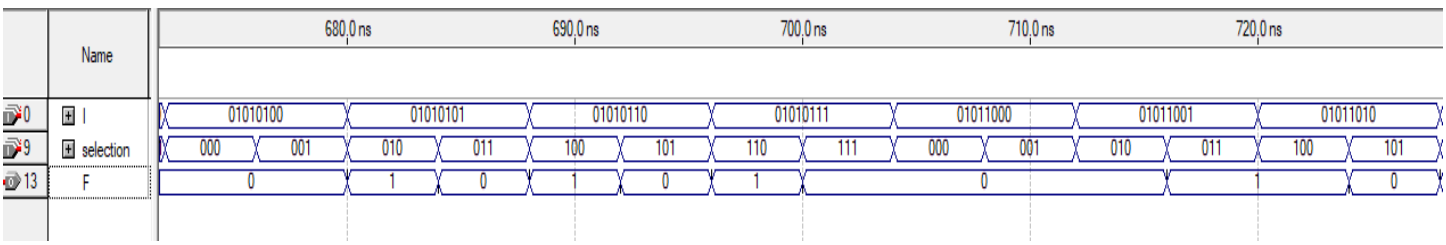


D) Build an 8x1 Multiplexer on behavioral.

Code :

```
1  module Mux_8to1(output reg F, input [7:0] I, input [2:0] selection);
2
3   //Mohammed Jamil Saada - 1221972
4   // 8x1 Multiplexer on behavioral
5
6  always @(*) begin
7  case(selection)
8   3'b000 : F = I[0];
9   3'b001 : F = I[1];
10  3'b010 : F = I[2];
11  3'b011 : F = I[3];
12  3'b100 : F = I[4];
13  3'b101 : F = I[5];
14  3'b110 : F = I[6];
15  3'b111 : F = I[7];
16  endcase
17  end
18  endmodule
```

Wave form :

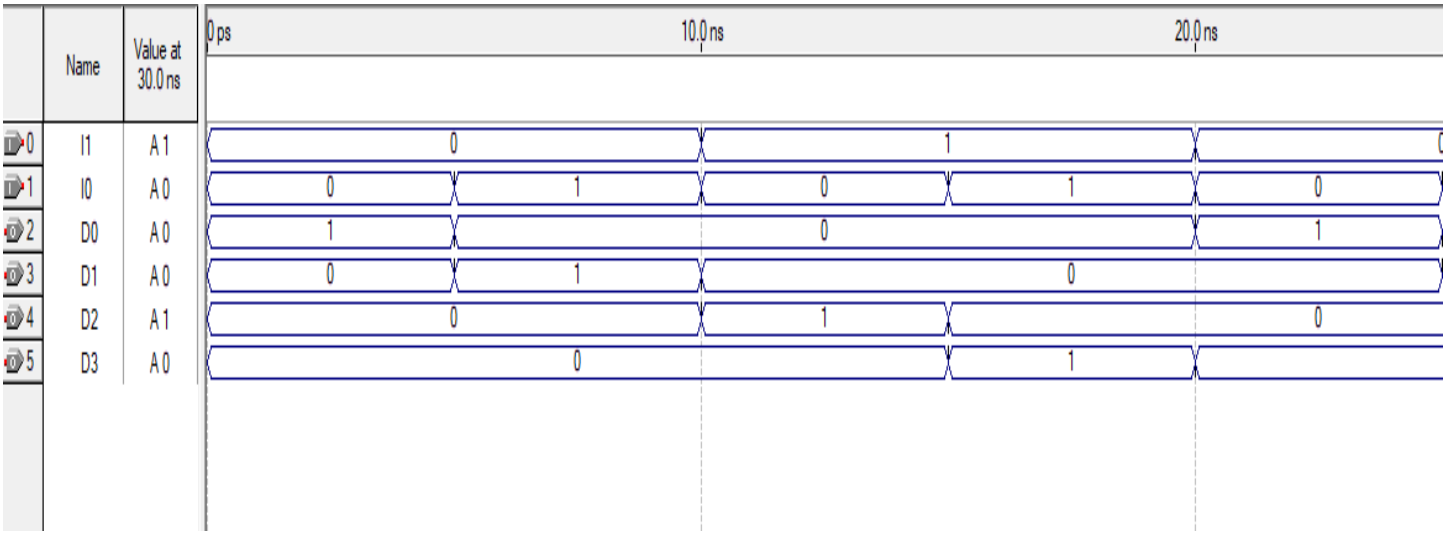


E) Build a 2x4 Decoder using basic gates (structural).

Code :

```
1  module Decoder_2to4(output D0, D1, D2, D3, input I0, I1);
2
3  //Mohammed Jamil Saada - 1221972
4  //2x4 Decoder using basic gates (stuctural)
5
6  wire i0, i1;
7  not gate1(i0,I0);
8  not gate2(i1,I1);
9  //i0 = I0' ,, i1 = I1'
10 and gate3(D0,i0,i1);
11 and gate4(D1,I0,i1);
12 and gate5(D2,i0,I1);
13 and gate6(D3,I0,I1);
14
15 endmodule
```

Wave form:



F) Show the wave form for above parts.

I have attached the wave form for each part above.