**Birzeit University**
**Faculty of Engineering and Technology**
**Department of Electrical and Computer Engineering**
**First Semester – 2023/2024**
**ENCS2340 - Digital Systems**
**Homework # 2**

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**Notes:**

1- Use this page as a cover for your homework.
2- Late homeworks will not be accepted (the system will not allow it).
3- Due date is Wednesday January 17, 2024at 11:59 pm on ritaj.
4- Organize your solution for each question (Q1, Q2, etc.) and add them to one file. Then, name you file as (Assign2_LastName_FirstName_StudetnsID.pdf).

Q1 **(10 points):** Design a combinational circuit with three inputs, x, y and z, and the three outputs, A, B, and C. when the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input.

Q2 **(5 points):** Implement the Boolean function **F(A,B,C) = AB + A'C + A'B'** Using a single 4x1 multiplexer.

Q3 **(5 points):** Implement the same function in **Q2** using the minimum number of 2x4 decoders with enable and a single NOR gate.

Q4 **(10 points):** Implement the following function F(A,B,C,D) = ∑(0, 2, 4, 6, 8, 10) using

a. Mux 4×1
b. Decoders 3-to-8
c. AND-OR
d. NAND-NAND

Q5 **(6 points):** In the following function determine the Essential prime implicant
F(A,B,C,D) = Σ (0,2,5,7,6,8.9,10,11,13,14,15)

Q6 **(4 points):** Explain the concept of odd parity generator?

Q1 **(10 points):** Design a combinational circuit with three inputs, x, y and z, and the three outputs, A, B, and C. when the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input.

## ① Specification :-

- number of input = 3 ( x, y, z)
- number of output = 3 ( A, B, C).
- input s are any number in binary from (0-7)
- output s for numbers (0-3) will increment one. and for numbers (4-7) will decrement one.
- Convert [0-3] to [1-4]
  Convert [4-7] to [3-6]

## ② truth table

| x | y | z | A | B | C |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |

## ③ K-map for output.

A

| x \ yz | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | | | 1 | |
| 1 | | 1 | 1 | 1 |

$A = xz + xy + yz$

↳ Can be written as $A = xy + z(x \oplus y)$

B

| x \ yz | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | | 1 | | 1 |
| 1 | 1 | | 1 | |

$B = xy'z' + x'y'z + xyz + x'yz'$

$= y'(xz' + x'z) + y(xz + x'z')'$

$= y'(x \oplus z) + y(x \oplus z)'$

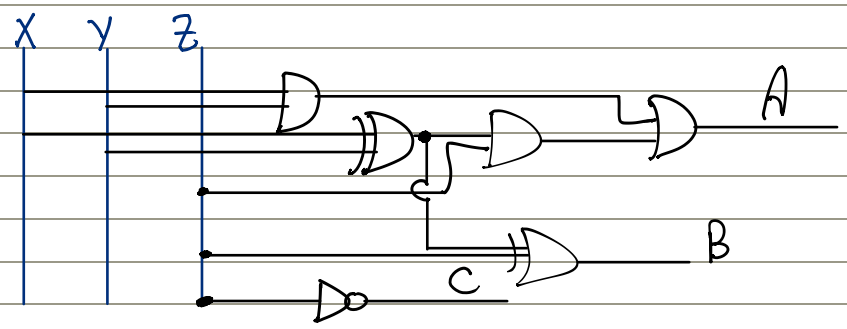
$= x \oplus z \oplus y$

C

| x \ yz | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | | | 1 |
| 1 | 1 | | | 1 |

$C = z'$

## ④ Technology Mapping :-




## ⑤ Verification

000 → 001 ✓

100 → 011 ✗

Q2 **(5 points):** Implement the Boolean function **F(A,B,C) = AB + A'C + A'B'**
Using a single 4x1 multiplexer.

① simplification :-

* input = 3 ( 4x1 Mux)
* out put = 1
* Selectors $(S_1, S_0) = (A, B)$

$$F(A,B,C) = AB(C+C') + A'(B+B').C + A'B'(C+C')$$

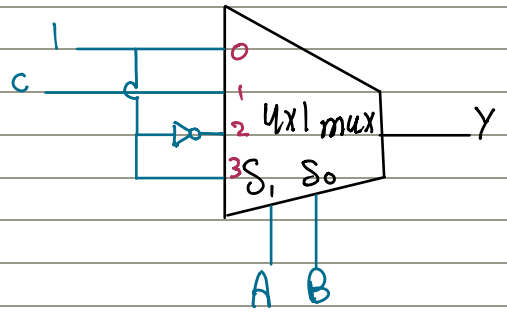
$$= ABC + ABC' + A'BC + A'BC + A'B'C + AB'C'$$

duplicated.

$$= m_7 + m_6 + m_3 + m_1 + m_0$$

$$F(A,B,C) = \Sigma(0,1,3,6,7)$$

| $S_1$ A | $S_0$ B | C | F | Comment |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | F = 1 |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 0 | F = C |
| 0 | 1 | 1 | 1 | |
| 1 | 0 | 0 | 0 | F = 0 |
| 1 | 0 | 1 | 0 | |
| 1 | 1 | 0 | 1 | F = 1 |
| 1 | 1 | 1 | 1 | |



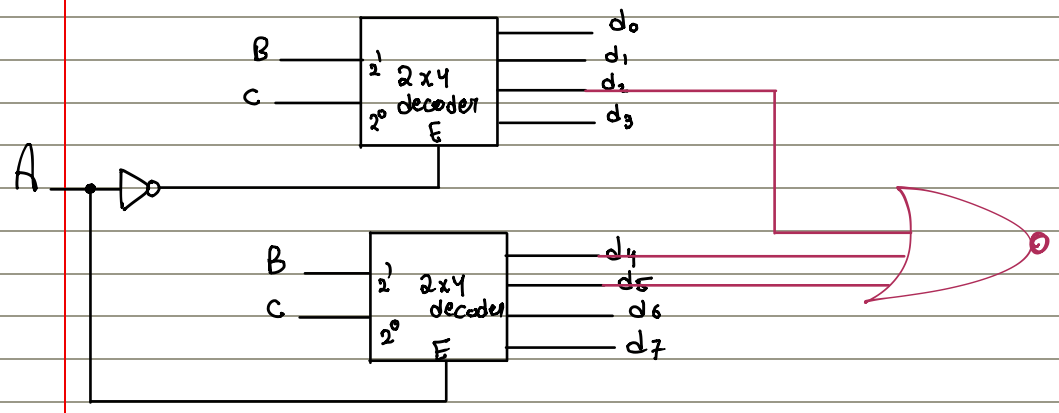
Q3 **(5 points):** Implement the same function in **Q2** using the minimum number of 2x4 decoders with enable and a single NOR gate.

$F(A,B,C) = AB + A'C + A'B'$

$= \Sigma(0,1,3,6,7) = \Pi(2,4,5)$

* input = 3
* output = $2^3 = 8$
* Enable

| A | B | C | $d_0$ | $d_1$ | $d_2$ | $d_3$ | $d_4$ | $d_5$ | $d_6$ | $d_7$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |



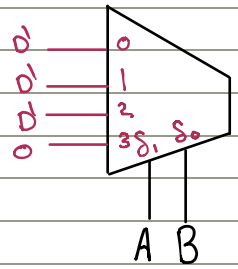
Q4 **(10 points):** Implement the following function F(A,B,C,D) = ∑(0, 2, 4, 6, 8, 10) using

a. Mux 4×1
b. Decoders 3-to-8
c. AND-OR
d. NAND-NAND

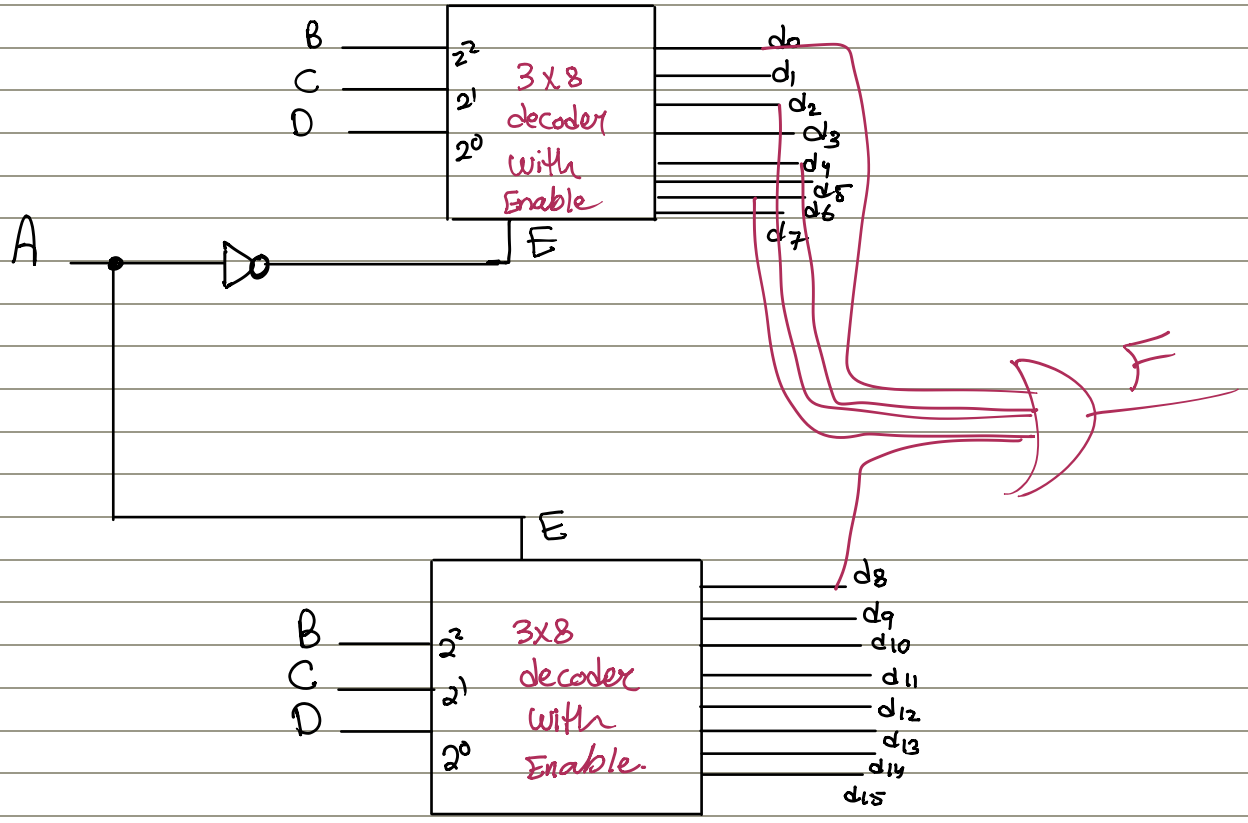
a)

| $S_1$ | $S_0$ | A | B | C | D | F | output |
|---|---|---|---|---|---|---|---|
| | | 0 | 0 | 0 | 0 | 1 | |
| | | 0 | 0 | 0 | 1 | 0 | $F=D'$ |
| | | 0 | 0 | 1 | 0 | 1 | |
| | | 0 | 0 | 1 | 1 | 0 | |
| | | 0 | 1 | 0 | 0 | 1 | |
| | | 0 | 1 | 0 | 1 | 0 | $F=D'$ |
| | | 0 | 1 | 1 | 0 | 1 | |
| | | 0 | 1 | 1 | 1 | 0 | |
| | | 1 | 0 | 0 | 0 | 1 | |
| | | 1 | 0 | 0 | 1 | 0 | $F=D'$ |
| | | 1 | 0 | 1 | 0 | 1 | |
| | | 1 | 0 | 1 | 1 | 0 | |
| | | 1 | 1 | 0 | 0 | 0 | |
| | | 1 | 1 | 0 | 1 | 0 | $F=0$ |
| | | 1 | 1 | 1 | 0 | 0 | |
| | | 1 | 1 | 1 | 1 | 0 | |

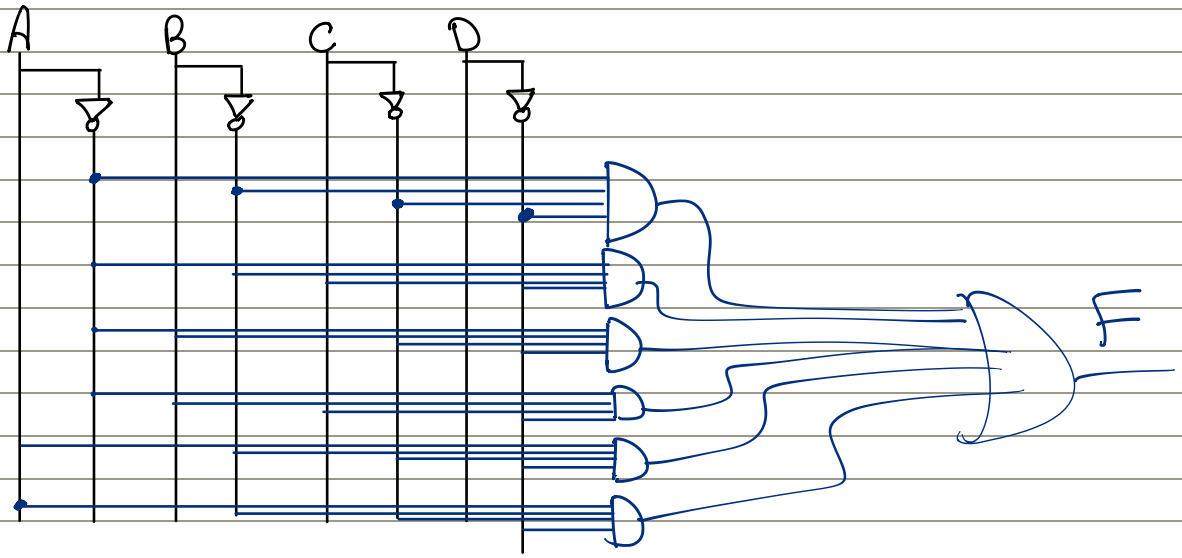
a) Mux 4x1 } selectors = 2
2 x 1



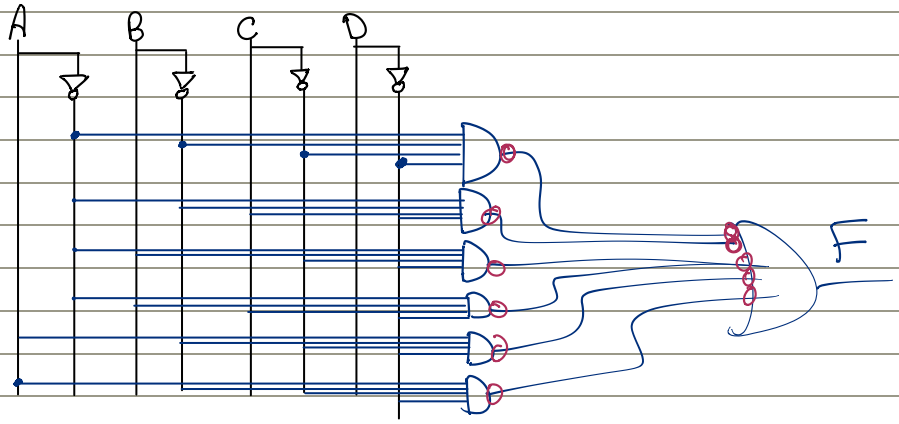

b) 3-8 decoder

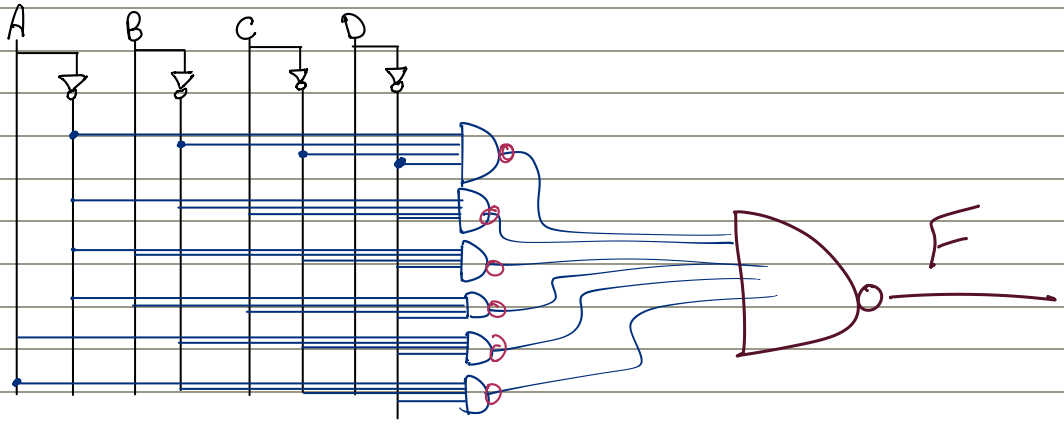


c) And - OR. $m_0 + m_2 + m_4 + m_6 + m_8 + m_{10}$

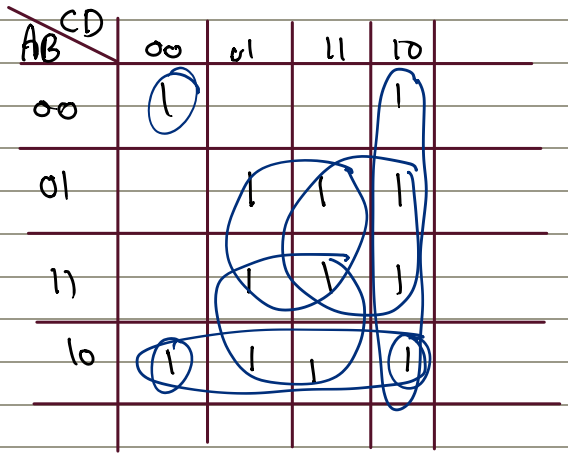



d) NAND - NAND gate



Q5 **(6 points):** In the following function determine the Essential prime implicant
F(A,B,C,D) = Σ (0,2,5,7,6,8.9,10,11,13,14,15)




EPI 8-

① $B'D'$
② $BD$

Q6 **(4 points):** Explain the concept of odd parity generator?