Experiment #8

Post Lab

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- **Verilog Codes :**

  - **Full Adder :**

FullDesign.bdf | Full_Adder.v

```
1  module Full_Adder(input A, B, C, output sum, c_out);
2
3  //Mohammed Jamil Saada - 1221972
4
5  assign sum = A^B^C;
6  assign c_out = (A&B)||(B&C)||(A&C);
7  endmodule
```

  - **Four Bit Adder**

FullDesign.bdf | Full_Adder.v | FourBit_Adder.v

```
1  module FourBit_Adder(input [3:0]A, input [3:0]B, input c_in, output [3:0]sum, output c_out);
2
3  //Mohammed Jamil Saada - 1221972
4
5  wire [2:0] c;
6  Full_Adder FA0(A[0],B[0],c_in,sum[0],c[0]);
7  Full_Adder FA1(A[1],B[1],c[0],sum[1],c[1]);
8  Full_Adder FA2(A[2],B[2],c[1],sum[2],c[2]);
9  Full_Adder FA3(A[3],B[3],c[2],sum[3],c_out);
10
11 endmodule
```

- **Four Bit AND :**

FullDesign.bdf | Full_Adder.v | FourBit_Adder.v

```
1  module FourBit_AND(input [3:0]A, input [3:0]B, output [3:0]Result);
2
3  //Mohammed Jamil Saada - 1221972
4
5  assign Result[0] = A[0] & B[0];
6  assign Result[1] = A[1] & B[1];
7  assign Result[2] = A[2] & B[2];
8  assign Result[3] = A[3] & B[3];
9
10 endmodule
```

- **Four Bit OR**

FullDesign.bdf | Full_Adder.v | FourBit_Adder.v | FourBit_AND.v

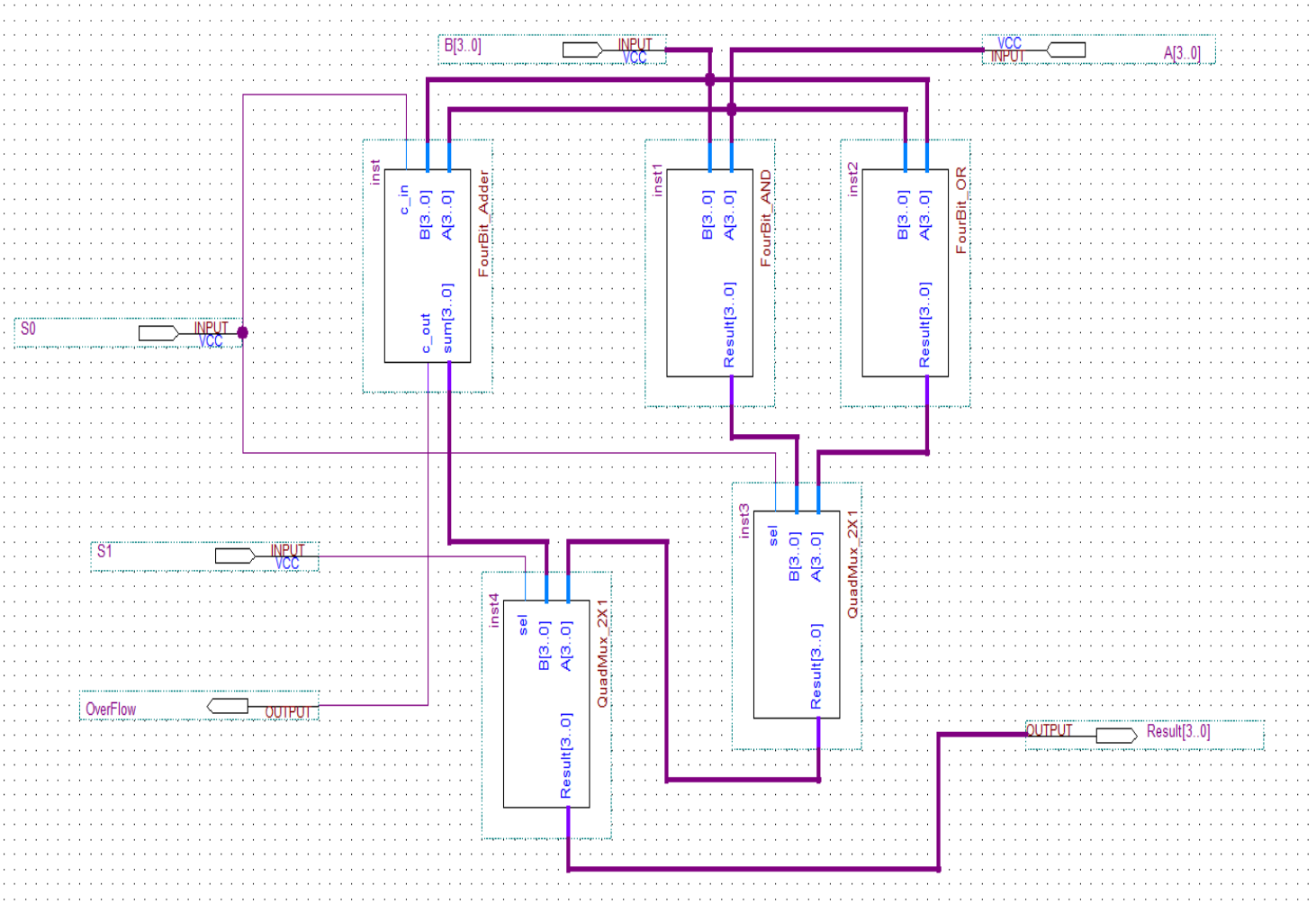
```
1  module FourBit_OR(input [3:0]A, input [3:0]B, output [3:0]Result);
2
3  //Mohammed Jamil Saada - 1221972
4
5  or gate1(Result[0],A[0],B[0]);
6  or gate2(Result[1],A[1],B[1]);
7  or gate3(Result[2],A[2],B[2]);
8  or gate4(Result[3],A[3],B[3]);
9
10 endmodule
```

- **(4-bit input) Multiplexer 2X1**

FullDesign.bdf | Full_Adder.v | FourBit_Adder.v | FourBit_AND.v | FourBit_OR.v

```
1  module QuadMux_2X1(input [3:0]A, input [3:0]B, input sel, output [3:0]Result);
2
3  //Mohammed Jamil Saada - 1221972
4
5  assign Result = (sel==0) ? A : B;
6
7  endmodule
```

- **Full Design :**



- **Wave Form for Full Design :**