Experiment #9

Pre Lab

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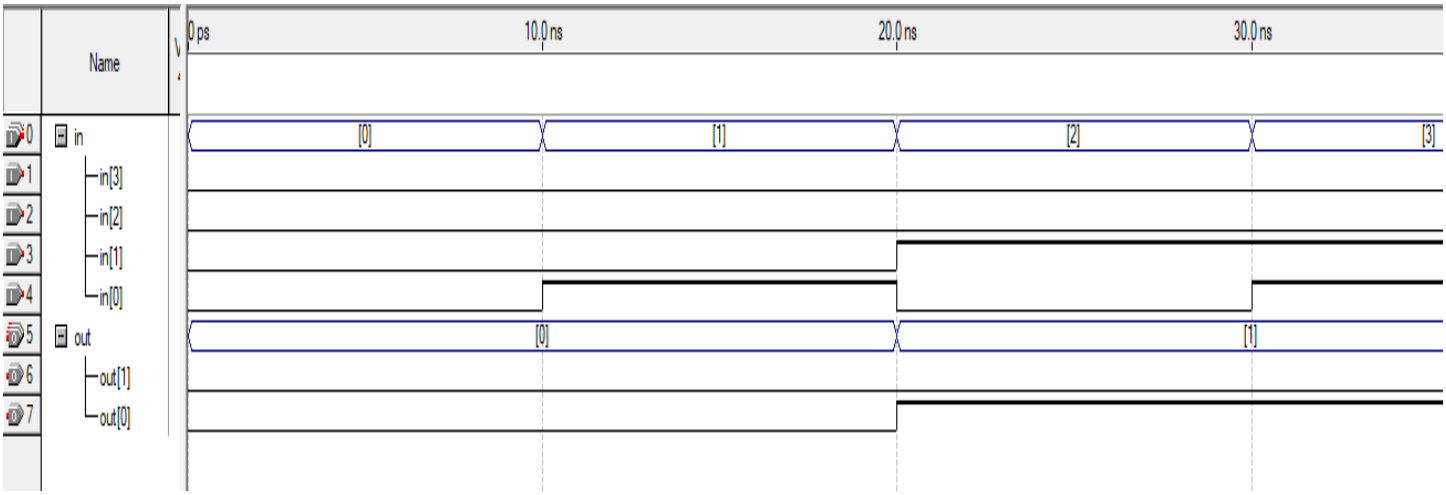
1) Design 4x2 priority encoder

Code :

priority_Encoder.v | Compilation Report - Flow Summary | priority_Encoder_Wave.vwf | Simulator Tool

```
1  //Design 4X2 priority encoder
2  module priority_Encoder(output reg [1:0] out, input [3:0] in);
3
4  //Mohammed Jamil Saada - 1221972
5
6  always @ (in)
7  if(in[3]==1) out[1:0] = 2'b11;
8  else if(in[2]==1) out[1:0] = 2'b10;
9  else if(in[1]==1) out[1:0] = 2'b01;
10 else if(in[0]==1) out[1:0] = 2'b00;
11 else out[1:0] = 2'b00;
12 endmodule
```

Wave form :



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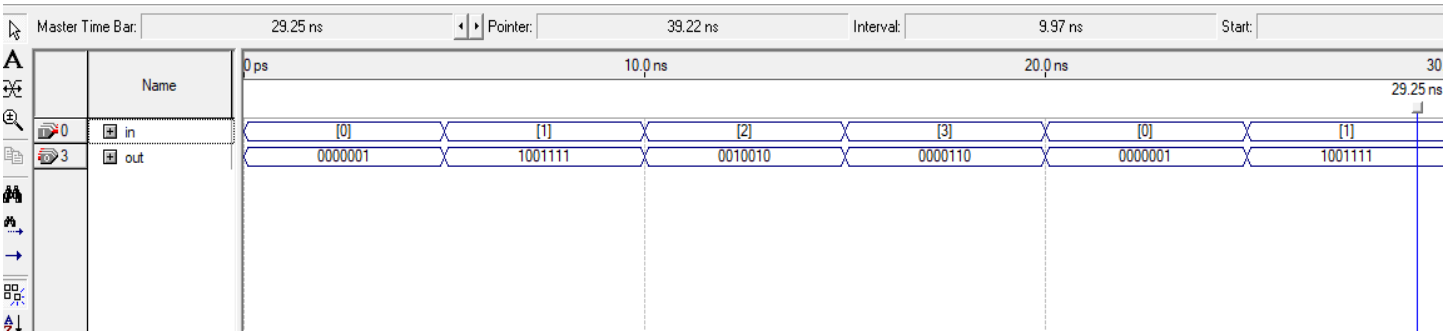
2) Design the 7-segment display

Code :

seven_segment_display_driver.v

```
1  //Design the 7-segment display driver
2  module seven_segment_display_driver(output reg [6:0]out, input [1:0] in);
3
4  //Mohammed Jamil Saada - 1221972
5
6  always @(in)
7      begin
8          case(in)
9              0 : out = 7'b0000001;
10             1 : out = 7'b1001111;
11             2 : out = 7'b0010010;
12             3 : out = 7'b0000110;
13         endcase
14     end
15 endmodule
```

Wave form :

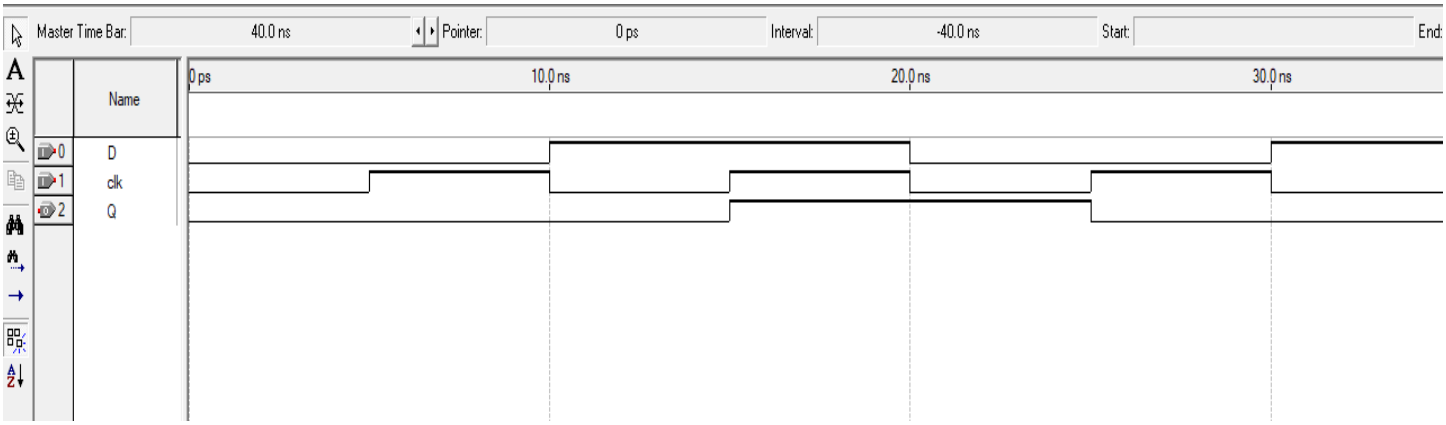


3) write and simulate the Verilog code of a D-Flip Flop

Code :

```
1  //D-Flip Flop
2  module D_Flip_Flop(output reg Q, input D,clk);
3
4  //Mohammed Jamil Saada - 1221972
5
6  always @ (posedge  clk)
7      Q <= D;
8  endmodule
```

Wave form :



4) Write and simulate the Verilog code of 2x1 MUX.

Code :

```
1   //2x1 MUX
2   module MUX_2x1(output reg m, input A, B, Sel);
3
4   //Mohammed Jamil Saada - 1221972
5
6   always @ (*)
7       if(Sel==0)
8           m = B;
9       else
10          m = A;
11  endmodule
```

Wave form :