# Experiment NO.4

## Digital Circuits Implementation using Breadboard

## Post Lab

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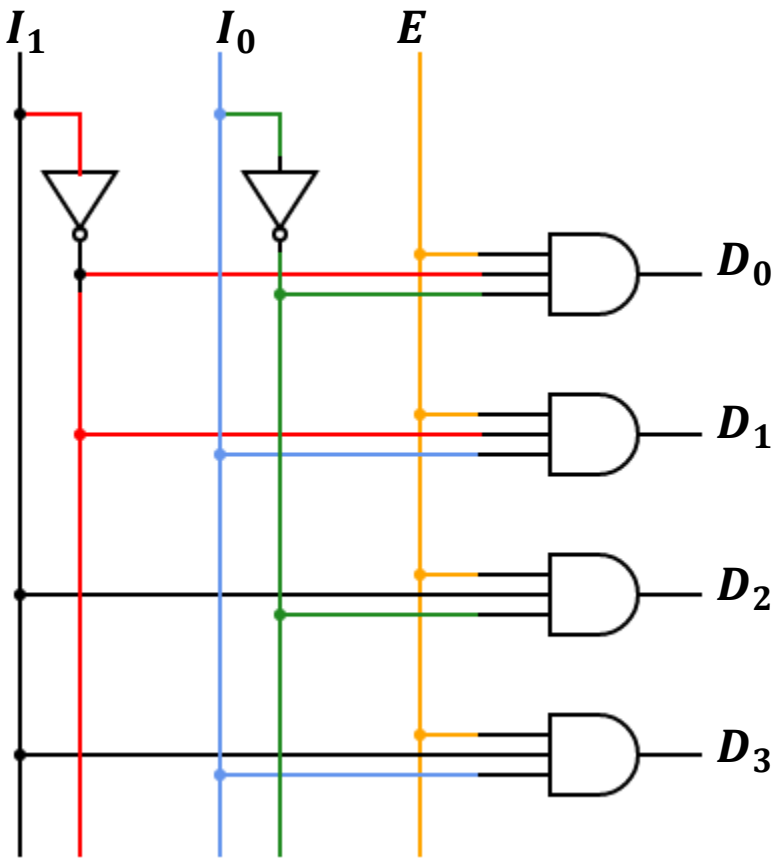
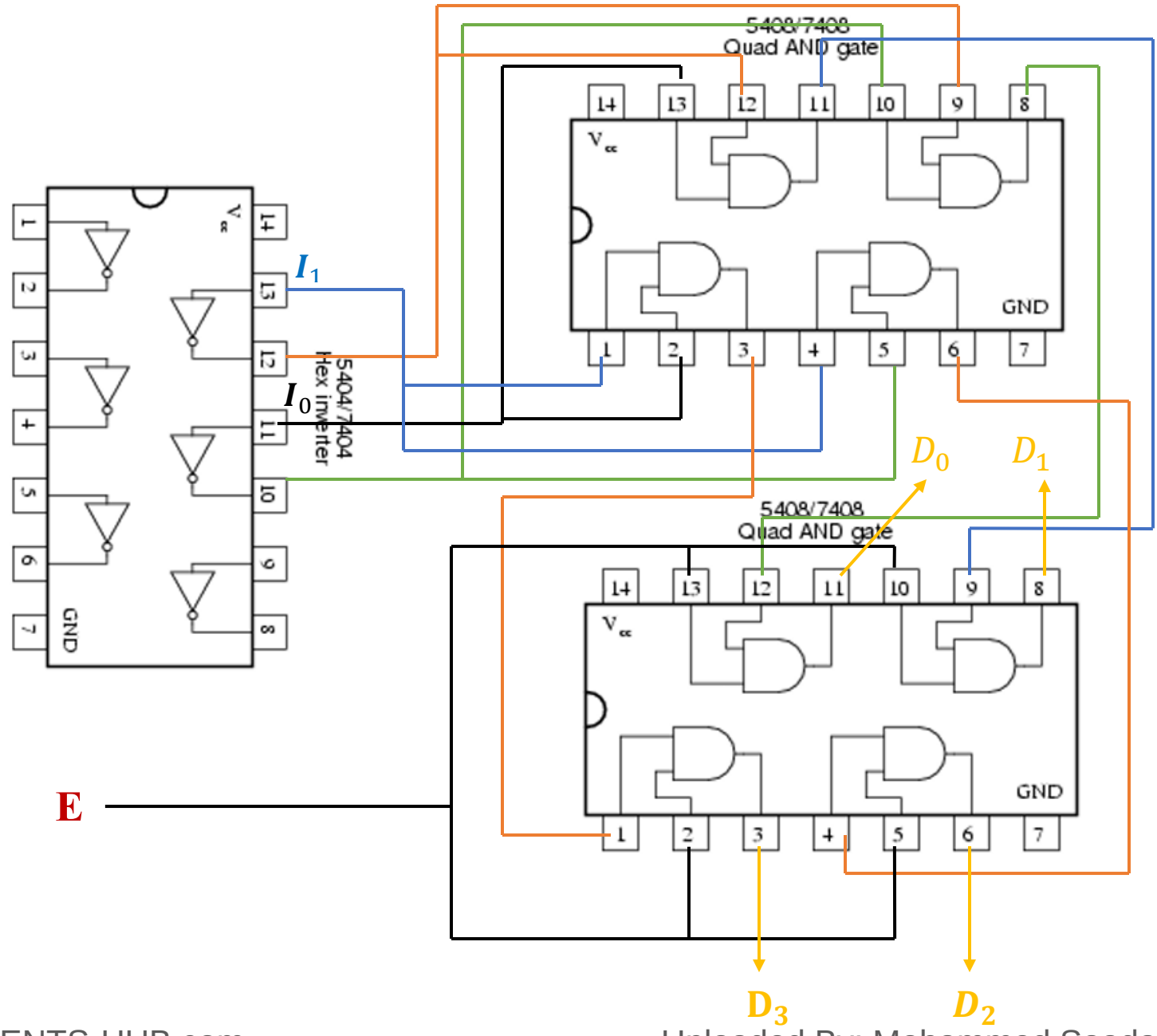
1) How do you go about adding an Enable (E) signal to the decoder in Figure 4.7? Modify the implementation to show that. (Design Only using chips in Figure 1).

To add an Enable to 2x4 decoder we will add a third input E to each AND gate as follow :

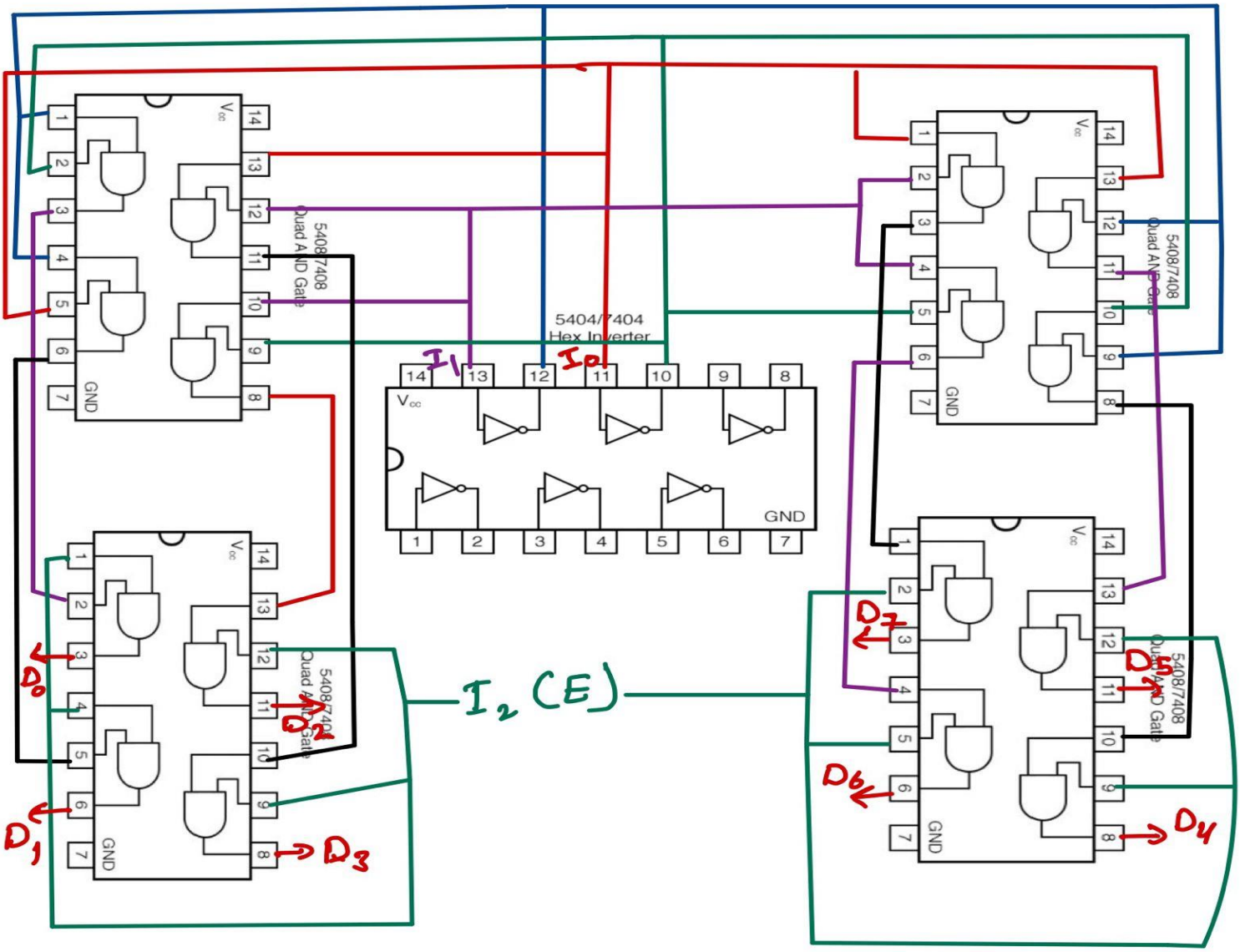


The truth table for this circuit as :

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| $I_1$ | $I_0$ | E | $D_0$ | $D_1$ | $D_2$ | $D_3$ |
| X | X | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |



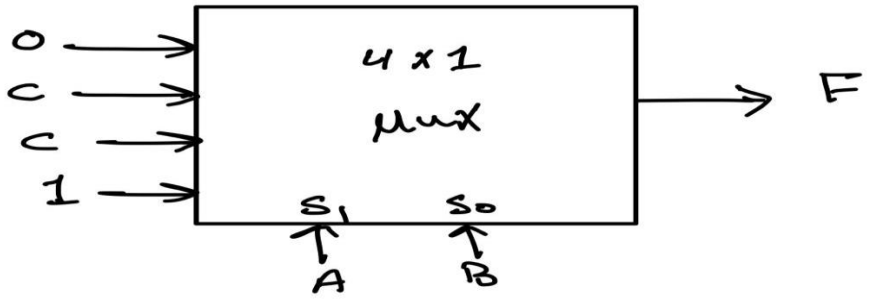
2) How to use that to implement a 3x8 decoder using chips in Figure 1.

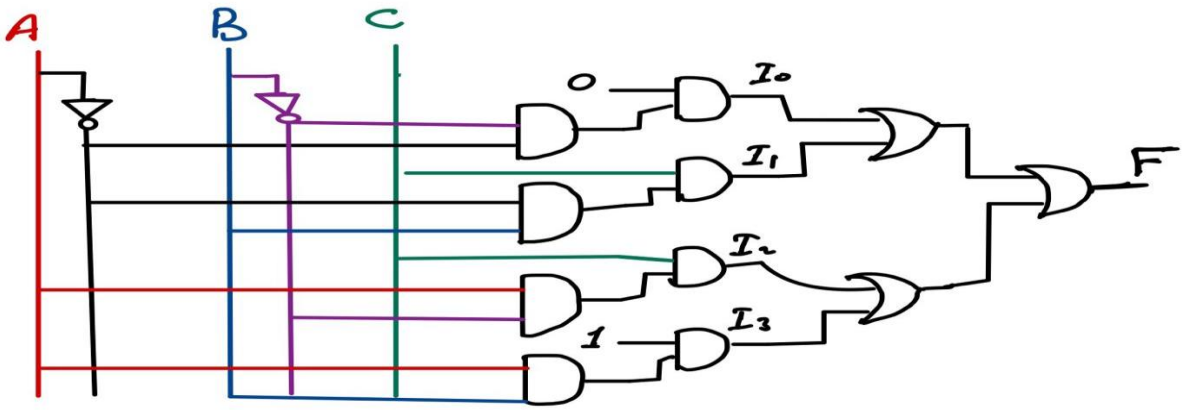


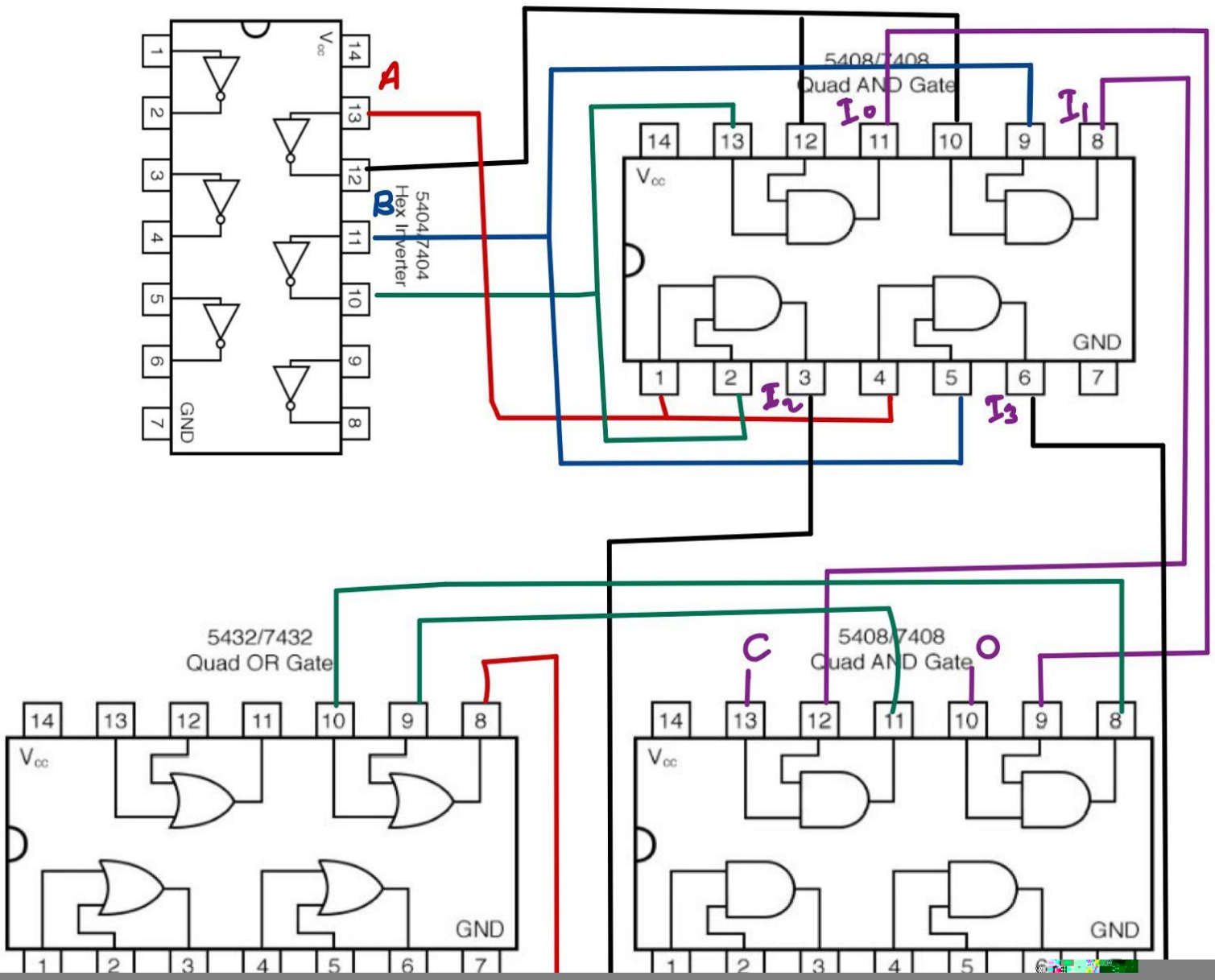

We make $I_2$ the enable of both decoders, and use $I_1$ *and* $I_0$ as the inputs of the decoders.

3) Use the just constructed 4x1 multiplexer to design a three inputs network that gives 1 if the majority of its inputs are 1 and outputs a zero otherwise (Design Only using chips in Figure 1).

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| A | B | C | F | F |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 0 | C |
| 0 | 1 | 1 | 1 | |
| 1 | 0 | 0 | 0 | C |
| 1 | 0 | 1 | 1 | |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | |



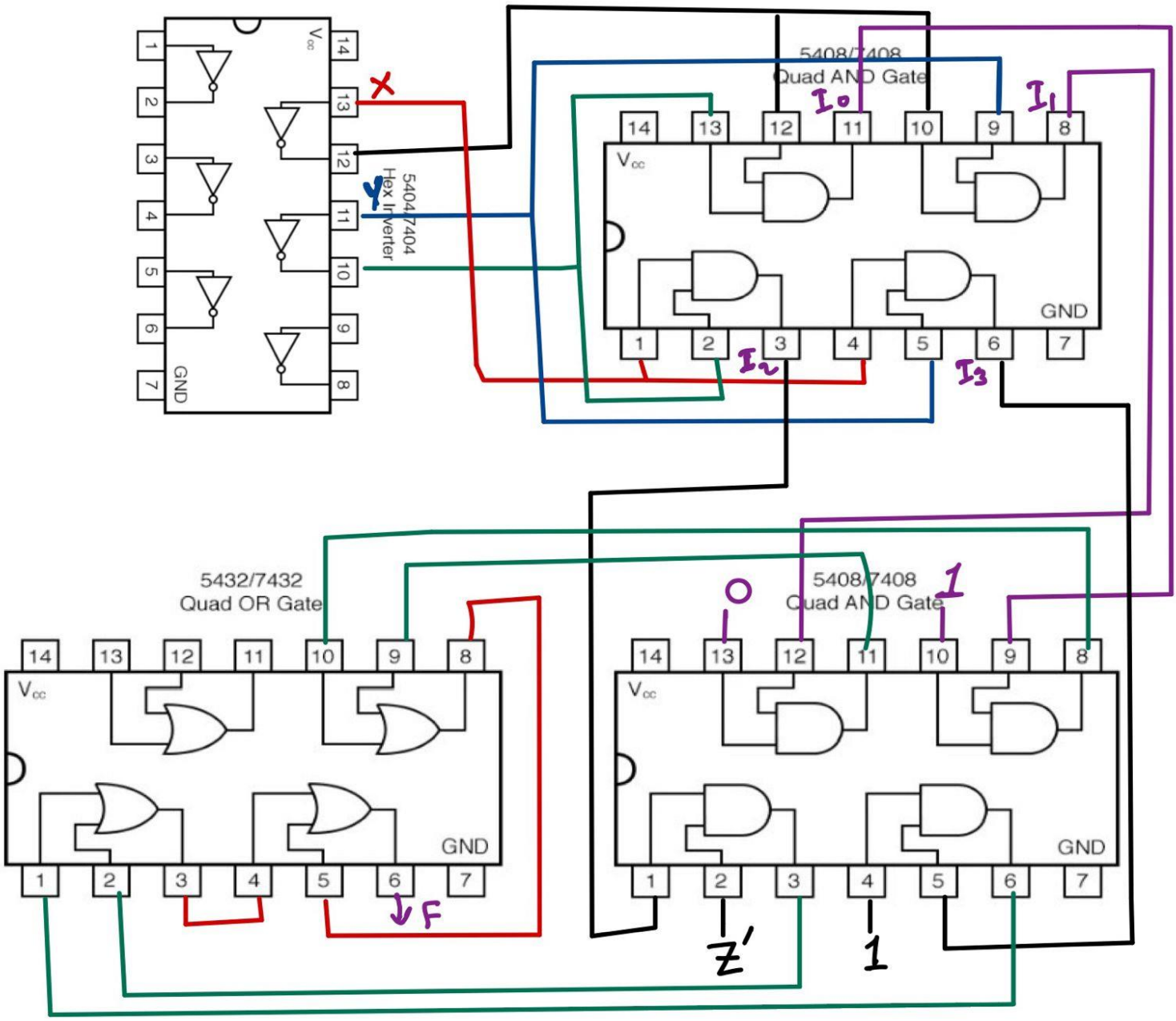





4) Implement f(x, y, z) = m(0, 1, 4, 6, 7), using 4x1 MUX using chips in Figure 1.

$f(x,y,z) = m(0,1,4,6,7)$

| Inputs | | | Outputs | |
|---|---|---|---|---|
| x | y | z | F | F |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | |
| 1 | 0 | 0 | 1 | z' |
| 1 | 0 | 1 | 0 | |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | |


5404/7404
Hex Inverter
X
Y
5408/7408
Quad AND Gate
$I_0$
$I_1$
$I_2$
$I_3$
5432/7432
Quad OR Gate
F
5408/7408
Quad AND Gate
0
1
Z'
1
GND
$V_{cc}$