# Digital Systems Section 2

Chapter (3)

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- Θ A Boolean **Function** is **uniquely** represented by a **truth table**
- Θ Boolean **Function** can be implemented (**NOT Uniquely**) by a Boolean **Equation** and the corresponding **logic diagram**
- Θ Simplest Functions use the **smallest** number of the **smallest** gates and therefore give the *most economical* and *efficient* circuit implementations Requires: Minimization
- Θ Boolean **Function** can be **simplified** by algebraic methods learned earlier
	- This process is **not** always **straight-forward** and may **not** result in the **simplest** form of an expression
- Θ A **formal** approach for simplification is needed (**systematic** procedure) **The Map Method**



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- Θ A **Straight-forward/Simpler** method to achieve minimization **systemically Graphical** representation of a Truth Table **K-Map**
- Θ A K-map is a **diagram** made up of **squares** representing **minterms**
	- $\bullet$  K-map for **n** variables is a collection of  $2^n$  squares/cells  $\lceil n \text{ variables } \rightarrow 2^n \text{ minterms} \rceil$
	- Each **Square/Cell** → **Minterm**
	- **Squares** arranged such that physically **adjacent cells** differ in the value of **only one literal**
- Θ Different **patterns** in this diagram can be detected to simplify expressions
	- Θ **Adjacent** minterms can be **combined** to form simpler terms
- Θ The **simplified** expression will always be in sum-of-products or product-of-sums form
- Θ K-Map produces a circuit diagram with **minimum** number of **gates**
- Θ K-Map produces circuits with gates having **minimum**  number of **inputs**
- Θ The simplest expression is **not unique**  two or more optimal expressions may exist









- Θ Boolean functions having **two** variables x and y
- Θ There are **2<sup>2</sup>** = **4** minterms for two variables  $xy, x'y, xy', x'y'$
- Θ A K-map for **two** variables will have **four squares** → Each cell will represent a minterm



Each **cell** represents the **minterm** of the corresponding **row** in the truth table

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- Θ Boolean functions having **three** variables x,y and z
- Θ There are **2<sup>3</sup>= 8** minterms for three variables

 $x'y'z', x'y'z, x'yz, x'yz', xy'z', xy'z, xyz, xyz'$ 

Θ A K-map for **three** variables will have **eight squares** → Each cell will represent a minterm



**Be Careful:** The order is **not** sequential  $m_3$  before  $m_2$  $m_7$  before  $m_6$ 

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Each **cell** represents the **minterm** of the corresponding **row** in the truth table

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- Θ Boolean functions having **Four** variables w,x,y and z
- Θ There are **2<sup>4</sup>= 16** minterms for Four variables
- Θ A K-map for **Four** variables will have **sixteen squares** → Each cell will represent a minterm

**Be Careful:** The order is **not** sequential  $m_3$  before  $m_2$  $m_7$  before  $m_6$  $m_{12} - m_{15}$  before  $m_{8} - m_{11}$ 

Each **cell** represents the **minterm**







- Θ **Construct** the corresponding map (based on number of variables)
- Θ **Enter** function **output (1's)** values on the map (from Truth Table or Canonical Form) to the corresponding cell/square

**Map** the following Function on a K-map

 $F_1(A, B, C) = A'B'C + A'BC' + ABC' + ABC$ 

1) Three variables  $\rightarrow$  2<sup>3</sup> = **8**-cell K-map

2) Place a **1** on the K-map in the cell having the **same** minterm index/value

 $A'B'C = 001$ ,  $A'BC' = 010$ ,  $ABC' = 110$ ,  $ABC = 111$ 

Primed  $\rightarrow 0$ Unprimed  $\rightarrow$  1

Canonical Form



**Be Careful:** The order is **not** sequential  $m_3$  before  $m_2$  $m<sub>7</sub>$  before  $m<sub>6</sub>$ 



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**Map** the following Function on a K-map

 $F_2(A, B, C, D) = A'BCD' + ABCD' + ABC'D' + ABCD$ Canonical Form

1) Four variables  $\rightarrow$  2<sup>4</sup> = **16**-cell K-map 2) Place a **1** on the K-map in the cell having the **same** minterm index/value



- Θ **Single** variable changes in **adjacent** cells
- Θ Cells that differ by only **one** variable are called **adjacent** cells
- Θ Example:
	- $\odot$  011 is adjacent to 010
	- 011 is **not** adjacent to 101
- Θ **Wrap-around** adjacency:
	- Cells in the left-most column are **adjacent** to the cells in the right-most column (100 & 110)

What is the **sum** of minterms in two adjacent squares?

$$
m_0 + m_4 = x'y'z' + xy'z'
$$
  

$$
= (x' + x)y'z' = y'z'
$$
  

$$
m_7 + m_6 = xyz + xyz'
$$
  

$$
= xy(z + z') = xy
$$
  

$$
m_0 + m_2 = x'y'z' + x'yz'
$$
  

$$
= x'z'(y' + y) = x'z'
$$



**Sum** of two minterms in **adjacent** squares can be simplified to a **single product**  term consisting of only **two literals**. The **dissimilar** variable will go away.

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- Θ Once a SOM expression has been **mapped** on the K-map, there are three steps in obtaining a simplified form
	- **1) Group** 1's
	- **2) Determine** the **product** term for each group
	- **3) Sum** the resulting terms
- Θ Group 1's with the following goal in mind: **Maximize** the **size** of the groups and **minimize** the **number** of groups
- Θ Group 1's according to the following rules:
	- $\checkmark$  Group size must be powers of 2 (1, 2, 4, 8, or 16,.. Cells)
	- ✓ Each **cell** in a group must be **adjacent** to one or more cells in that **same** group.
		- (**Not** all cells in a group have to be adjacent to each other)
	- ✓ Always include the **largest** possible number of **1's** in a group
	- ✓ Each **1** on the map must be included in at **least one** group
	- ✓ The **1's** already in a group can be included in another group as long as the **overlapping** groups include **non-common 1's**



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$$
F(x, y, z) = z + x'y
$$



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*K -Map Simplification* 

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#### No. of **literals** in an expression = Total No. of variables - log<sub>2</sub> (No. of cells in group)





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*K-Map Simplification* 

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# More Examples:  $F(W, X, Y, Z) = \sum_{m}(3,4,5,7,13,14,15)$



## $F(W, X, Y, Z) = ZX + \overline{W}YZ + WXY + \overline{W}XY$

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#### **More Examples:**



 $F = A'B + B'C$ 



 $F = y' + w'z' + xz'$ 

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- Θ In choosing **adjacent** squares in a map, we must **ensure** that:
	- **D** All minterms of the function are **covered** when we combine squares
	- ↇ The number of **terms** in the expression is **minimized**
	- ↇ **No redundant** terms
- Θ Sometimes there might be **two or more expressions** that **satisfy** the simplification criteria



- Θ The procedure for **combining** squares in the map may be made more **systematic** if we understand the meaning of the following terms.
	- *D* Implicant: is a product term of a function obtained by valid grouping of adjacent squares (minterms or 1's)
	- **D** Prime Implicant (PI): is a product term obtained by combining the maximum possible number of adjacent squares
		- ↇ **Examples:**
			- $\checkmark$  **1** that is not adjacent to any other 1's.
			- $\checkmark$  **Two** adjacent 1's that are not in a group of four adjacent 1's.
			- $\checkmark$  **Four** adjacent 1's that are not in a group of eight adjacent 1's
	- **Essential Prime Implicant (EPI):** If a **minterm** is **covered** by **only one** prime implicant,

that prime implicant is said to be **essential prime implicant**

The **simplified** expression is obtained from the **logical sum** of **all the essential prime implicants**, plus **other prime implicants that may be needed** to **cover** any remaining minterms **not covered** by the essential prime implicants.

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#### **Example:**



The Minterm is **only** covered by this **PI**.

Essential prime implicants  $BD$  and  $B'D'$ 27STUDENTS-HUB.com



Prime implicants CD, B'C,  $AD$ , and  $AB'$ Mohammed Khalil STUDENTS-HUB.com Uploaded By: 1230358@student.birzeit.edu **Example** Continue**:**

Essential prime implicants  $BD$  and  $B'D'$ 

Prime implicants CD, B'C,  $AD$ , and  $AB'$ 

The **simplified** expression is obtained from the **logical sum** of the **two essential** prime implicants and **any** two prime implicants that **cover** the remaining minterms (m3, m9, m11)

$$
F = \frac{BD + B'D'}{BD + B'D'} + CD + AD
$$
  
= 
$$
\frac{BD + B'D'}{BD + B'D'} + \frac{BC + AD}{BD + B'C + AD}
$$

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Avoid **Unnecessary overlap** amongst additional **selected PI's**

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- Θ **Functions** that have **unspecified** outputs for some input combinations are called incompletely specified functions
	- **D** Such situation arises in which some input variable combinations are not allowed OR might **never occur**
	- ↇ For example, in **BCD** there are six **invalid combinations**.
- Θ Since these **unspecified/unallowed** terms will **never** occur, they can be treated as **don't-care** terms with respect to their effect on the outputs
- Θ For these "**don't-care**" terms either a **1 or a 0 may** be assigned to the output ↇ it really **does not matter** since they will **never occur**
- Θ For the "**don't-care**" input combinations, an **X** is placed in the corresponding square (minterm)
- Θ When **grouping 1's**, the **X's** can be **treated as 1's** to form larger groups → **simpler expression**  $\bullet$  To get the simplified expression, we **must include all 1's** in the map, but we **may or may not include** any of the **X's**



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#### **Example: BCD Code : > 6**  $\rightarrow$  F=1





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#### Simplify the function  $F(w, x, y, z) = \Sigma(1, 3, 7, 11, 15)$ , which has **Extra Example:** the don't care conditions  $d(w, x, y, z) = \Sigma(0, 2, 5)$



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#### **Extra Example:**



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- Θ So far, We have been **combining minterms** (**'1' squares**), to get **F** as a **Sum of Products**  (SOP) out of the K-Map simplification process
- Θ If we combine the **remaining** minterms (**'0' squares**), we get the **compliment** of **F** => (**F'**) ↇ Using **DeMorgan**' s Theorem we can get **F** as a **Product-of-Sums** (POS) by complementing  $F' = > (F')' = F$

#### **Product of Sums (POS) Procedure**

- Combine the 0's into groups
- Form a sum-of-products (SOP) expression from these groups of  $0's \rightarrow F'$
- 3) Take its **complement** using DeMorgan's theorem to get **F** as **product-of-sum**



The following groups of 0's are formed:

- Red group:  $A'B'$
- Blue group:  $ABC'$
- Green group:  $B'C$

The expression of  $F' = A'B' + ABC' + B'C$ 

Use DeMorgan's theorem to find its complement in order to write an expression of  $F$ 

 $\texttt{S}$ TUDENTS-HUB.com  $F = (A + B)(A^2 + B^2 + C)$ Uploaded By: 1230358 @student.birzeit.celulii



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#### **Extra Example:**  $F(A, B, C, D) = \Sigma(0, 1, 2, 5, 8, 9, 10)$



$$
F = (AB + CD + BD')' = (A' + B')(C' + D')(B' + D)
$$

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# $\blacksquare$  **Extra Example:**  $\mathbf{F(A,B,C,D)} = \Sigma_{\text{m}}(3{,}9{,}11{,}12{,}13{,}14{,}15) + \Sigma \mathbf{d} \ (1{,}4{,}6)$





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# What if the function was **given** as **product of maxterms**?

- **1) Complement**  $F \rightarrow F'$  in **Sum-of Product** From (SOP)
- 2) Mark **F' minterms**' squares with **0's** and the **remaining** squares with **1's**.





# The map of **five** variables  $\rightarrow$  **two four** variable maps.



## **F(A,B,C,D,E)**

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#### **Example:**  $F(A, B, C, D, E) = \sum (0, 2, 4, 6, 9, 13, 21, 23, 25, 29, 31)$









**Example:**



- Θ Digital circuits are frequently constructed with **NAND** or **NOR** gates rather than with AND or OR gates.
- Θ **NAND** and **NOR** gates are **easier to fabricate** with electronic components and are **the basic gates** used in all Integrated Circuit (IC) digital logic families.
- Θ NAND and NOR gates are **universal gates** ↇ **Any** digital system can be **implemented** with **them**
- Θ To implement a function with **NAND** it need to be in **Sum-of Products** (SOP) form Θ To implement a function with **NOR** it need to be in **Product-of Sums** (POS) form

Rules have been developed to **convert** any logic circuit to its **equivalent** form in just **NAND gates or NOR gates**



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### **NAND Graphic Symbols**



- Θ **Both** Symbols are **same** because of DeMorgan's theorem
- Θ Circuits could be **drawn** using **any** of these symbols
- Θ When a circuit uses **both** symbols it is said to follow **mixed notation**

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- Θ A **set** of gates is **functionally complete** if **any** Boolean expression can be **realized** with this set of gates AND, OR, and inverter is functionally complete
- Any set of gates which can *implement* AND, OR and inverter is also functionally complete

**All** gates can be **represented** using Only **NAND** gates  $\rightarrow$  NAND is **functionally complete** 



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#### **Example:** Implement  $F = AB + CD$ , using NAND gates



#### **Inverts** on **same** line **cancel** each others





**Use the AND-Invert Form**



- Θ **Two-level Implementation using NAND Gates**
	- **1) Simplify** the function and express it in **sum-of-products** form.
	- 2) Draw a **NAND gate** for each product term of the expression that has **at least two literals**. The inputs to each NAND gate are the literals of the term. This procedure produces a group of **first-level gates**.
	- 3) Draw a **single gate** using the AND-invert or the invert-OR graphic symbol in the **second** level, with **inputs** coming from outputs of **first-level gates**.
	- 4) A term with a **single literal** requires an inverter in the first level. However, if the single literal is **complemented**, it can be connected **directly** to an input of the **second level NAND gate.**



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- Θ The general procedure for converting a **multilevel** AND–OR diagram into an **all-NAND** diagram using mixed notation is as follows:
	- **1) Convert** all AND gates to NAND gates with **AND-invert** graphic symbols.
	- **2) Convert** all OR gates to NAND gates with **invert-OR** graphic symbols.
	- **3) Check** all the bubbles in the diagram. For every **bubble** that is not compensated by another **small circle (bubble)** along the same line, **insert an inverter** (a one-input NAND gate) **or complement the input literal.**

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The **NOR** operation is the **dual** of the **NAND** operation. Therefore, all procedures and rules for NOR logic are the **duals** of the corresponding procedures and rules developed for NAND logic

## **NOR Graphic Symbols**



- Θ **Both** Symbols are **same** because of DeMorgan's theorem
- Θ Circuits could be **drawn** using **any** of these symbols
- Θ When a circuit uses **both** symbols it is said to follow **mixed notation**

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**All** gates can be **represented** using Only **NOR** gates → NOR is **functionally complete** 



Logic Operations with NOR gates

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**Example:** 
$$
F = (A + B)(C + D)E
$$

**Simplify** the function and express it in **product-of-soms** form









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#### **Extra Example:**

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#### *AND-OR to NAND Conversion*





20 24 *AND-OR to NOR Conversion*

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- Θ SOP and POS are **basic** forms of expressing functions
- Θ These functions can be implemented in **different** ways
- Θ So far, we have seen **multiple** ways of implementing the SOP and POS expressions
	- ✓ SOP can be represented as two-level **AND-OR** logic
	- ✓ SOP can be represented as two-level **NAND-NAND** logic
	- ✓ POS can be represented as two-level **OR-AND** logic
	- POS can be represented as two-level **NOR-NOR** logic

**How many two-level logics may be formed using the four types of gates (AND, OR, NAND, NOR)?**

 $2^4 \rightarrow 16$  Ways



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#### **How many two-level logics may be formed using the four types of gates (AND, OR, NAND, NOR)? <sup>2</sup>**  $2^4 \rightarrow 16$  Ways





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AND-OR NAND-NAND NOR-OR OR-NAND OR-AND NOR-NOR NAND-AND AND-NOR

- Θ The **first** gate listed in each of the forms constitutes a **first level** implementation.
- Θ The **second** gate listed is a single gate placed in the **second level**.
- Θ Note that any **two forms** listed in the same line are **duals** of each other.
- Θ The green four forms have been investigated **previously**.
- Θ The red four forms are investigated **next**.





## **AND-OR-INVERT** Implementation



- Θ The two forms **NAND-AND** and **AND-NOR** are equivalent forms and can be treated together
- Θ Both perform the **AND-OR-INVERT** function
- Θ The **AND–OR–INVERT** implementation is similar to **AND-OR** (SOP), except for the **inversion**

$$
F = (AB + CD + E)'
$$



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### **OR–AND–INVERT** Implementation



- Θ The two forms **OR–NAND** and **NOR–OR** are equivalent forms and can be treated together
- Θ Both perform the **OR–AND–INVERT** function
- Θ The **OR–AND–INVERT** implementation is similar to **OR-AND** (POS), except for the **inversion**

 $F = [(A+B) (C+D) E]'$ 



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Θ The following table summarizes the procedures for implementing a Boolean function in any one of the **four 2-level** forms: **NAND-AND, AND-NOR, OR-NAND and NOR-OR**



Θ Because of the **INVERT** part in each case, it is convenient if we find the **simplification of F'**

Θ When **F '** is implemented as an AND-OR or an OR-AND form, we can easily **get F** by simply **adding an INVERT at the end.** This will give us the circuit in one of the above-mentioned forms

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$$

$$
F(x,y,z)=\Sigma(0,6)
$$

## 1) Find the **simplified** form of **F '**

- $\checkmark$  Form a K-map and **group 0's**  $\hat{ }$  SOP form of **F**<sup><sup> $\checkmark$ </sup></sup>
- 2) Implement **F '** in a two-level **AND-OR** form
- 3) By adding a **NOT** gate at the output, we get **F**

Implementation With **AND-NOR** and **NAND-AND**

The resulting form is **AND-OR-INVERT** form which can be easily converted to get AND-NOR and NAND-AND forms



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$$

$$
F(x,y,z)=\Sigma(0,6)
$$

- 1) Find the **simplified** form of **F**
	- $\checkmark$  Form a K-map and **group 1's**  $\hat{\to}$  SOP form of  $\mathbf{F} \hat{\to}$  find  $\mathbf{F}'$  by taking the **complement** of **F**
- 2) Implement **F '** in a two-level **OR-AND** form

Implementation With **OR-NAND** and **NOR-OR**

- 3) By adding a **NOT** gate at the output, we get **F**
	- The resulting form is OR-AND-INVERT form which can be easily converted to get OR-NAND and NOR-OR forms







Remember: We always get a **SOP** from the K-map

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### *Other Two-Level Implementations –Summary*

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- Θ The **Exclusive-OR (XOR)** function is an important Boolean function used **extensively** in logic circuits.
- Θ Implemented **directly** as an electronic circuit (true gate) or implemented by **interconnecting other** gate types.
- Θ The **Exclusive-NOR (XNOR)** function, also known as **equivalence** function, is the **complement** of the **XOR** function.



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7STUDENTSH HUBBILGIN only when both X and Y are equal (equivalent). Uploaded By: 1230358@student.birzeit.edulil

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XOR: 
$$
x \oplus y = xy' + x'y
$$
  
\nXNOR:  $(x \oplus y)' = xy + x'y'$   
\n $x \oplus 0 = x, x \oplus 1 = x'$   
\n $x \oplus x = 0, x \oplus x' = 1$   
\n $x \oplus y' = x' \oplus y = (x \oplus y)'$   
\n $x \oplus y = y \oplus x$  Commutative  
\n $(x \oplus y) \oplus z = x \oplus (y \oplus z) = x \oplus y \oplus z$ 

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**Associative**

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Θ Multi-input XOR gates are **difficult** to fabricate with hardware

Θ Even a two-input gate is usually **constructed** with **other** types of gates



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*XOR is an Odd Function*

Θ The exclusive-OR operation with three or more variables can be expressed as:

$$
A \oplus B \oplus C
$$
  
=  $(AB' + A'B)C' + (AB + A'B')C$   
=  $AB'C' + A'BC' + ABC + A'B'C$   
=  $\sum (1, 2, 4, 7)$ 

Θ The multiple-variable exclusive-OR operation is defined as an **odd function** ('1' when **odd** number of **variables** are equal to **1**)



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Θ The complement of an **odd** function is an **even** function

$$
(A \oplus B \oplus C)' = \Sigma(0,3,5,6)
$$





## *K-Maps for XOR and XNOR Operations*

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- Θ A **parity bit** is an extra bit included with a binary message to make the **number of 1**'s either **odd or even**.
- Θ Parity bit is used for the purpose of **detecting errors** during the transmission of binary information.
- Θ The circuit that **generates** the parity bit in the **transmitter** is called a **parity generator**.
- Θ The circuit that **checks** the parity in the **receiver** is called a **parity checker**.
- Θ **Exclusive-OR/NOR** gates (Odd/Even Functions) are useful for generating and checking a parity bit





20 24 *Parity Generation/Checking (Application for Odd/Even Functions)* **ENCS** 2340

Transmitting a **3-bit** message with **even parity bit**. The three bits – x, y, and z constitute the message and are the inputs to the circuit. The parity bit **P** is the **output. Example:**

**Parity Generator**

**P** is **Even parity** bit  $\rightarrow$  P = 1 if the number of 1's in the 3-bit message is **odd**  $\rightarrow$ **P** is an **odd function** and can be implemented using **3-Inputs XOR**

$$
P=x\oplus y\oplus z
$$



**Parity Generator**

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## **Parity Checker**



- 1) The **three bits** in the message together with the **even** parity bit **P** are transmitted (**4 bits**)
- 2) The **receiver** at the destination checks for an **even** number of 1's in the **4-bit** message and
- generates an **error C** equal to 1 if the **number of 1's** in the message is **odd**
- **3) C** (error) can be implemented using **XOR**

$$
C = x \oplus y \oplus z \oplus P
$$



**Parity Checker**

 $C = 1 \rightarrow E$ rror





