

## Experiment NO.5

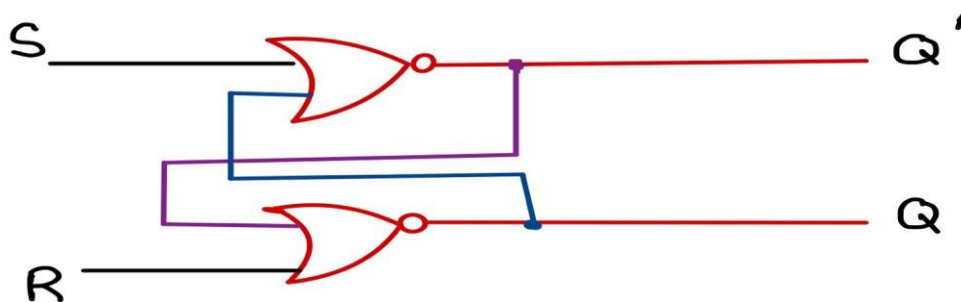
### Sequential Logic Circuit

#### Pre Lab

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Design the Logic Diagram, function table of the SR latch using NOR gates, and explain how it works.



Inputs		outputs		State
S	R	Q	Q'	
0	0	Q	Q'	No Change
0	1	0	1	RESET
1	0	1	0	SET
1	1	0	0	Invalid

**How it works?**

SR Latches From NOR gates work as following :

- ① When Set (S) = 1 , then Q = 1
- ② When Reset (R) = 1 , then Q = 0
- ③ When both set and Reset = 0 (S = 0, R = 0) then there is no change in value of Q
- ④ When both set and Reset = 1 (S = 1, R = 1) then the output is invalid , because it's impossible for Q and Q' to have the same value (Q = Q' = 0) . This is contradiction .