

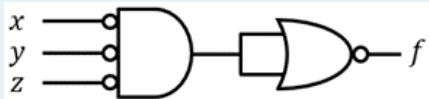
<b>Started on</b>	Thursday, 4 January 2024, 6:00 PM
<b>State</b>	Finished
<b>Completed on</b>	Thursday, 4 January 2024, 6:30 PM
<b>Time taken</b>	29 mins 55 secs
<b>Grade</b>	11.00 out of 12.00 (91.67%)

Question 1

Correct

Mark 1.00 out of 1.00

The following circuit is equivalent to:



- a. 3-input **OR** gate ✓
- b. 3-input **NAND** gate
- c. 3-input **XNOR** gate
- d. 3-input **AND** gate
- e. 3-input **NOR** gate

Question 2

Correct

Mark 1.00 out of 1.00

Given the Boolean function  $F(W, X, Y, Z) = \prod(0, 1, 2, 5, 8, 9, 10)$ , which of the following is not a **Prime Implicant** of  $F$  ?

- a. YZ
- b. XY
- c. XZ'
- d. None ✓
- e. WX



Question 3

Correct

Mark 1.00 out of 1.00

Which of the following expressions is **not** equivalent to  $X'$  ?

- a.  $X \text{ XOR } 1$
- b.  $X \text{ NAND } X$
- c.  $X \text{ NOR } 1$  ✓
- d.  $X \text{ NOR } X$
- e.  $X \text{ NAND } 1$

Question 4

Correct

Mark 1.00 out of 1.00

The Boolean function  $F(A, B, C, D) = A \oplus B \oplus C \oplus D = 1$  means:

- a. Half of the inputs are zeros (for example:  $A = 0, B = 0, C = 1, D = 1$ )
- b. All inputs are zeros ( $A = 0, B = 0, C = 0, D = 0$ )
- c. One or three of the inputs are ones ✓
- d. All inputs are ones ( $A = 1, B = 1, C = 1, D = 1$ )
- e. One or two or three of the inputs are ones



Question 5

Correct

Mark 1.00 out of 1.00

Given the following K-map of the Boolean function  $F(W, X, Y, Z)$ :

		YZ			
		00	01	11	10
WX	00	1	1	0	1
	01	1	X	X	1
	11	0	X	X	0
	10	1	1	0	0

Which of the following is an **Essential Prime Implicant** of  $F$ ? (Select all that apply)

- a.  $W'X$
- b.  $W'Z'$  ✓
- c.  $X'Y'$  ✓
- d.  $YZ$
- e.  $W'Y'$

Question 6

Correct

Mark 1.00 out of 1.00

The minimum product-of-sums (POS) expression for the Boolean function  $G(A, B, C, D)$  subject to the **don't care conditions** given in the following K-map is:

		CD			
		00	01	11	10
AB	00	X	1		
	01	1	1	X	1
	11	1	X	X	
	10		1		X

- a.  $G(A, B, C, D) = (B + D) \cdot (A' + C') \cdot (C' + D')$  ✓
- b. None
- c.  $G(A, B, C, D) = (B' + C) \cdot (A + B') \cdot (C + D')$
- d.  $G(A, B, C, D) = (B' + D') \cdot (A + C) \cdot (B' + C)$
- e.  $G(A, B, C, D) = (B + D) \cdot (A' + C') \cdot (B + C') \cdot (C' + D')$



Question 7

Correct

Mark 1.00 out of 1.00

A communication system for binary-coded decimal (**BCD**) codes uses even parity for error detection. Assume the sender wants to **send** the two numbers: 9 and 7. Then, the sender **transmits**:

**(Note:** In this communication system, the parity bit is padded/added for every transmitted BCD digit)

- a. 01001 10111 ✓
- b. 1 1001 0111
- c. 11001 00111
- d. 1001 0111
- e. 0 1001 0111



Question 8

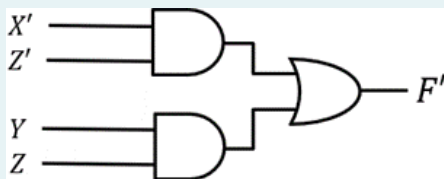
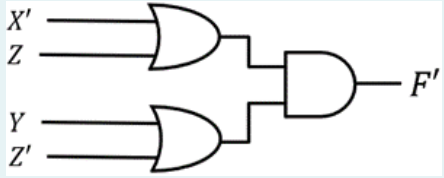
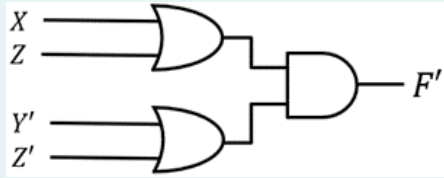
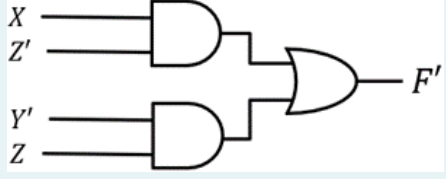
Correct

Mark 1.00 out of 1.00

Consider the following K-map of the Boolean function  $F(W, X, Y, Z)$ :

		YZ			
		00	01	11	10
WX	00	0	1	0	0
	01	1	1	0	1
	11	1	1	0	1
	10	0	1	0	0

The gate-level implementation for the **simplified complement** of  $F$  expressed as sum-of-products (SOP) is:

- a. 
- b. 
- c. None
- d. 
- e. 

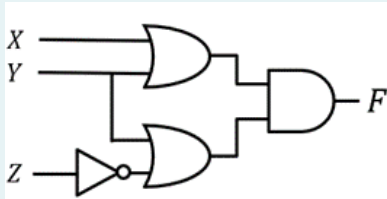


Question 9

Correct

Mark 1.00 out of 1.00

Given the following circuit diagram with AND/OR/NOT gates:



The equivalent **NAND** gates only implementation of the above circuit is:

- a. 

This diagram shows a NAND implementation with inputs X', Y', and Z. The first NAND gate has inputs X' and Y'. The second NAND gate has inputs Z and the output of the first NAND gate. The output of the second NAND gate is connected to a third NAND gate, which produces the output F.
- b. 

This diagram shows a NAND implementation with inputs X', Y', and Z'. The first NAND gate has inputs X' and Y'. The second NAND gate has inputs Z' and the output of the first NAND gate. The output of the second NAND gate is connected to a third NAND gate, which produces the output F.
- c. 

This diagram shows a NAND implementation with inputs X', Y', and Z'. The first NAND gate has inputs X' and Y'. The second NAND gate has inputs Z' and the output of the first NAND gate. The output of the second NAND gate is connected to a third NAND gate, which produces the output F.
- d. 

This diagram shows a NAND implementation with inputs X', Y', and Z. The first NAND gate has inputs X' and Y'. The second NAND gate has inputs Z and the output of the first NAND gate. The output of the second NAND gate is connected to a third NAND gate, which produces the output F. A green checkmark is next to this option.
- e. 

This diagram shows a NAND implementation with inputs X', Y', and Z. The first NAND gate has inputs X' and Y'. The second NAND gate has inputs Z and the output of the first NAND gate. The output of the second NAND gate is connected to a third NAND gate, which produces the output F.

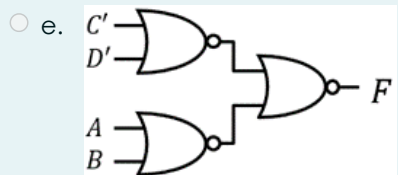
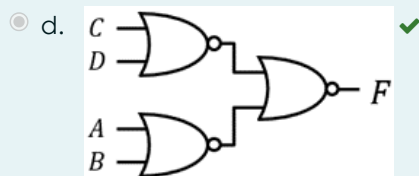
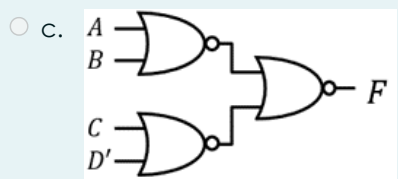
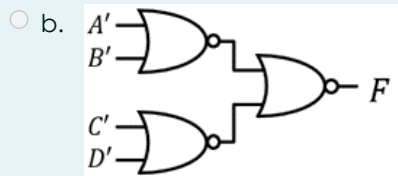
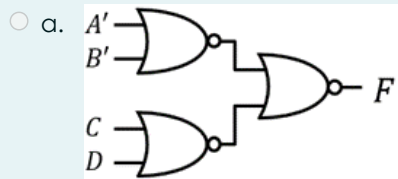


Question 10

Correct

Mark 1.00 out of 1.00

The implementation of Boolean function  $F(A, B, C, D) = (A + B) \cdot (C' \cdot D)'$  using **NOR** gates only is:



Question 11

Incorrect

Mark 0.00 out of 1.00

Consider the Boolean function  $F(W, X, Y, Z) = \sum(0, 1, 2, 4, 6, 10, 12)$  which has the don't care conditions  $D(W, X, Y, Z) = \sum(7, 13, 14, 15)$ , the minimum sum-of-products (SOP) expression of **F** is:

- a.  $F(W, X, Y, Z) = W'X'Y' + W'Z' + XZ' + YZ'$
- b.  $F(W, X, Y, Z) = W'X'Y' + W'Z' + XZ'$
- c.  $F(W, X, Y, Z) = W'X'Y' + W'Z' + YZ'$
- d.  $F(W, X, Y, Z) = W'X'Y' + XZ' + YZ'$
- e.  $F(W, X, Y, Z) = W'X'Y' + WX + XZ' + YZ'$  ✘



Question **12**

Correct

Mark 1.00 out of 1.00

Consider the circuit with the following *truth table*. The circuit has three inputs; **A**, **B**, and **C**. The output **Z** =

A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

- a. None
- b.  $B'C' + BC'$
- c.  $B'$
- d.  $BC + B'C$
- e.  $C'$  ✓

