Faculty of Engineering and Technology

Department of Electrical and Computer Engineering

ENEE 3102

Prelab for Experiment 6

Multistage Amplifiers and Frequency Response

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Prepared For:

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A. Multistage Amplifier:

I. Multistage Amplifier Design:

We want to design a two-stage amplifier with a voltage gain 30 to give a peak-to-peak output of 2.5 v.

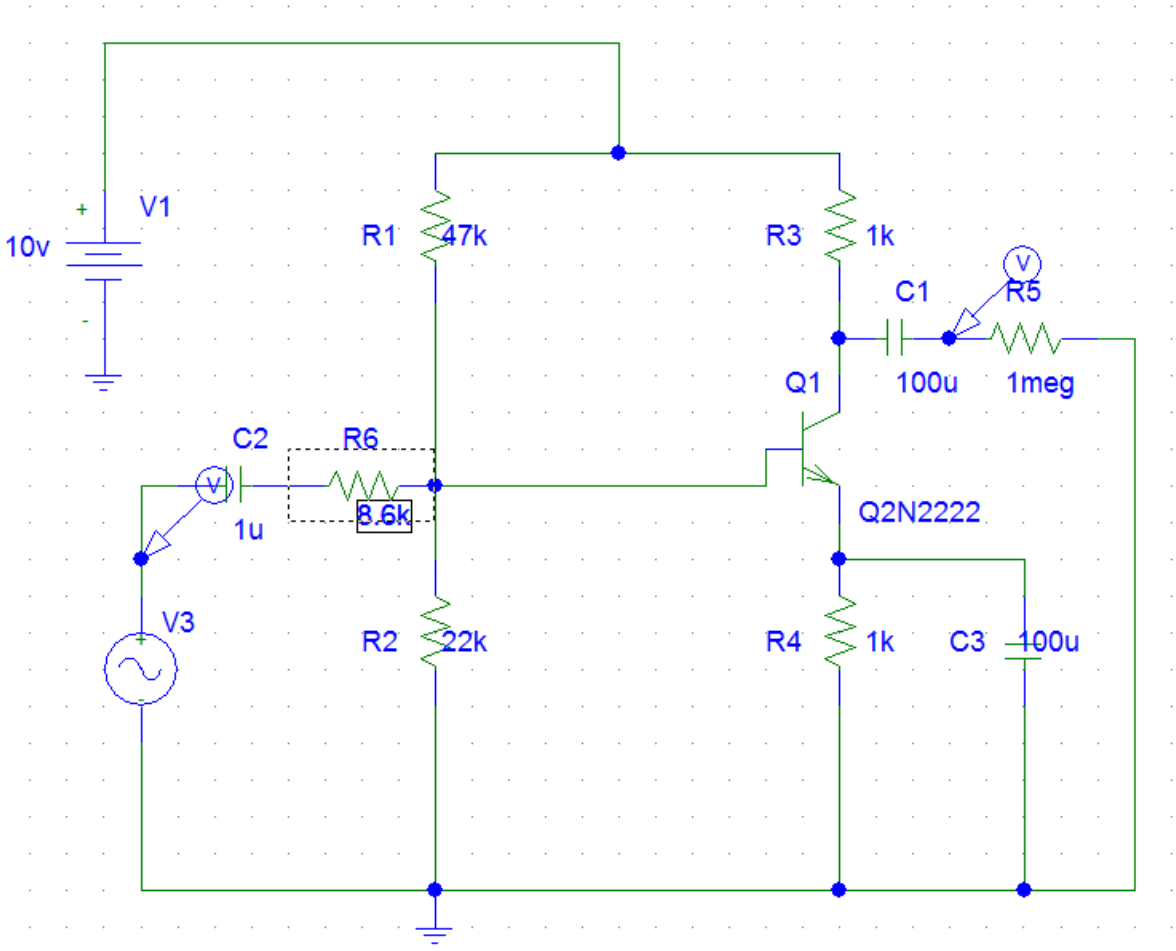
Av1 = 15, Av2 = 2, Vi = 100 mVp-p .

To design the first stage of the amplifier for the h-parameters of a transistor are:

hie = 2*$10^3\Omega$, hoe = 10^{-4} 1\Ω , hfe = 200 , hre = 10^{-3} , Vcc = 10v

The capacitor = 100uF in parallel with R_E.

So the first stage is:



The first stage in dc analysis

VB1=2.983v

VE1=2.317

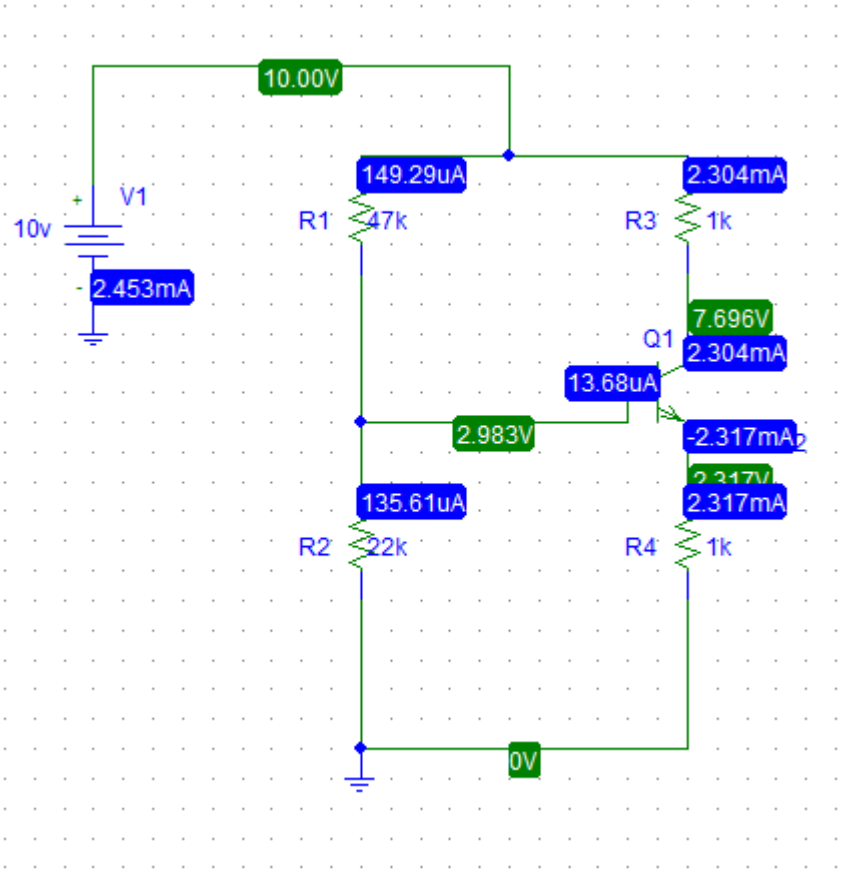
VCE1=7.696-2317v

h_{fe} = β = 168

$\frac{h_{ie} = \ 25.69mv}{13.68} =$

I_C = I_E = 2.304 mA

I_b = $13.68uA$



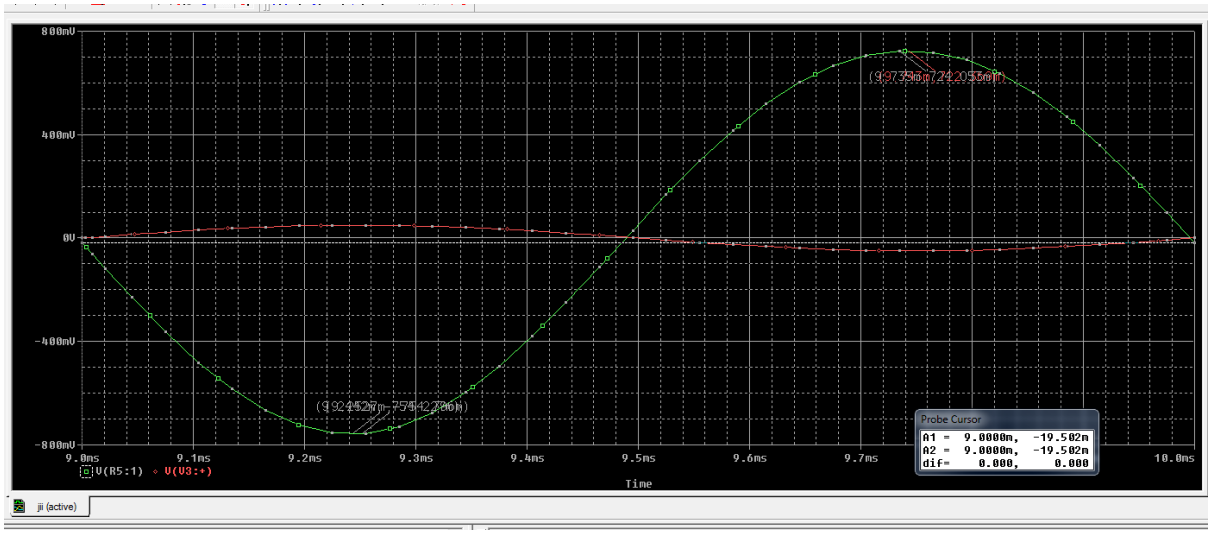
The first stage in dc analysis

VB1=2.983v

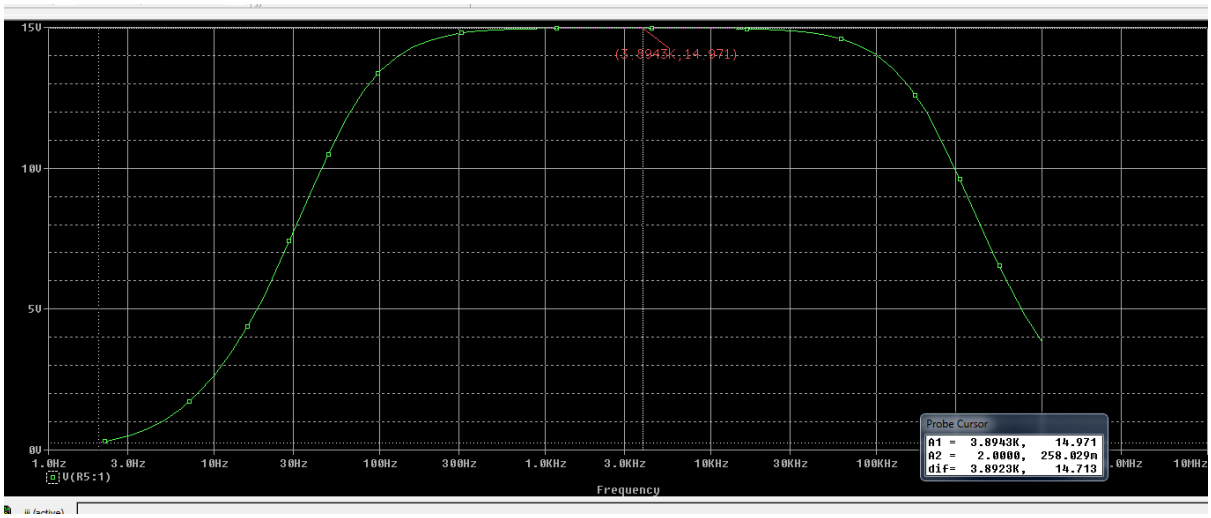
VE1=2.317

VCE1=7.696-2317v

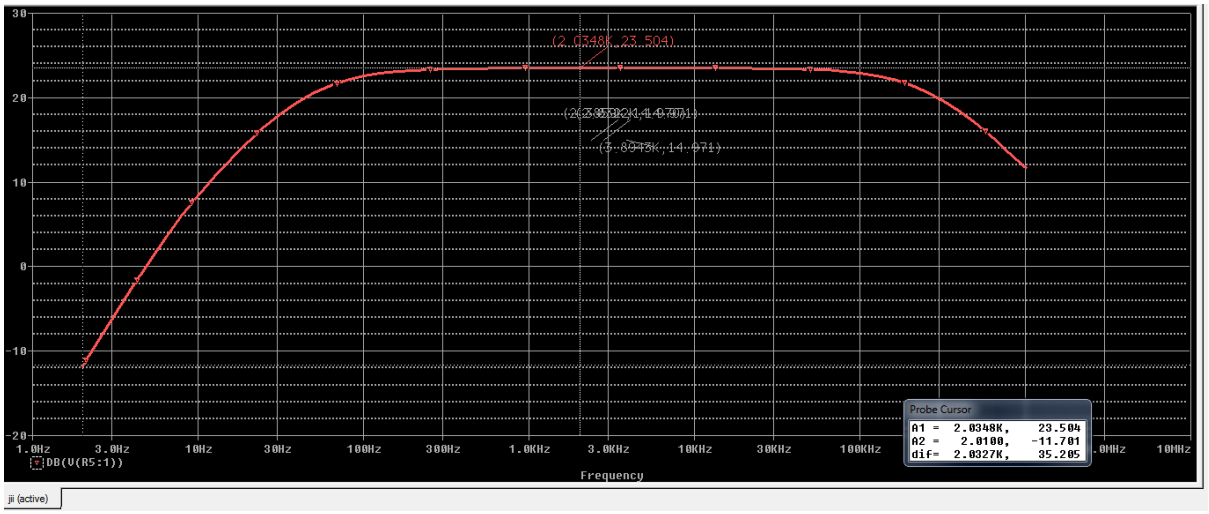
The simulation for first stage



AC analysis



When 24db=20log(15)



Stage 2 :

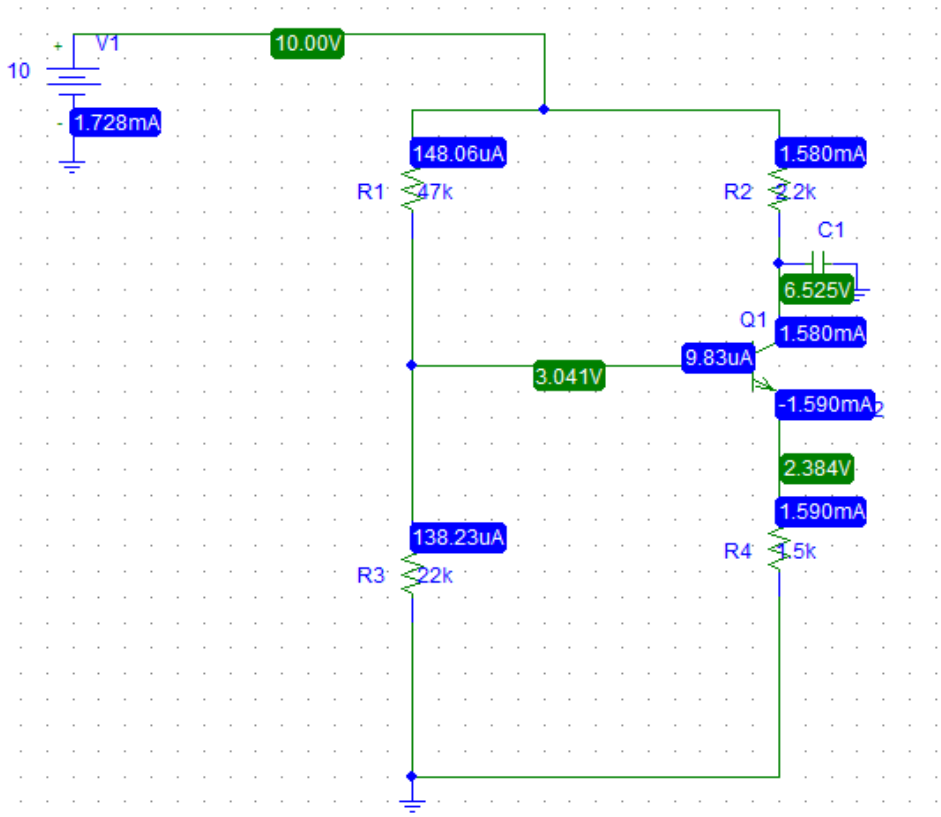
Q point

VB2=3.041V

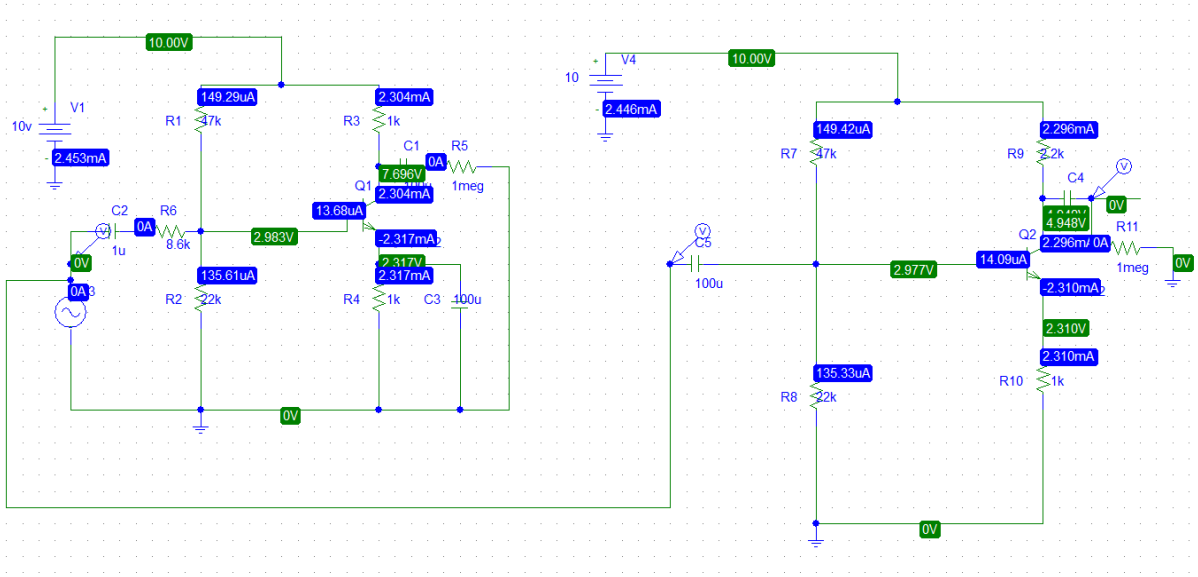
VE2=2.384V

VCE2=

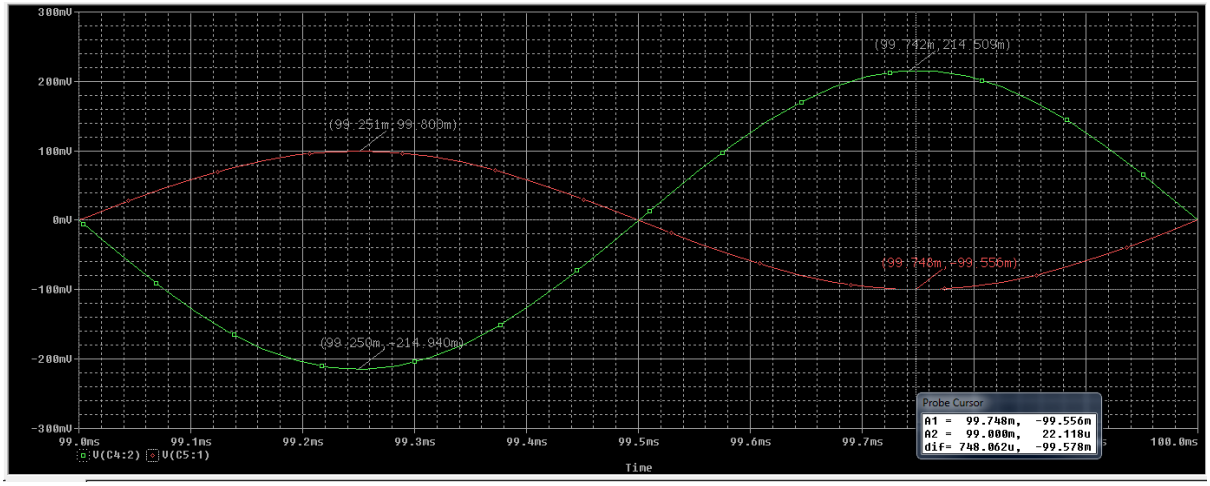
6.525-2.384=



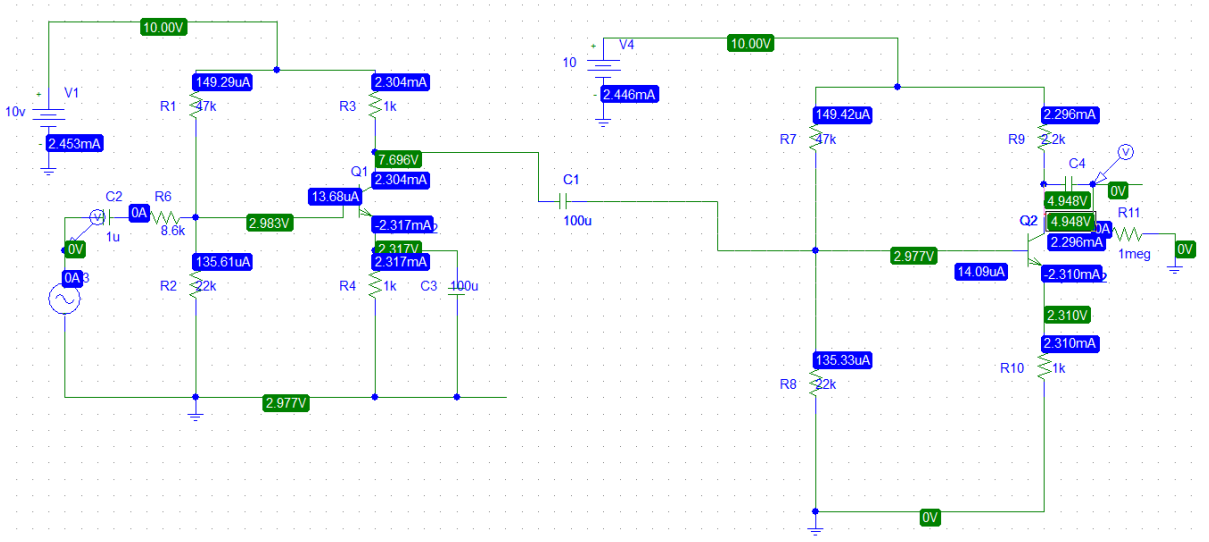
Then when connect two stages :



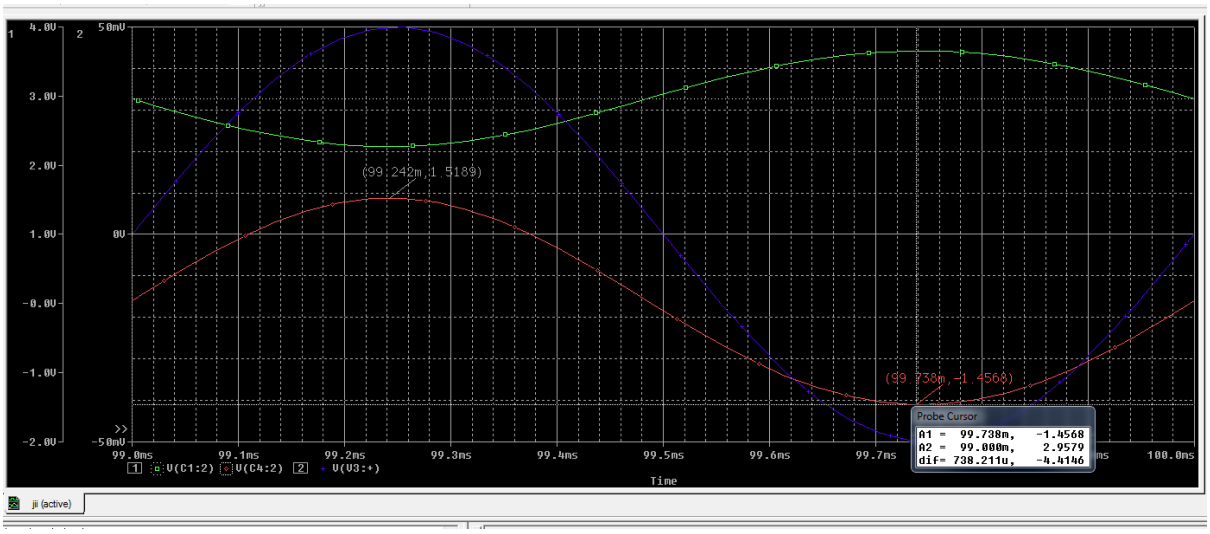
The output



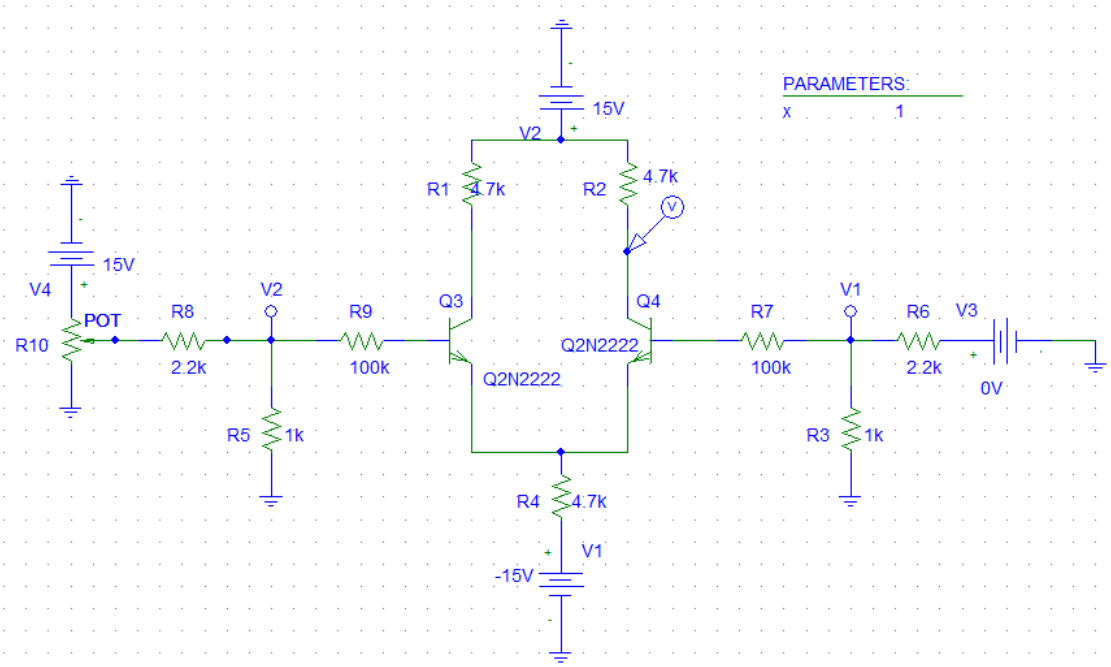
Two stages together :



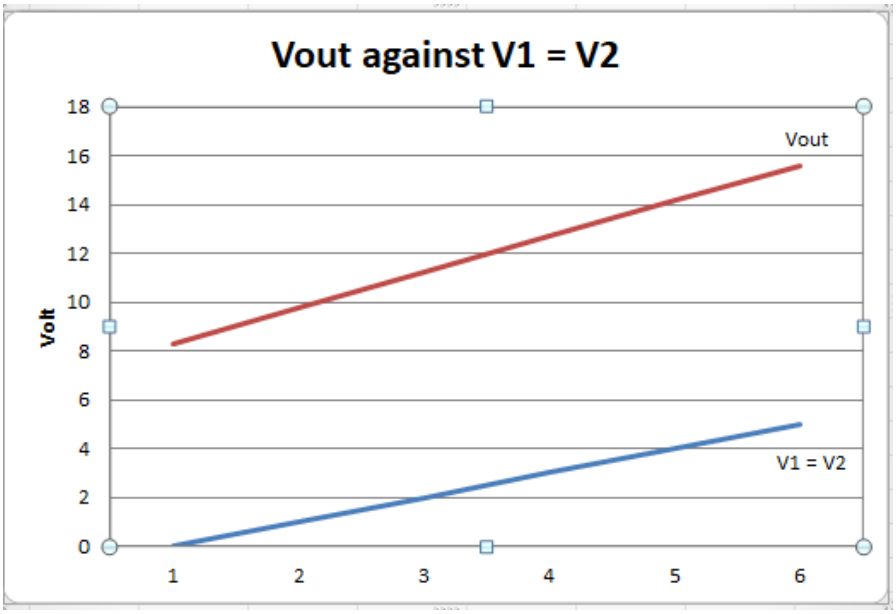
The simulation

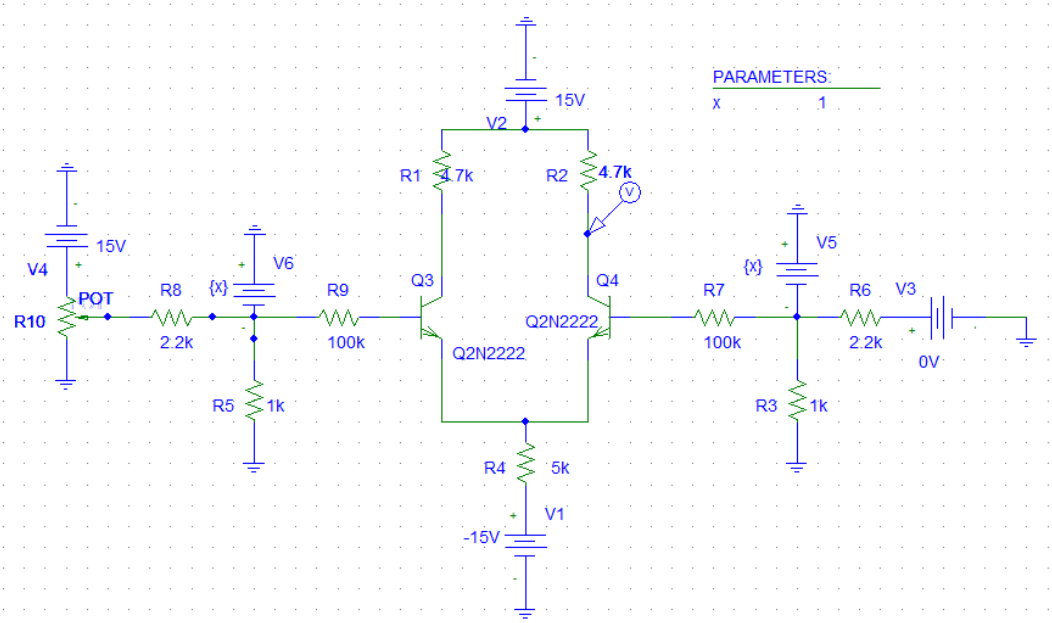


III. Differential Amplifier



$V_1 = V_2$ (V)	V_{out} (V)
0	8.286
1	8.750
2	9.214
3	9.680
4	10.15
5	10.61





V_1(V)	V_2 (V)	V_{out} (V)
0	0	8.667
0.05	-0.05	9.060
0.1	-0.1	9.454
0.15	-0.15	9.850
0.2	-0.2	10.24

The Slope = -1