Chapter 3 8- Gate-Level Minimization

* The complexity of digital logic gates is directly properties to the boolean expression from which the function 15 implemented.

$$= (X + \overline{X}) \cdot (X + \overline{Y})$$

we need to find the simplest boolean expression to describe the function

Minimize the function using algebra is a wakward approach (Lacks of specific rules to predict the next step).

50 we need another way for minimization which is

Map Method 3-straight forward

- Truth table 15 unique (befor and after minimization)

-1-

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× Karnaugh map (1c-map)

It is a diagram made of squares where each square represented one minterm.

2 variable map =

2 Variables -> 2 minterns = 4 minterns

$\overline{\chi}$	7	
0	0	mo
0	1	mi
1		M2
1	0	\ m3
	(\

Examples-Minimize the following functions

$$F(x,y) = \overline{xy} + x\overline{y} + x\overline{y}$$

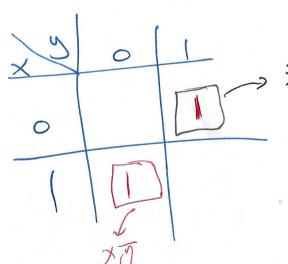
$$= x\overline{y} + x\overline{y} + x\overline{y}$$

$$= x\overline{y} + x(y+\overline{y})$$

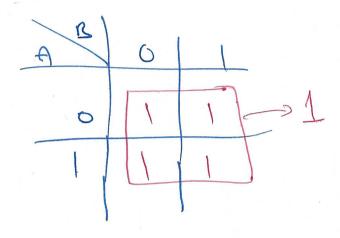
 $= (x + x) \cdot (x + y)$

Examples - minimize the following expression

m, + me



Example & minimize the following exert ssion =



$$F = \overline{A}(B + \overline{B}) + A(\overline{B} + B)$$

$$= \overline{A} + A = 1$$

* Three Voriables map

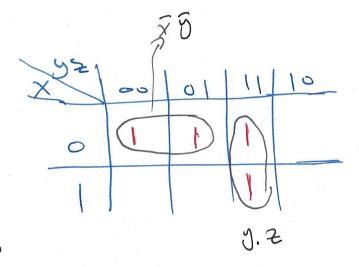
3 variables -> 2 = 8 minterns

XYZ	٥	1
00	mo	m (
01	MI	m 3
11	Mb	mz
10	m	ns l

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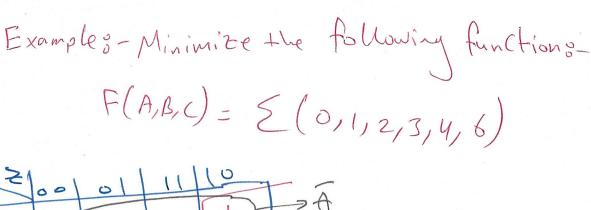
Examples-Minimize the following function using 12-map F(X, 972)= S(0, 1, 3, 7)

= mo+m1+m3+m7



	\times	S	そ	£
_	0	0	0	
	0	٥)	\ \
	0	\	0	0
	0		\	\ \
		0	0	0
	١	0	\	10
		1	0	0
	1	r.,	(- 1

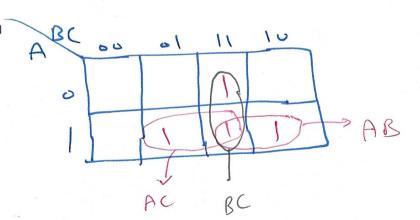
Example :- Minimize the following expression



F= A+C

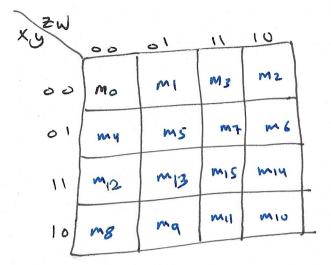
Examples-Minimize the following function

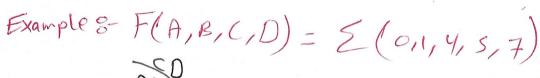
F(A,B,C) = m3 + m5 + m6 + m7

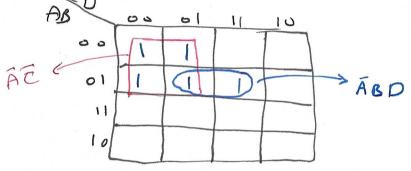


* Four Variables Maps

F(x, w, z, w) => 4 variables => 2=16 miterus = 16 squares

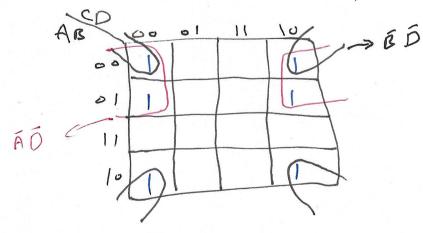






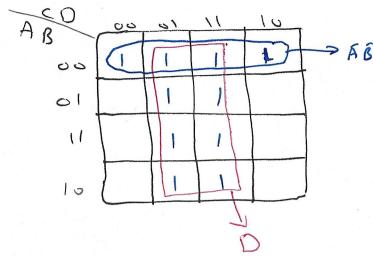
F=AC+ ABD

Example 3- Minimize Using 15-map F(A,B,GD) = & (0,2,4,6,8,10)



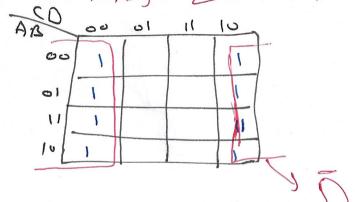
F= AD+BD

Examples - F(A,B,C,D) = \(\(\chi_{1/2}, 3, 5, 7, 13, 15, 9, 10 \)



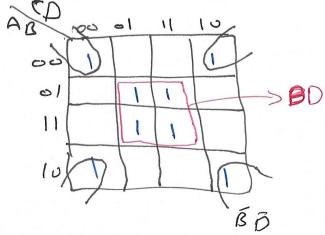
F= AB+D

Examples- F(A,B,C,D) = \((0,2,4,6,8,10,12,14) \)



F=D

Examples F(A,B,C,D)= {(0,2,5,7,8,10,13,15)

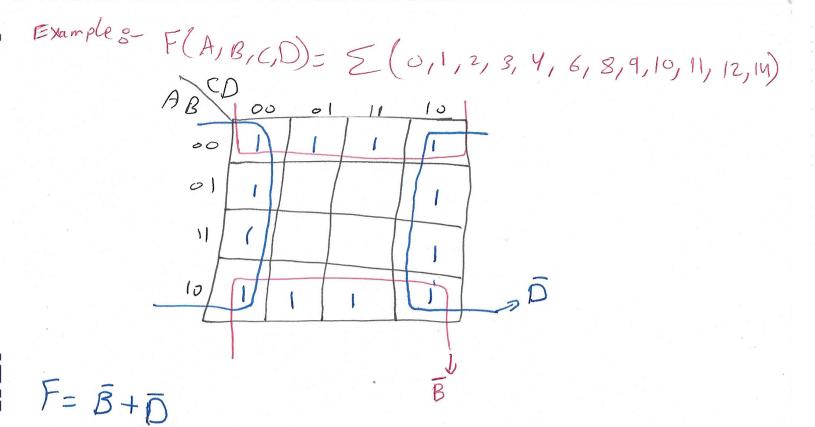


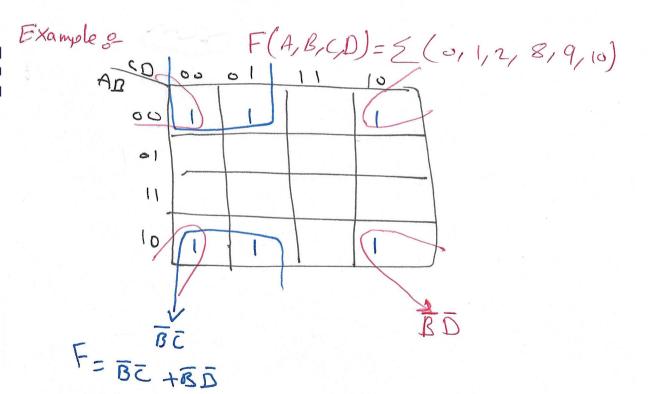
= (BOD)

XNOR

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* Five Variables Map

F(A,B,C,D,E) => 5 Variable => == 32 minterms

A = 0)			
PE	00	01	11	10
00	Mo	MI	m3	m2
01	my	ms	м	m6
()	mis	M13	mis	MIU
,	1000	ma	Mil	mio

NO COE	F
A B C D E	Mo
0 0 0 0 1	MI
0 0 0 0	mz
00011	M3
00000	me
0 0 1 0 1	ms
00110	ME
A=0 0 0 1 1	mit
0 1000	mg
0 1001	ma
0 1010	mio
01011	
0 110) wiz
0 110	Jui3
0 1 1 1	o nea
0 111	mis
1000	D M16
1000	1 MIT
	mix
1 6 6 1	1 ma
A=11001	* =
1010	D 120
1010	l mzi
,	o m22

DE		ol		10
BZ	m16	mIŦ	mia	m18
01	mio	mzl	me3	m22
11	mes	mzq	m31	m30
10	mzy	mrs	me7	m26

A=1

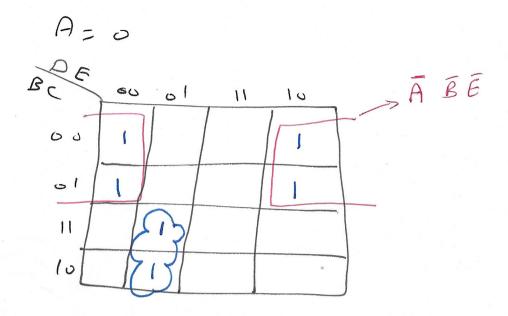
please note that mo is adjacent to mis

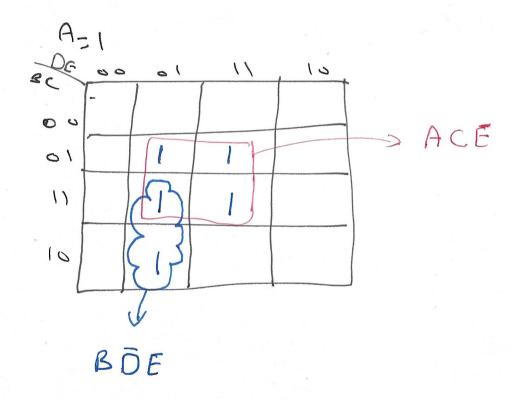
mi is adjacent to mit

and so an

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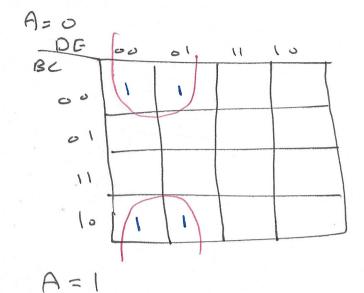
Example o- Minimize F (A,B,C,D,E)= E(0,2,4,6,9,13,21,23,25,29,3)

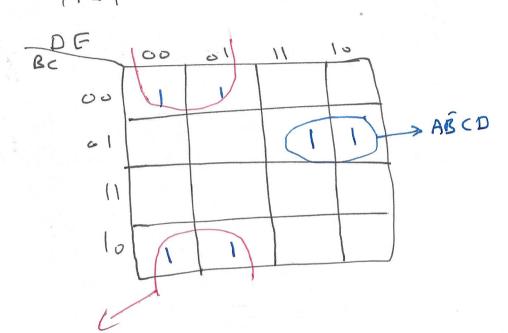




F= BDE + ABE + ACE

Example: F(A,B,C,D,E) = E(0,1,8,9,16,17,22,23,24,5)

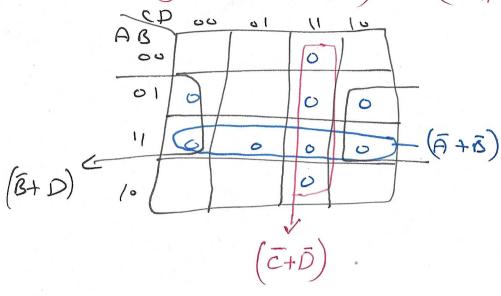




+ 05

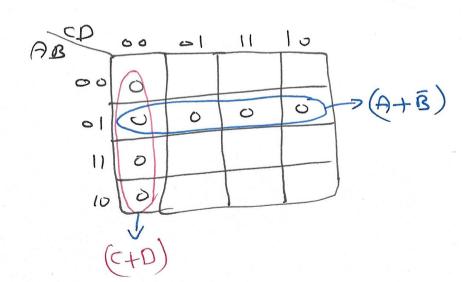
F= CO+ABCD

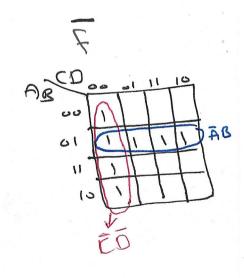
* Product of Maxterms



$$F = (\bar{A} + \bar{B}) \cdot (\bar{B} + D) \cdot (\bar{c} + \bar{D})$$

Examples F(A,B,C,D)=TT(0,4,5,6,7,8,12)





* Don't Corre Conditions-

A Function table may contain entries for wich

1- The input values of the Variables will never occur

2- The output value of the function is never used

Example & Gosider a function (f) defined over BCD inputs where the function output is (o) if the BCD input is (o-4), and the function output is (i) if the BCD input is (5-9). The function output is (X) if the input is (10-15)

F= E_(S,6,7,8,9) + Ed(10,11,12,13,14,15)

ABD ON THE SABC

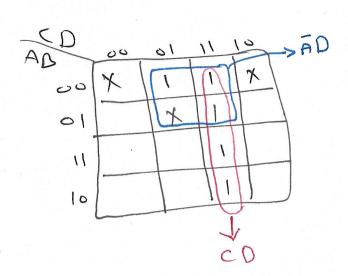
without using don't court F=ABD+ABC+ABC

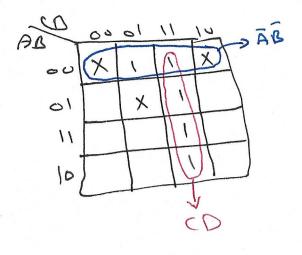
BD COOLING BC

with durt come F=A+BD+BC

ABCD	
	U
0000	0
0010	0
0011	O
0100	0
0101	1
0110	1
0 111	1
1000	1
1001	1
,010	X X X
1611	X
1100	X
, 101	X
, 110	×
, ,)	X
1 .	

Example 8- Simplify F = & (1,3,7,11,15) + & (0,2,5)





F= AD+CD

OY

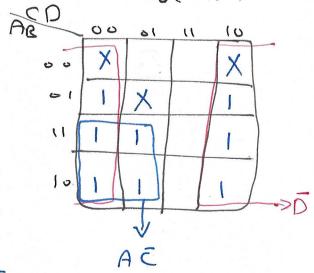
F=AB+CD

not all don't comes need to be covered

-15-

Example : Simplify F = & m(1,3,7,11,15) + &d(0,2,5)

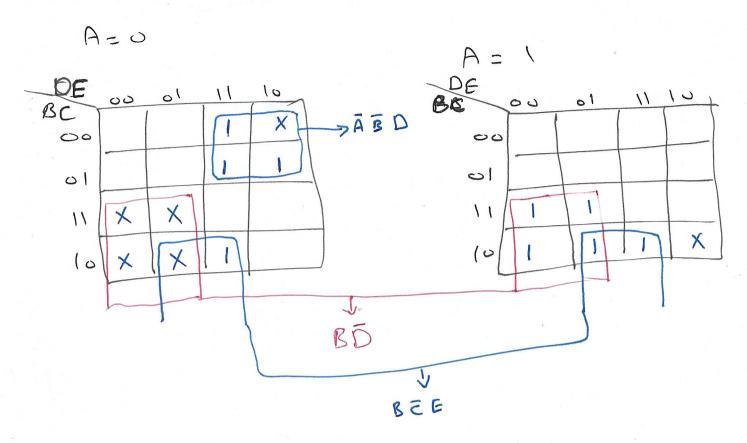
obtain a product of sums minimal expression



$$\vec{F} = A\vec{c} + \vec{D}$$

$$F = \vec{F} = (A\vec{c}) + \vec{D}$$
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Example & F(A, B, C, D, E) = Em(3,6,7,11,24,25,27,28,29) + Ed(2,8,9,12,13,26)



F = ABD + BCE + BD

* Prime Implicant and Essential Prime Implicant

Prime Implicants-approduct term Obtained by Combining the (PI) maximum number of adjacent squares in the K-map

Essential Prime Impliant = 15 a prime impliant that covers at least one (EPI)

minterm not covered tog the other prime impliants

Examples F(A,B,C,D) = E(0,2,5,7,8,10,13,15)AB

In this example we have

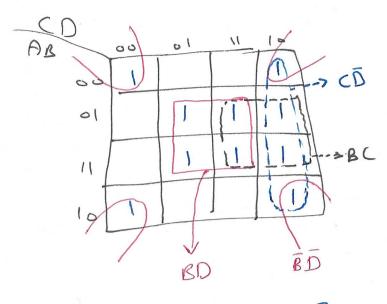
BD->PI two pinne Impliants and they

or are both essential

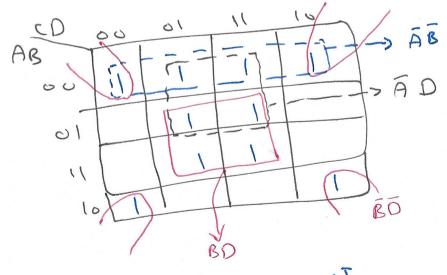
-16-

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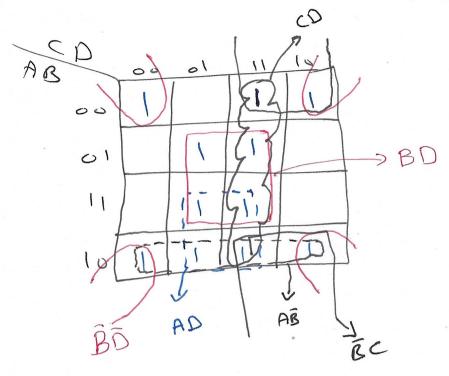
Examples F(A,B,C,D)= 5(0,2,5,6,7,8,10,13,14,15)



Example & F(A,B,C,D) = & (0,1,2,3,5,7,8,10,13,15)



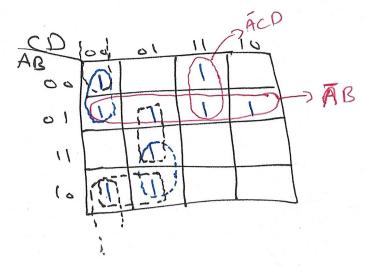
Example & F(A,B,C,D)= &(0,2,3,5,7,8,9,10,11,13,15)



So we have 6 prime Implicants

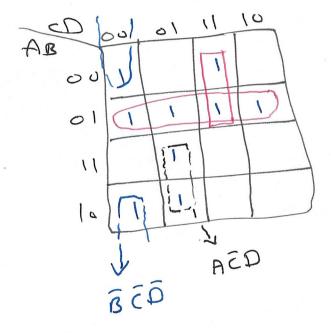
two are essential

Example & F(A,B,C,D) = \(\(\text{O}_1 \, 3, 4, 5, 6, 7, 8, 9, 13 \)



So we have 7 prime implicants

two ove Essential



F= AB+ ACD+ACD+BCD

NAND/NOR Implementation

NAND and NOR gates are said to be universal gates bacause any logic circuit can be implemented with It.

Digital Circuits are frequently constructed with NAND or NOR gates rather than with AND and OR gates for the following reasons:

1) use fewer transistors

Locus cost

Locus delay

Locus space

@NAND and NOR one easier to fabricate.

* NAND gate

$$\frac{A}{B} = \frac{A}{D} = \frac{A}{A} + \frac{B}{B}$$

$$= \frac{A}{A} + \frac{B}{B} = \frac{A}{B} + \frac{B}{B}$$

$$= \frac{A}{B} + \frac{B}{B} = \frac{A}{B} + \frac{B}{B} = \frac{A}{B} + \frac{B}{B}$$

$$= \frac{A}{B} + \frac{B}{B} = \frac{A}{B} + \frac{B}{B} = \frac{A}{B} + \frac{B}{B}$$

$$= \frac{A}{B} + \frac{B}{B} = \frac{A}{B} + \frac{B}{B} = \frac{A}{B} + \frac{B}{B} = \frac{A}{B} + \frac{B}{B}$$

$$= \frac{A}{B} + \frac{B}{B} + \frac{B}{B} = \frac{A}{B} + \frac{B}{B}$$

(1) NAND gate as inverter

$$A = Do (A.A) = \overline{A}$$
 $A = \overline{D} = \overline{A}$

@NAND Oute as AND

3) NAND gate as OR

$$A-DOA$$

$$B-DOB$$

$$OR$$

* NOR gate

$$A = D - F = (A + B)$$

$$= A - B$$

$$= A - B$$

O NOR as inverter

$$A = D \circ F = (A+A) = \overline{A}$$

A - Do-A
inverter

2 NOR as OR

$$A = D = D = A + B$$

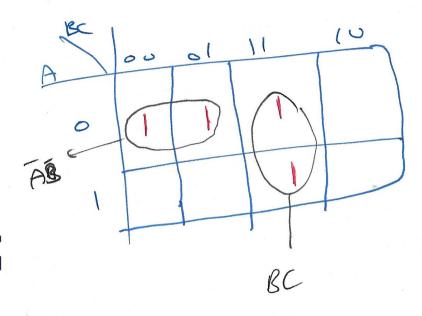
$$A = D = A + B$$

(3) NOR as AND

XAND-OR Implementation

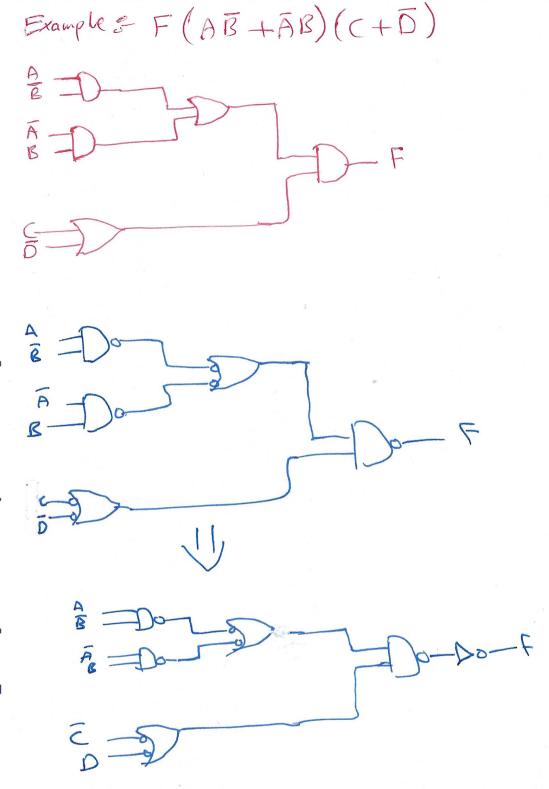
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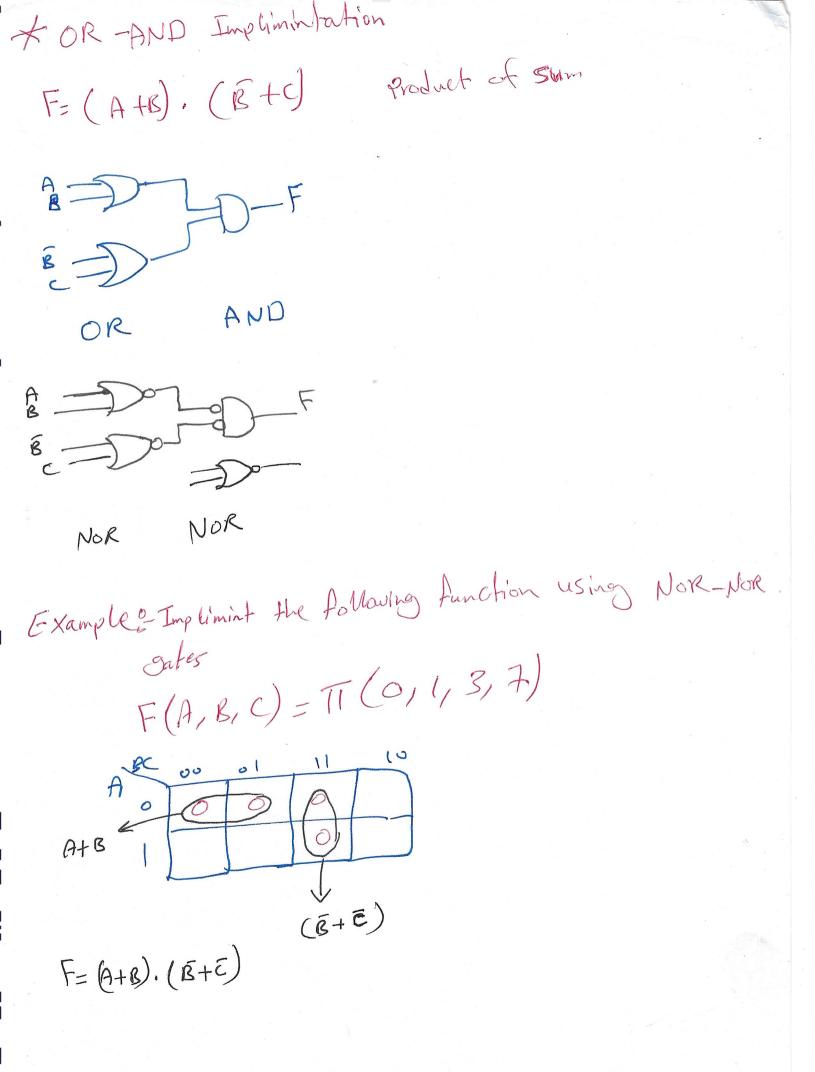
Example 8- Implement the following Function with NAND gates

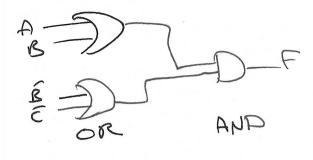


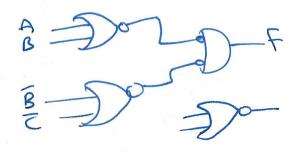
CHAM

MAND









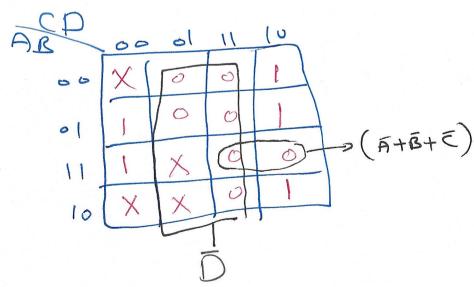
NOR

NOR

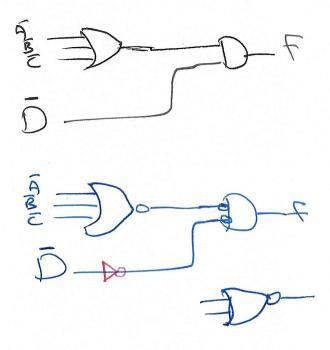
Examples - F(A,B,GD) = 2(2,4,6,10,12)

d (A,B,C,D) = 2(0,8,9,13)

Implimint the function using NOR gates



F= D. (A+B+C)



* Parity Generators

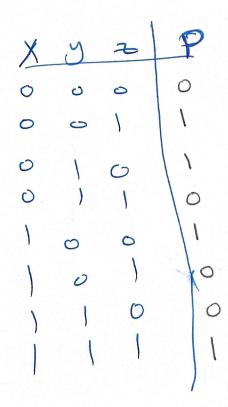
Parity & Extra bit added to the message to check

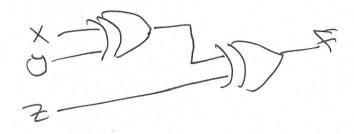
If the recieved message is correct (single error)

Parity & Even

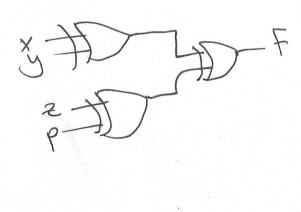
Examples - Design even parity generator and Checker for 3-bit codes

odd parity -> even Function even parity -> odd Function





×	5	7	9/	Check
0	0	0	0	0
0	O	0	1	1
G	0	1	0	1
0	0	1	1	0
0		0	0	1
0	1	0	1	0
0	1	1	O	0
0	1	١	1	1
\	0	0	0	1
1	0	D	1	0



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Example 9- F= (AB + AB) E(C+D)

