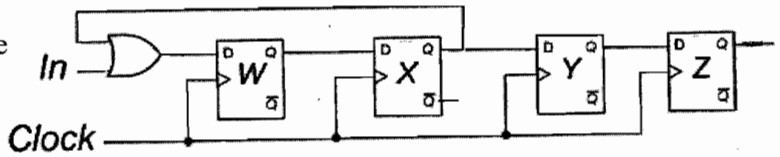
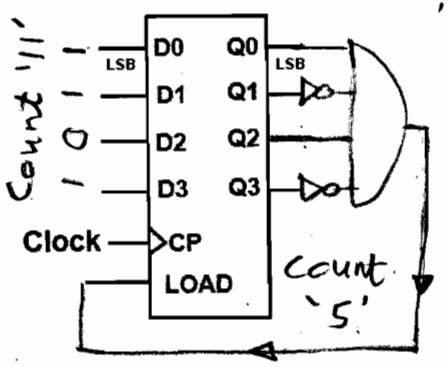
1. Initially the feedback D-type shift register shown has the contents WXYZ = 0110. For the sequence of the serial input shown in the table below, fill in the spaces in the table to indicate the register contents following the arrival of each of the next five clock pulses. In the last column, express the contents in HEX.



Clock Pulse #	Serial Input, just before the arrival of the next clock pulse	W $D_W = In + X$	X $D_X = W$	Y $D_Y = X$	Z $D_Z = Y$	Register Contents (in Hex)
Initial State	1	1 0	1	1	0	6
1	0	0 1	0	1	1	B
2	0	1 0	1	0	1	5
3	1	1 1	0	1	0	A
4	0	1 1	1	0	1	D
5	1	1	1	1	0	E

2. Given the 4-bit synchronous binary down counter with a parallel load synchronous input (LOAD) (shown opposite).



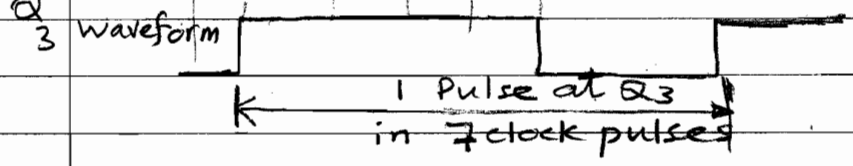
   a. Add the required logic to obtain a counter that follows the following counting sequence: …11, 10, 9, 8, 7, 6, 5, 11, 10, 9, 8, 7, 6, 5, …..

   b. This counter is a modulo- 7 counter.

   c. This counter is a divide-by- 7 counter.

   d. Sketch the Q3 output (the MSB) for the counting sequence given in (a) above and use the result to verify your answer in (c).

Count: 5 11 10 9 8 7 6 5 11 10
Q3 0 1 1 1 1 0 0 0 1 1



   e. With a clock frequency of 1400 pulses per second, the signal at output Q3 of the counter has a frequency of 200 pulses per second.

1400/7 = 200

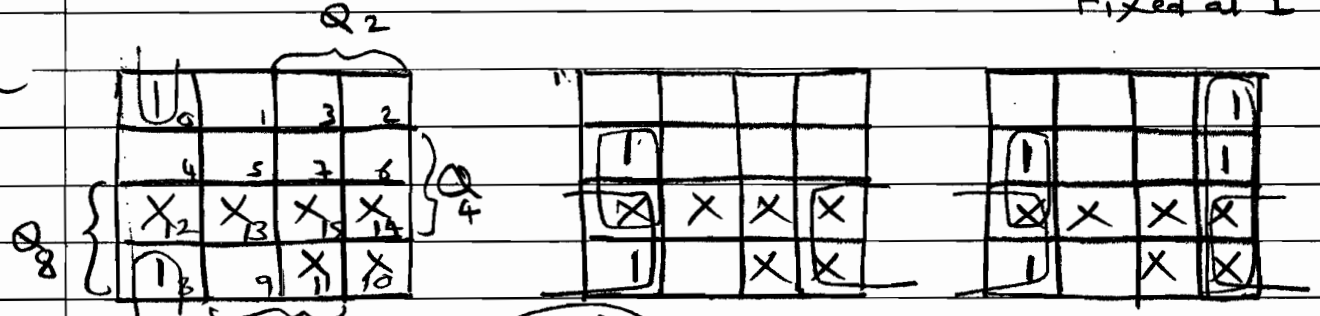
3. a. JK FFs with J,K tied together

(J,K=1 : Toggle, JK=0 : No change)

State Table for BCD Down Counter

	Present State				Next State				$[J,K]_8$	$[J,K]_4$	$[J,K]_2$	$[J,K]_1$
	Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1				
0	0	0	0	0	1	0	0	1	1	0	0	1
1	0	0	0	1	0	0	0	0	0	0	0	1
2	0	0	1	0	0	0	0	1	0	0	1	1
3	0	0	1	1	0	0	1	0	0	0	0	1
4	0	1	0	0	0	0	1	1	0	1	1	1
5	0	1	0	1	0	1	0	0	0	0	0	1
6	0	1	1	0	0	1	0	1	0	0	1	1
7	0	1	1	1	0	1	1	0	0	0	0	1
8	1	0	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	0	0	0	0	0	0	1

Fixed at 1



$[J,K]_8$

$J_8 = K_8 = \bar{Q}_1 \bar{Q}_2 \bar{Q}_4$

$J_1 = K_1 = 1$

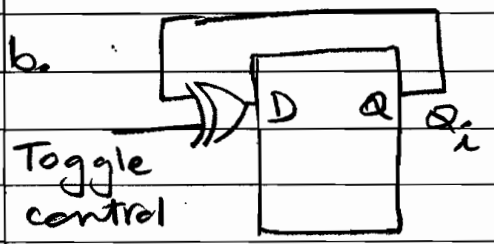
$[J,K]_4$

$J_4 = K_4 = \bar{Q}_1 Q_8 + \bar{Q}_1 \bar{Q}_2 Q_4$

$[J,K]_2$

$J_2 = K_2 = \bar{Q}_1 Q_2 + \bar{Q}_1 Q_8 + \bar{Q}_1 \bar{Q}_2 Q_4$

b.



($= [J,K]_i$ from part (a) above)

$D_8 = Q_8 \oplus [\bar{Q}_1 \bar{Q}_2 \bar{Q}_4]$

$D_4 = Q_4 \oplus [\bar{Q}_1 Q_8 + \bar{Q}_1 \bar{Q}_2 Q_4]$

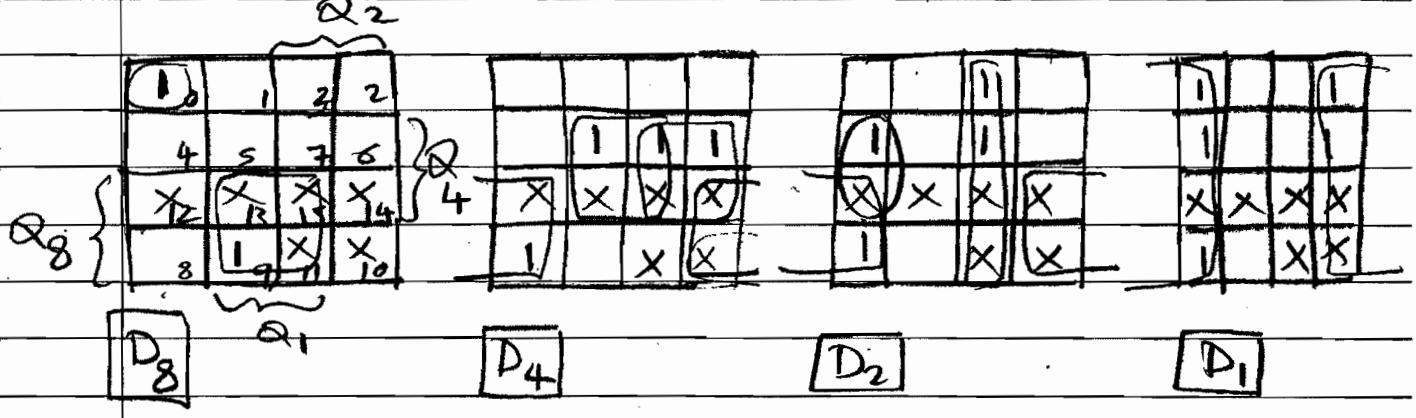
$D_2 = Q_2 \oplus [\bar{Q}_1 Q_2 + \bar{Q}_1 Q_8 + \bar{Q}_1 \bar{Q}_2 Q_4]$

$D_1 = Q_1 \oplus 1$

$= \bar{Q}_1$

c. DFFs with D inputs obtained directly from the state table (FF is set/reset).

on p. 2



$D_8 = Q_1 Q_8 + \bar{Q}_1 \bar{Q}_2 \bar{Q}_4 \bar{Q}_8$

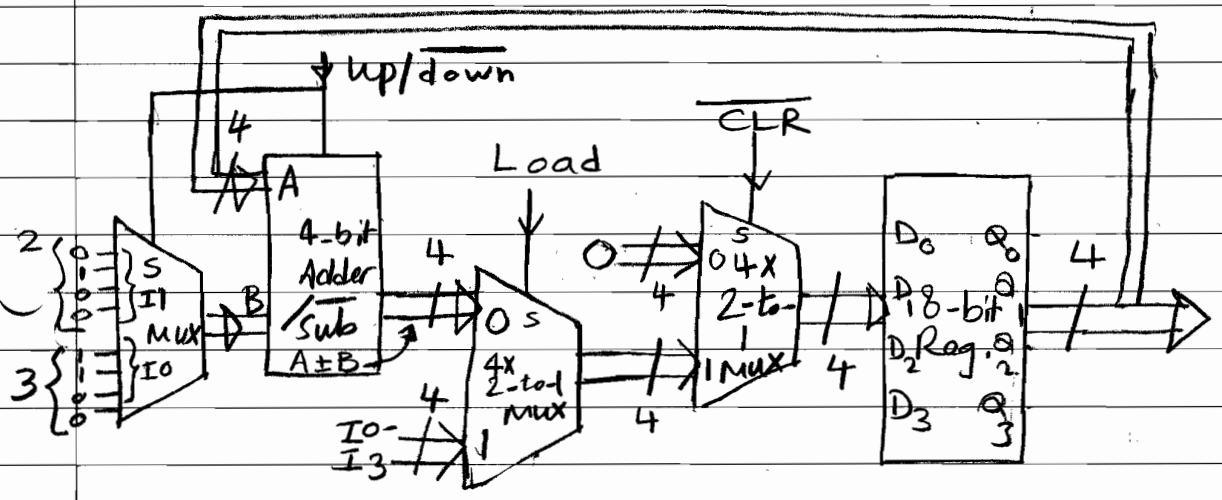
$D_4 = Q_2 Q_4 + Q_1 Q_4 + \bar{Q}_1 Q_8$

$D_2 = Q_1 Q_2 + \bar{Q}_1 Q_8 + Q_1 \bar{Q}_2 Q_4$

$D_1 = \bar{Q}_1$

6.

CLR	Load	Up/down	Action Taken on Next Clock Edge
0	X	X	Clear counter
1	1	X	Parallel Load with External Inputs (I3I2I1I0)
1	0	0	Decrement by 3
1	0	1	Increment by 2



7.

S1 S0

00: No change

01: // Load external data

10: Rotate right

11: Load with 1's complement of Register contents