Field Effect Transistor : FET

Advantager

1. high input impedance ; 100M Ω
2. fewer steps in the manufactoring process.
3. more devices Can be package into smaller area for integrated Circuit IC

Disadvantager

1. Low Valuer of Voltage gain.
2. poor high frequency performance.

FET types

1. Junction Field Effect Transistor : JFET

   n-channel JFET
   p-channel JFET

2. Metal Oxide Semiconductor FET : MOSFET

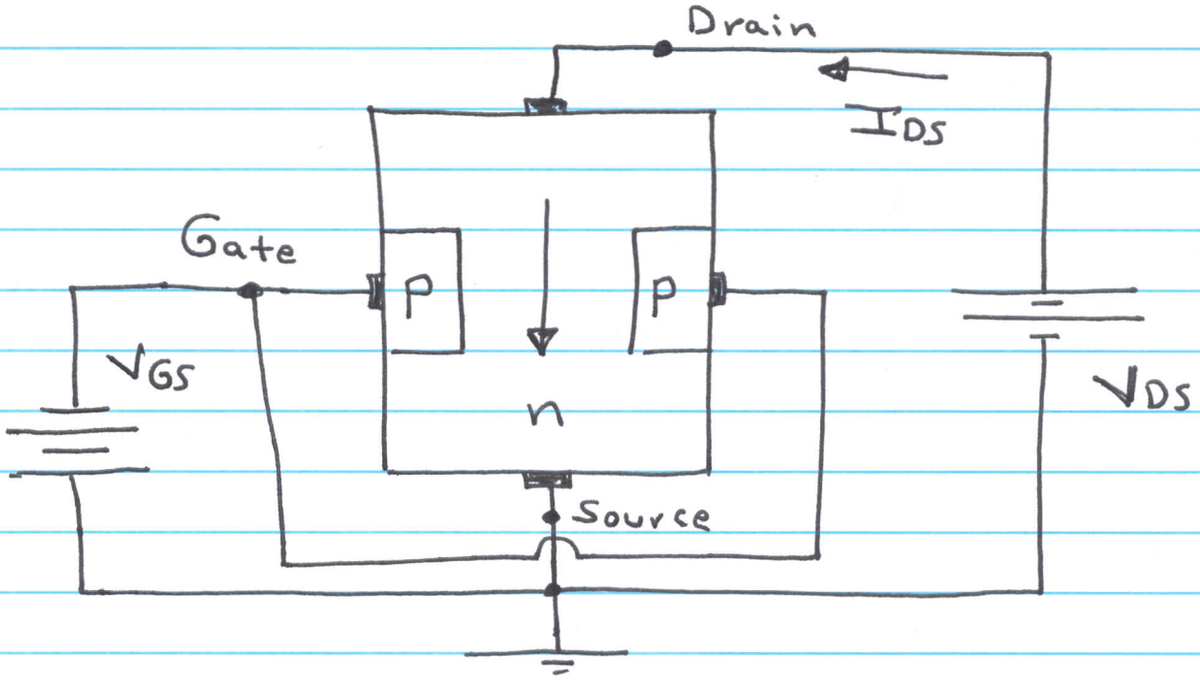
   a) Depletion type MOSFET : DMOSFET

      n-channel DMOSFET
      p-channel DMOSFET

   b) Enhancement type MOSFET : EMOSFET

      n-channel EMOSFET
      p-channel EMOSFET

JFET Construction



n-channel JFET

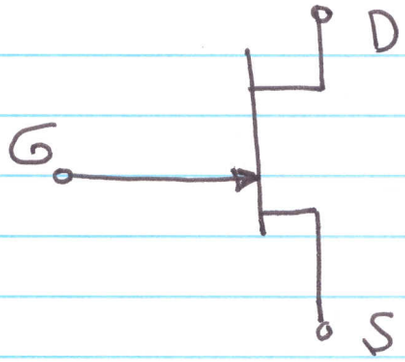
- Reverse biasing the gate to source junctions causes the formation of depletion regions.
- The drain has the proper polarity with respect to the source, to establish the drain current I_{DS}.
- The value of I_{DS} depends on the width of the channel.
- The width of the channel is Controlled

by reverse biasing the pn junctions between gate and source.

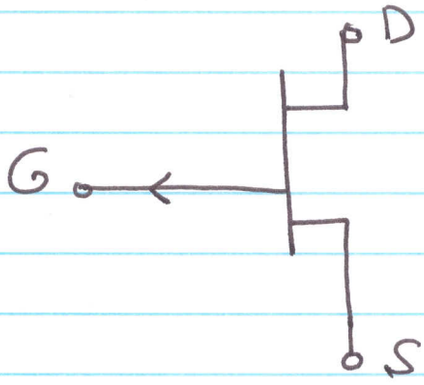
- If the channel width increases, I_{DS} increases.

JFET Circuit symbol

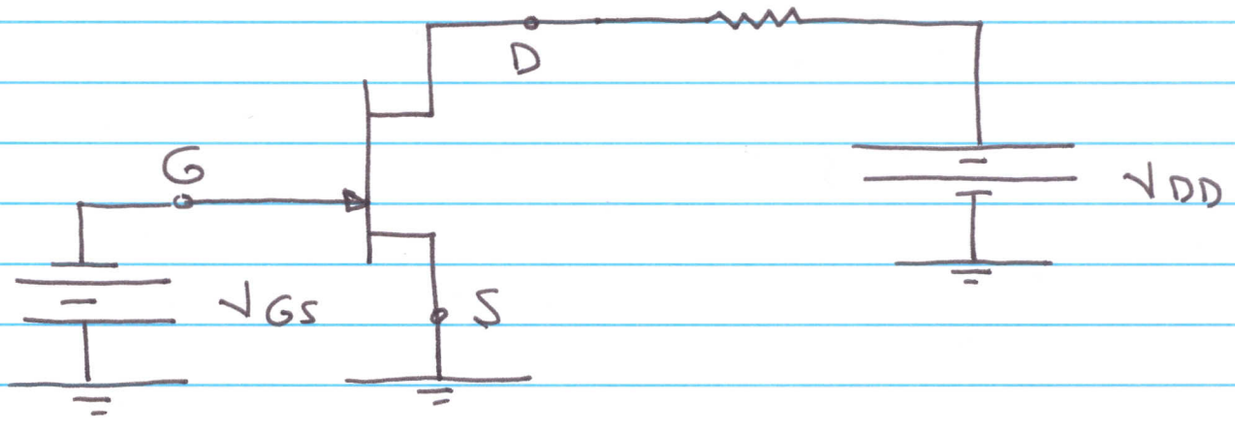
1) n- channel JFET

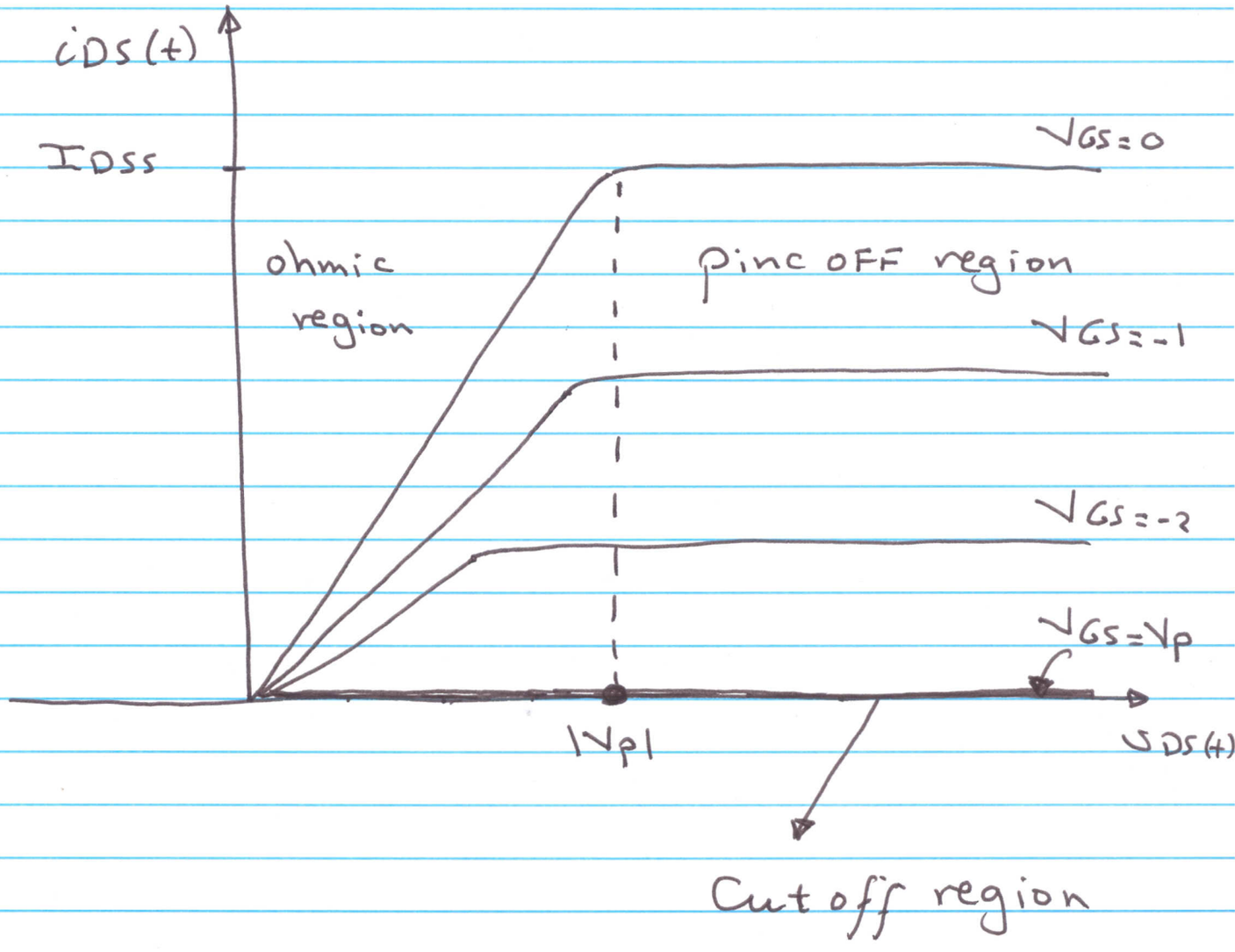


2) p- channel JFET

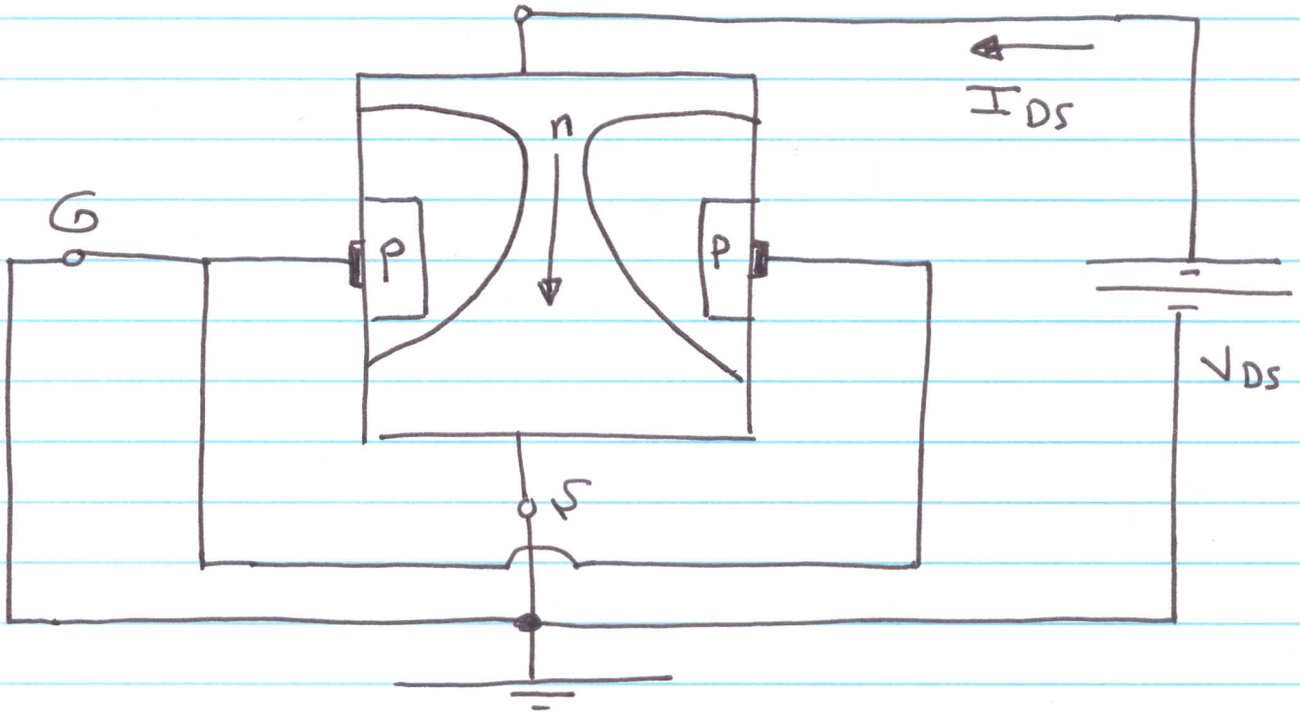


JFET output characteristic





Pinch off Voltage : V_p



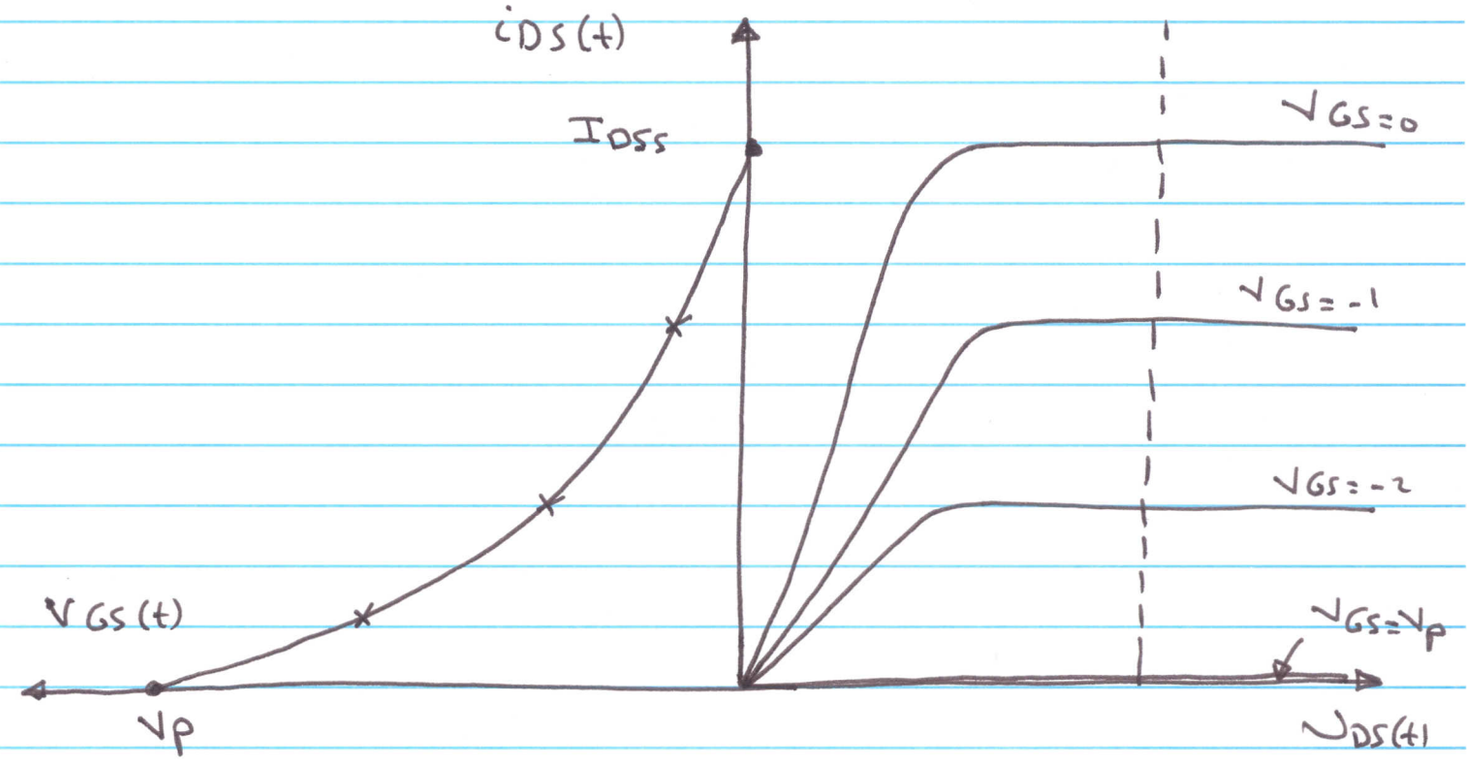
For $V_{GS}=0$, the value of V_{DS} at which I_{DS} becomer essentially Constant is the absolute of the pinch off voltage

$$V_{DS} = |V_p|$$

$$V_p = \begin{cases} \text{negative value for n-channel} \\ \text{positive value for p-channel} \end{cases}$$

JFET Transfer characteristic Curve

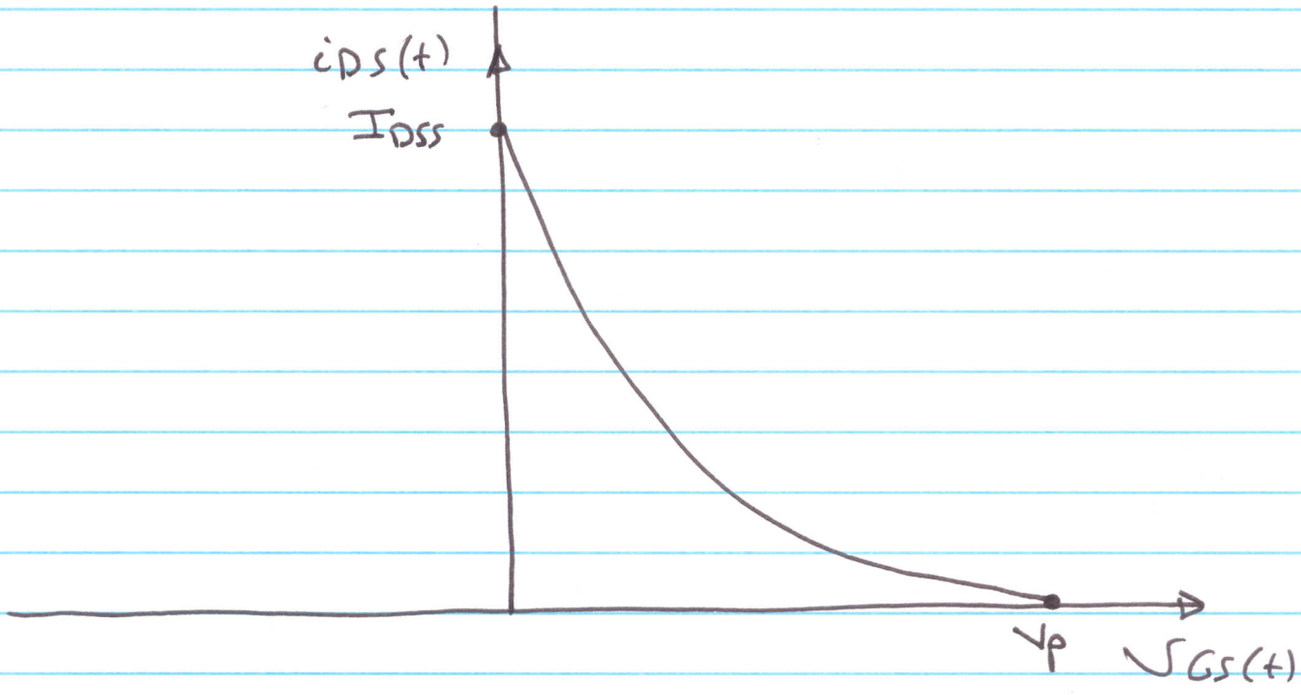
1) n-channel



$$i_{DS}(t) = I_{DSS}\left(1 - \frac{V_{GS}(t)}{V_p}\right)^2$$

* In the pinch off region
* $V_p < V_{GS} \leq 0$
* $|V_{DS}| > |V_p| - |V_{GS}|$

2) For p-channel JFET



In the pinch off region

$$i_{DS}(t) = I_{DSS}\left(1 - \frac{V_{GS}(t)}{V_p}\right)^2$$

$$|V_{DS}| > |V_p| - |V_{GS}|$$

$$V_p > V_{GS} \geq 0$$

Pinch off Voltage

The voltage that causes the depletion region to touch and close the channel is called pinch off voltage.

For the n-channel JFET to be in the pinch off region

$$0 \geq V_{GS} > V_p$$

and $|V_{DS}| > |V_p| - |V_{GS}|$

For the p-channel JFET to be in the pinch off region

$$V_p > V_{GS} \geq 0$$

and $|V_{DS}| > |V_p| - |V_{GS}|$