



DEPARTMENT OF COMPUTER SYSTEM ENGINEERING

Digital Integrated Circuits - ENCS333

Dr. Khader Mohammad

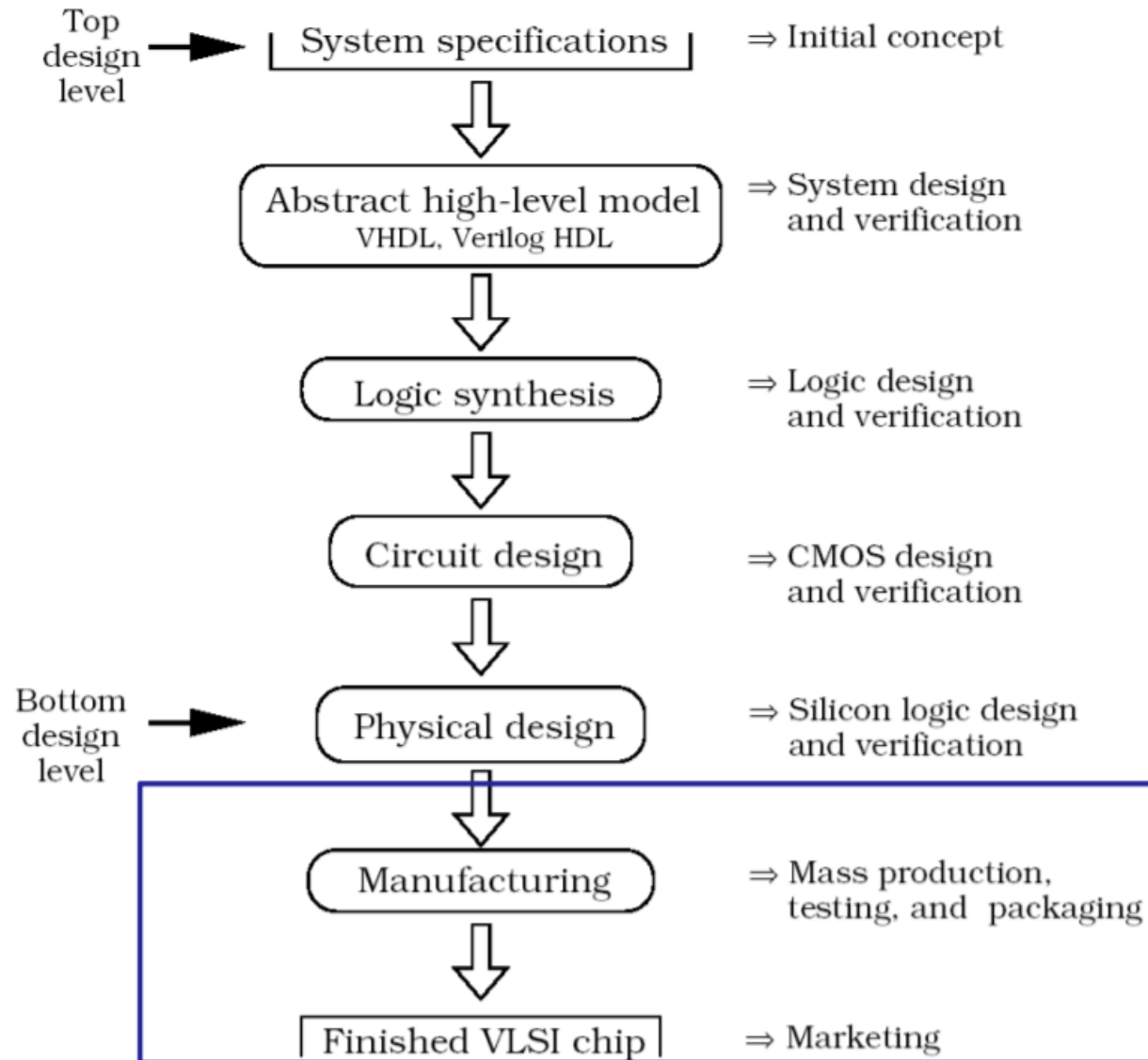
Lecture #3- Design Flow

Integrated-Circuit Devices and Modeling

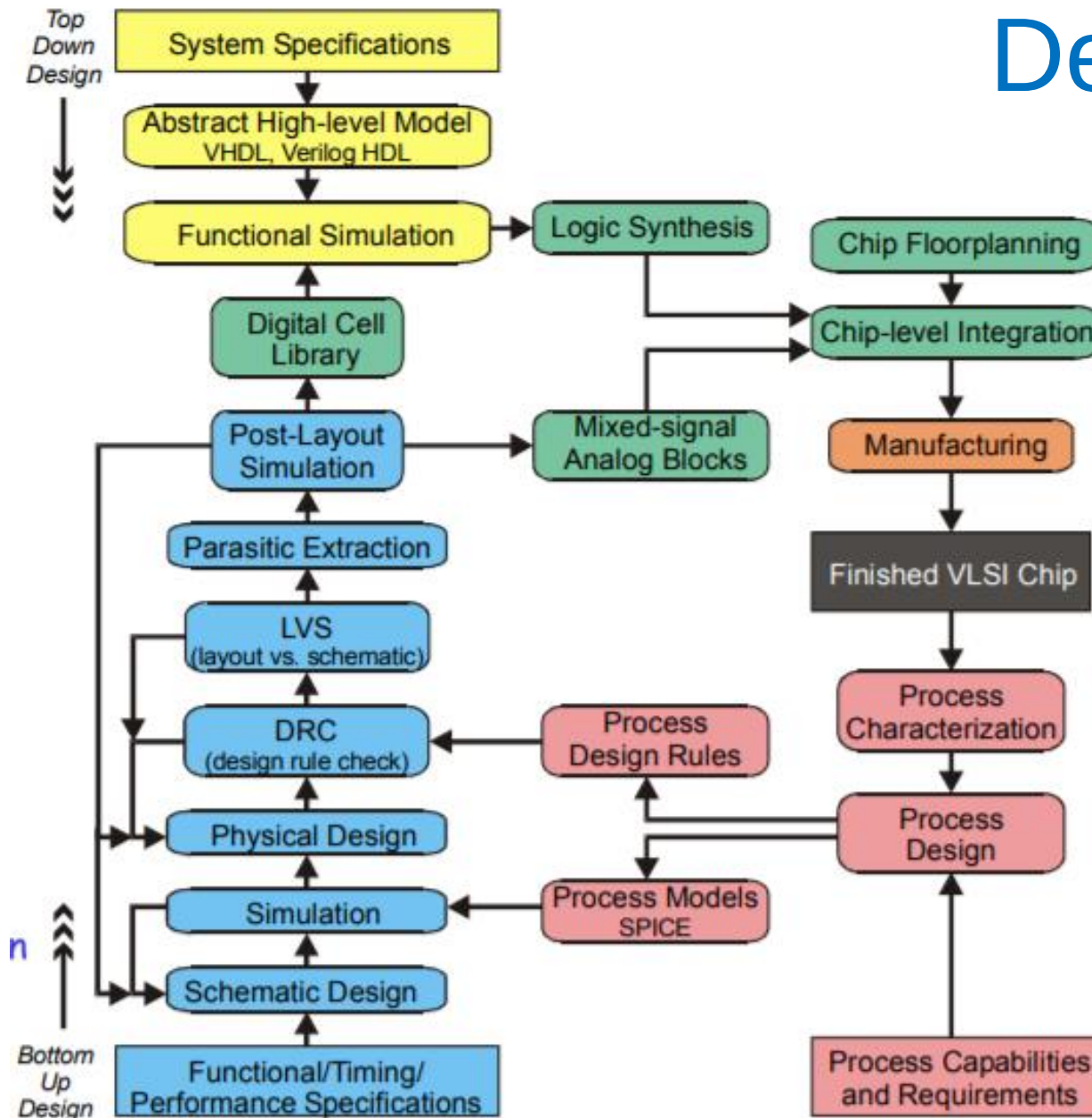
Integrated Circuit Technologies

- Why does CMOS dominate?
 - Other technologies
 - passive circuits , III-V devices, Silicon BJT
- CMOS dominates because:
 - Silicon is cheaper preferred over other materials
 - physics of CMOS is easier to understand?!!
 - CMOS is easier to implement/fabricate
 - CMOS provides lower power-delay product
 - CMOS is lowest power
 - can get more CMOS transistors/functions in same chip area
- Note: CMOS is not the fastest technology!, III-V devices, Silicon BJT Is faster

General overview of the design hierarchy



Design flow



VLSI – very large scale integration

lots of transistors integrated on a single chip •

Top Down Design

Bottom Up Design

Silicon in 2010

Die Area: 2.5x2.5 cm
Voltage: 0.6 V
Technology: 0.07 μm

	Density (Gbits/cm ²)	Access Time (ns)
DRAM	8.5	10
DRAM (Logic)	2.5	10
SRAM (Cache)	0.3	1.5

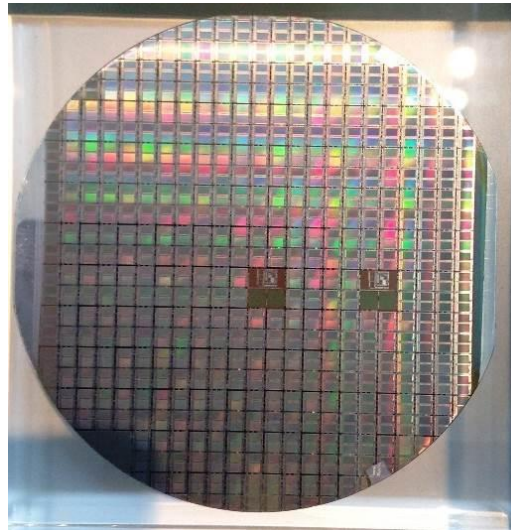
	Density (M gates/cm ²)	Max. Ave. Power (W / cm ²)	Clock Rate (GHz)
Custom	25	54	3
Std. Cell	10	27	1.5
Gate Array	5	18	1
Single-Mask GA	2.5	12.5	0.7
FPGA	0.4	4.5	0.25

Producing a Wafer

Watch : Sand to silicon



Producing a Wafer (2)

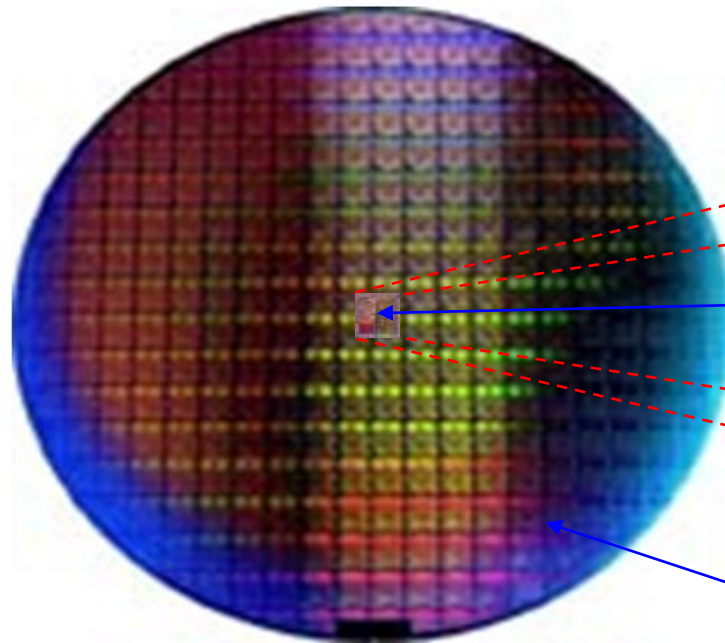


Wafer and Die

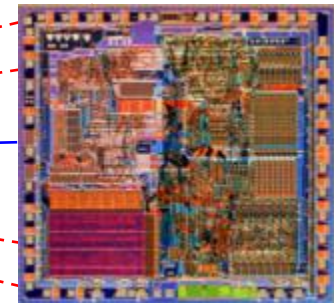
- CMOS ICs are fabricated on circular slices of silicon called wafers.
 - Wafer contains various identical dies.

<https://www.youtube.com/watch?v=aWVywhzuHnQ>

Side view of a Wafer



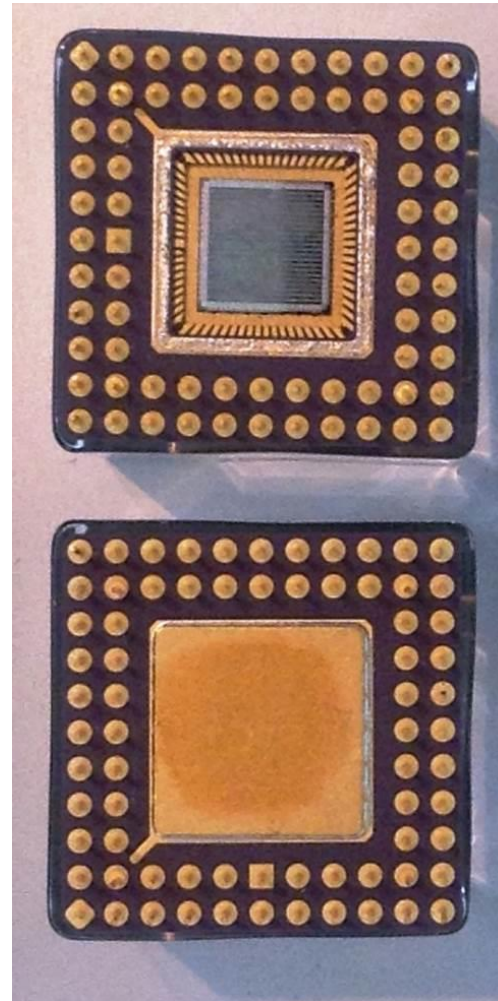
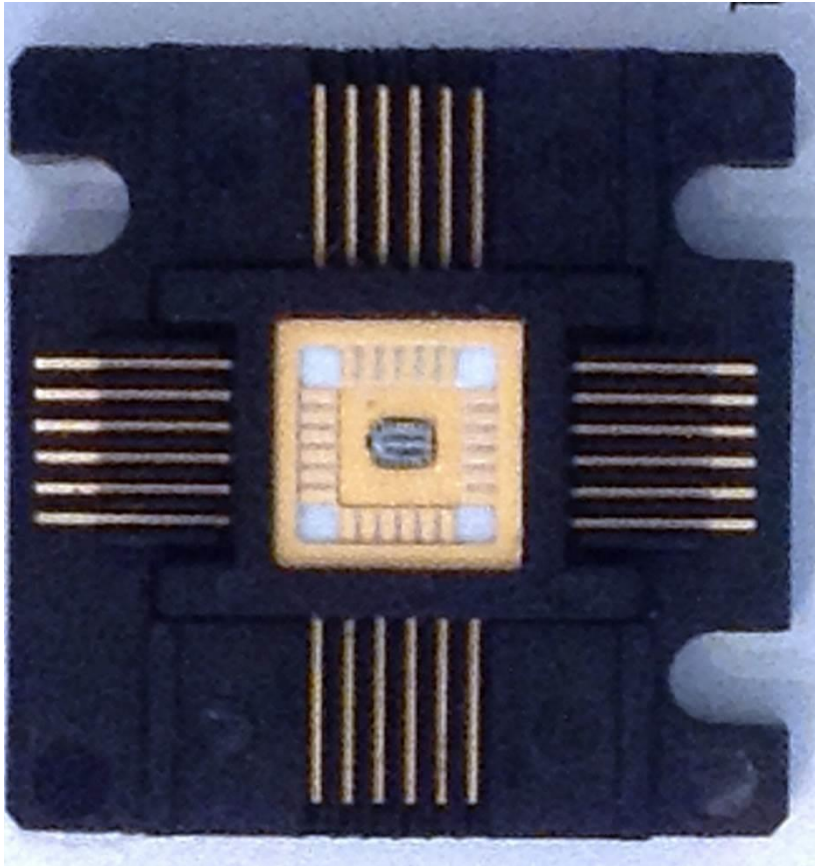
Die



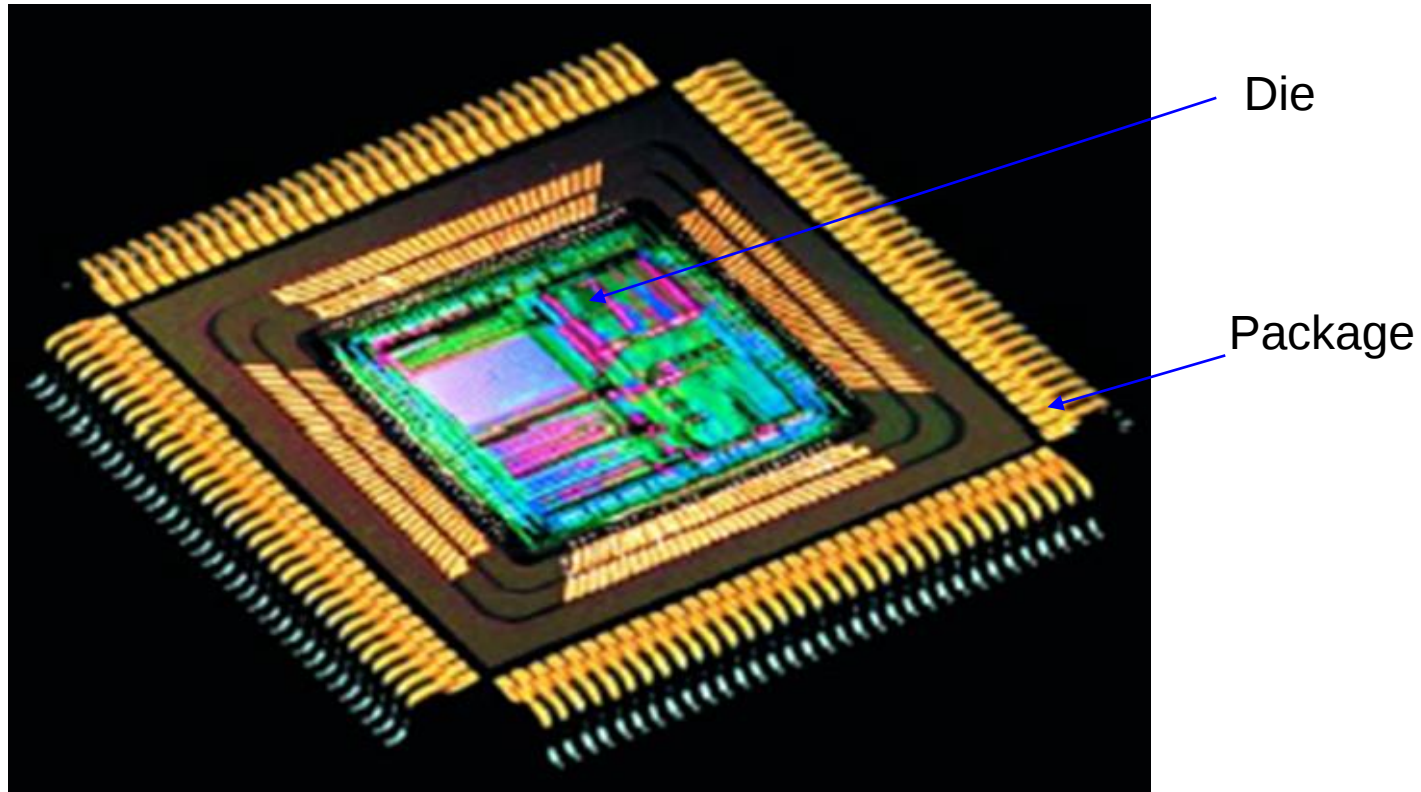
Top view of a die

Wafer

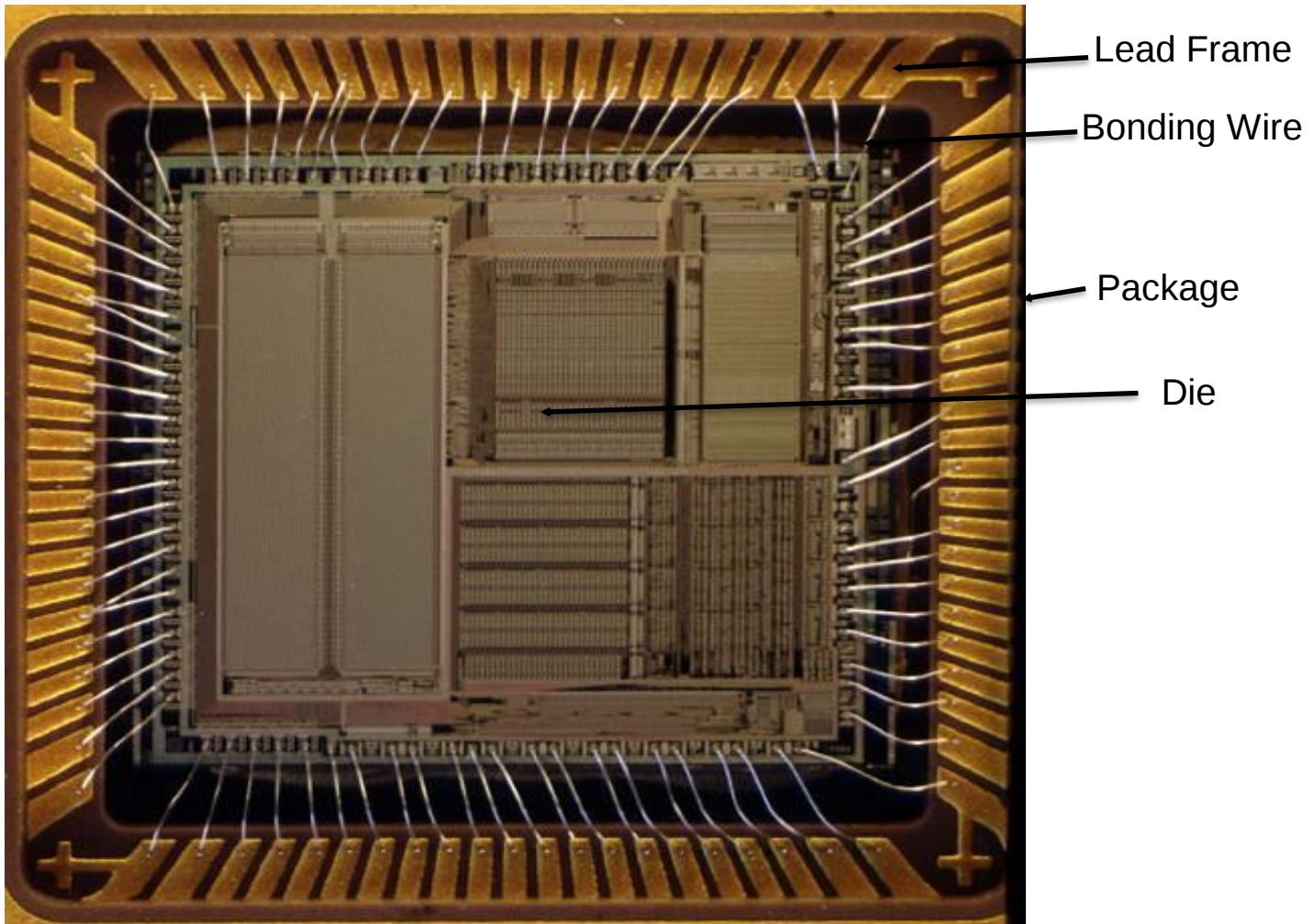
Chip Packages



Die and Package

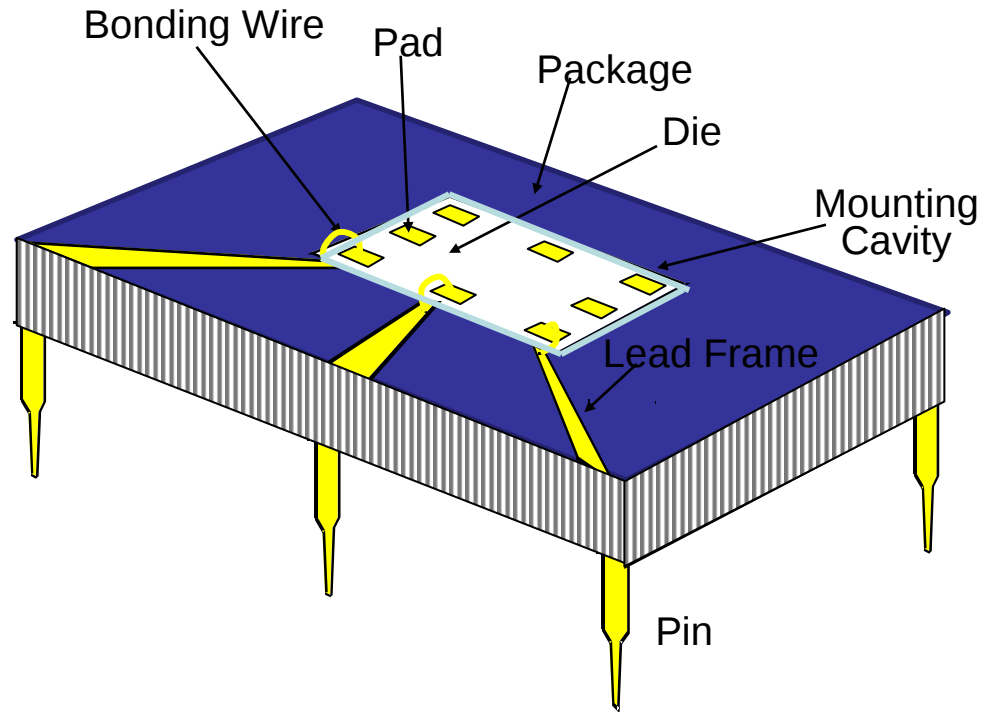


Packaging of Real IC



Chip Packaging

- Bonding wires connect the package to the chip.
- Pads are arranged in a frame around the chip.



Chip, PCB

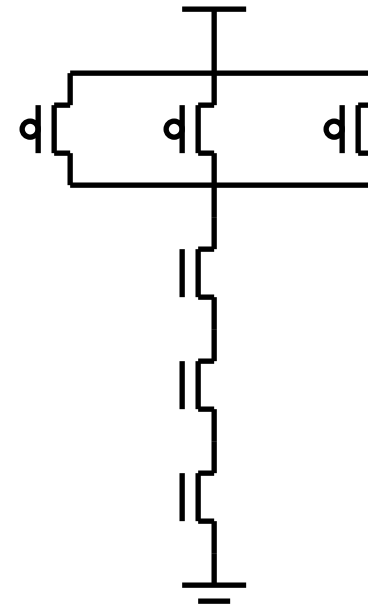
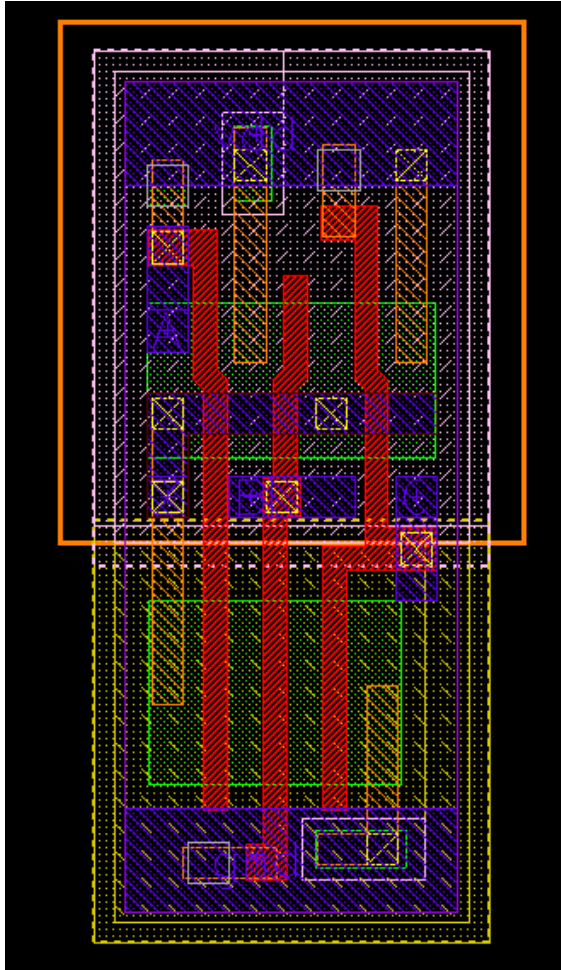
Chip



Chip

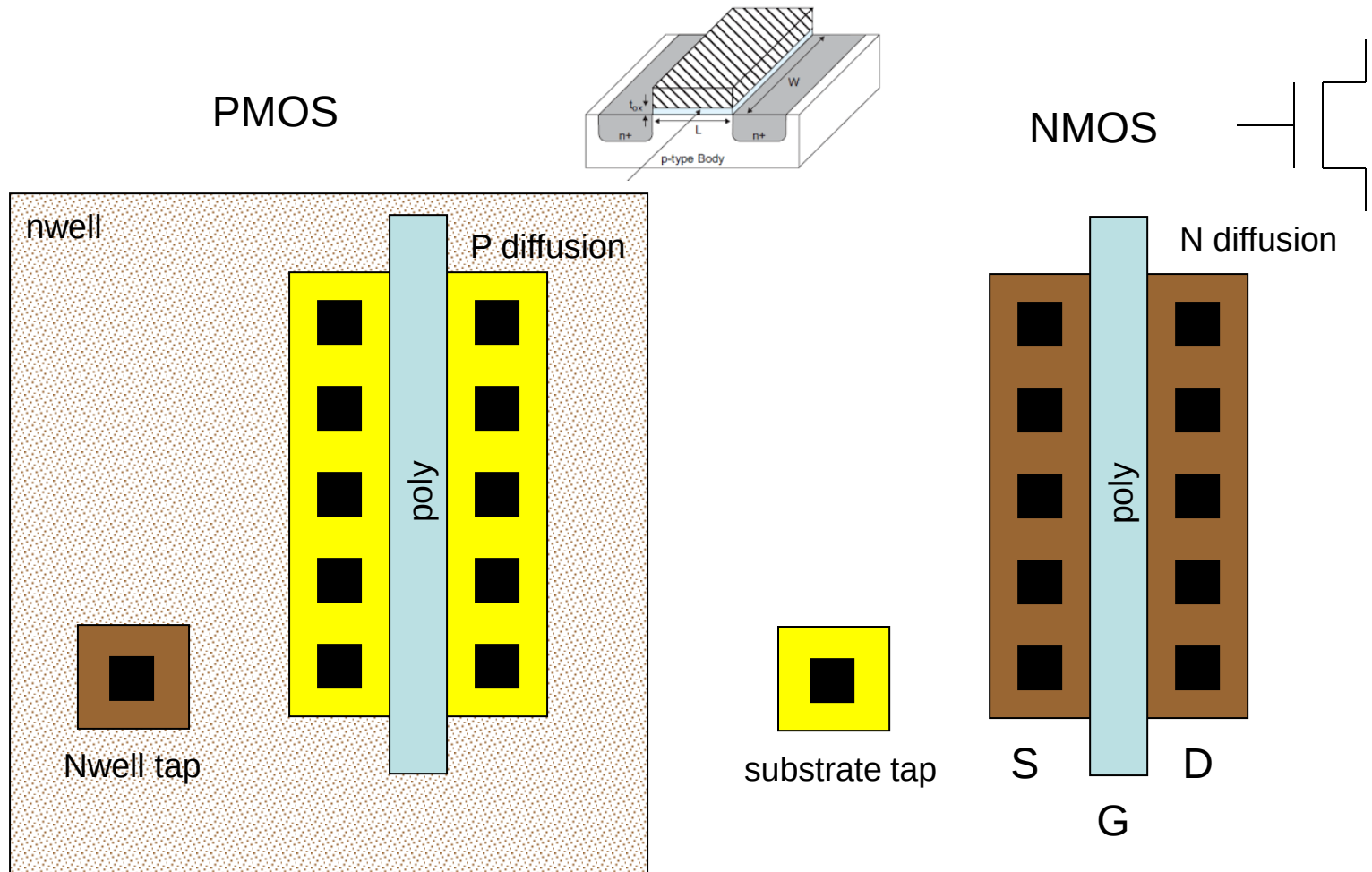
Printed circuit board (PCB)

Layout vs. Schematic

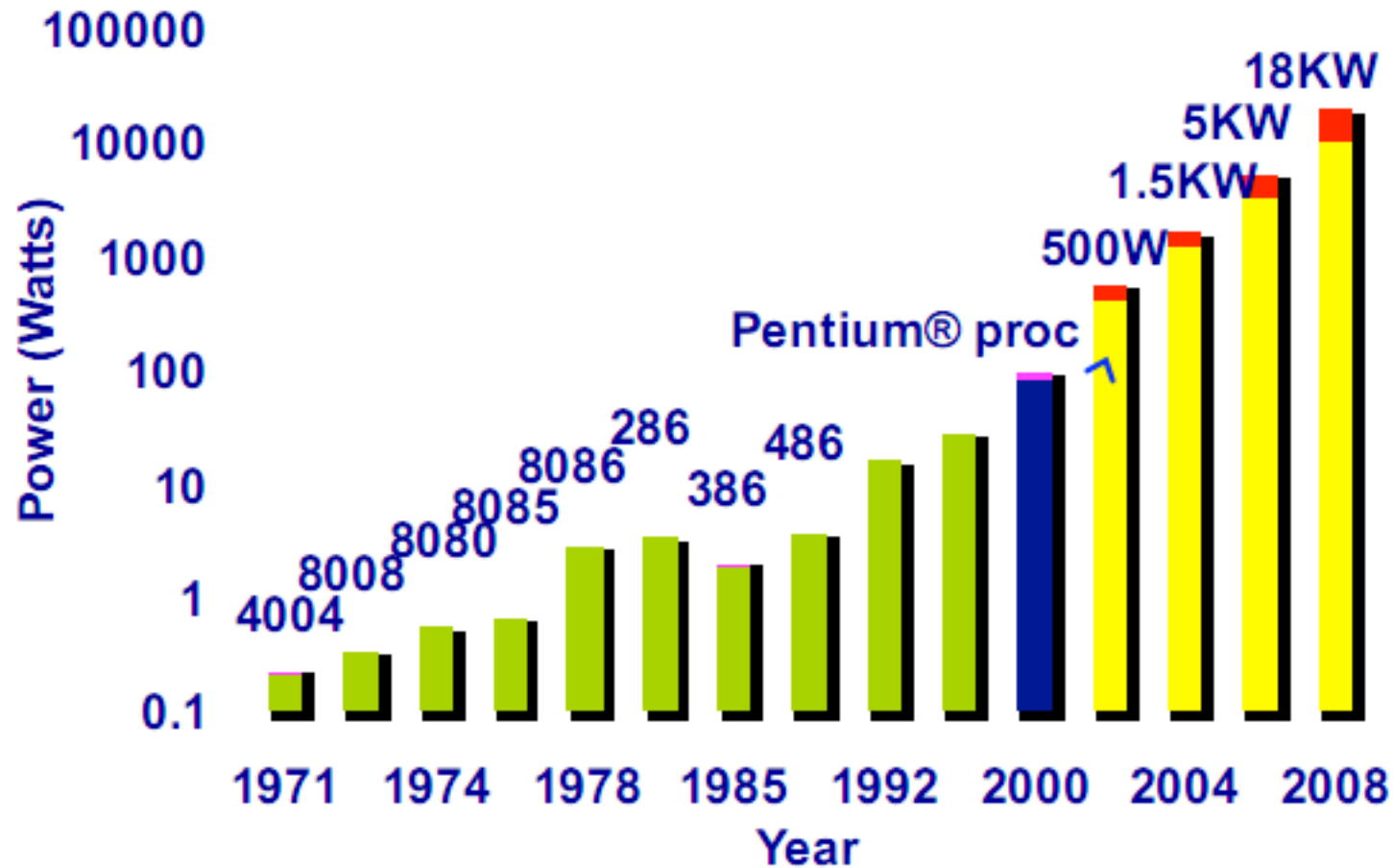


Layout

- Transistor defined as poly over diffusion



Power Dissipation Prediction (2000)



❑ Did this really happen?

Challenges

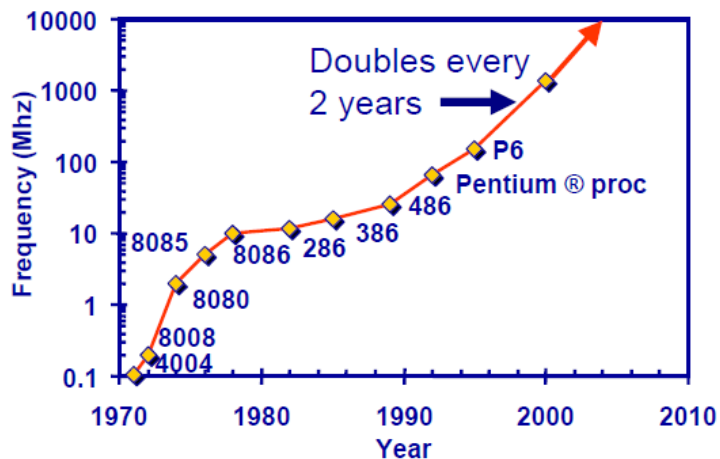
- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.



- Time-to-Market
- Millions of Gates
- High-Level Abstraction
- Reuse & IP: Portability
- Predictability
- etc.

Challenges

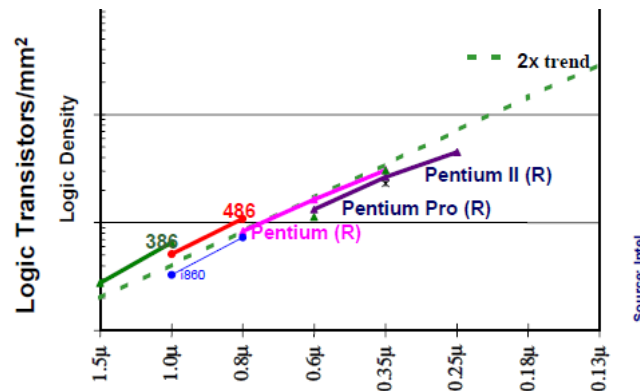
Frequency/speed



S. Borkar

Lead Microprocessors frequency doubles every 2 years

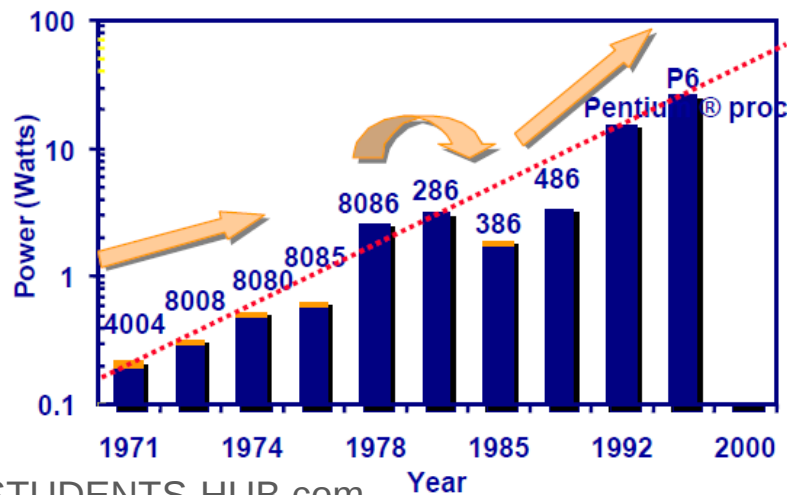
Moore's Law - Logic Density/Area



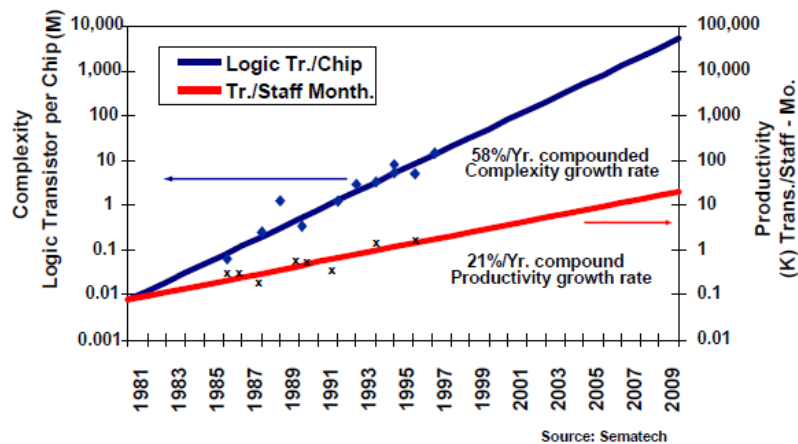
Source: Intel

Shrinks and compactions meet density goals
New micro-architectures drop density

Power



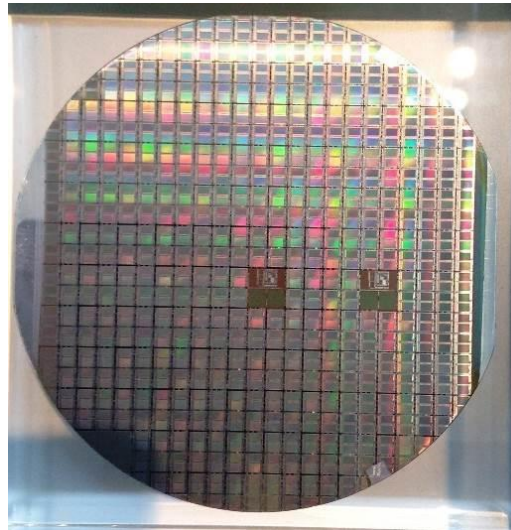
S. Borkar



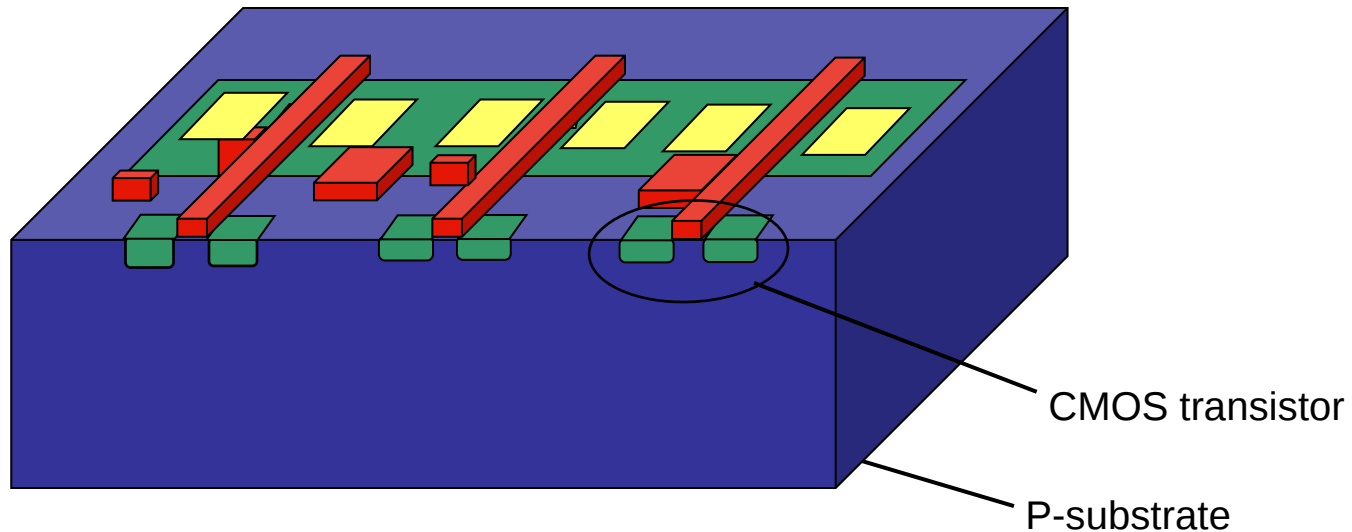
Source: Sematech

Complexity outpaces design productivity

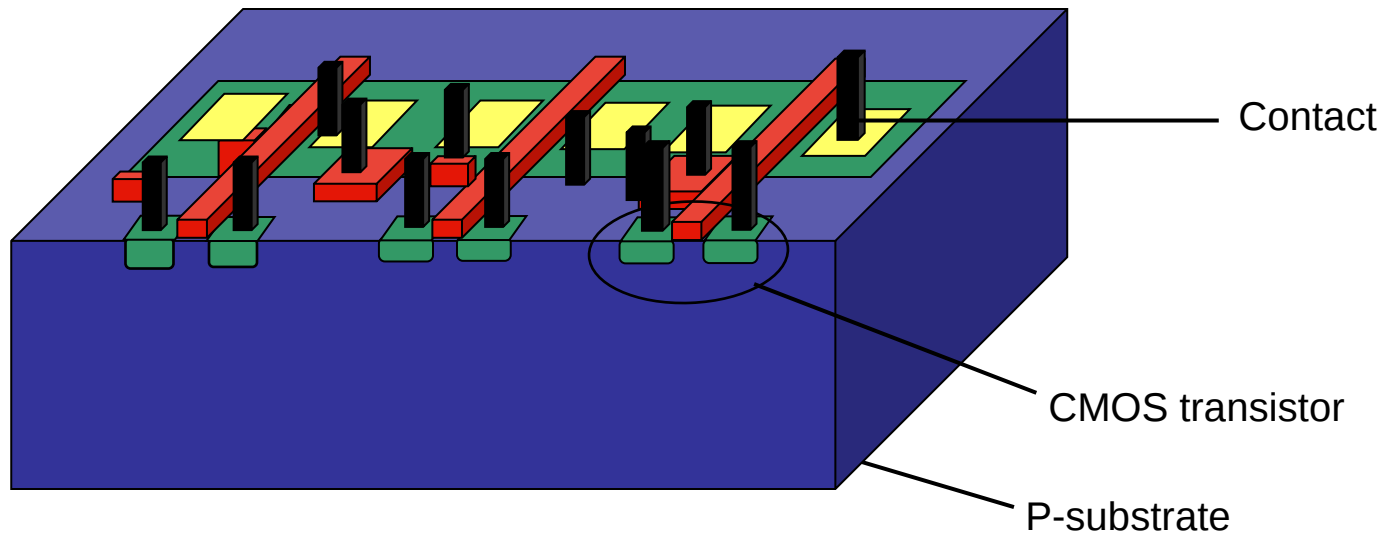
Producing a Wafer (2)



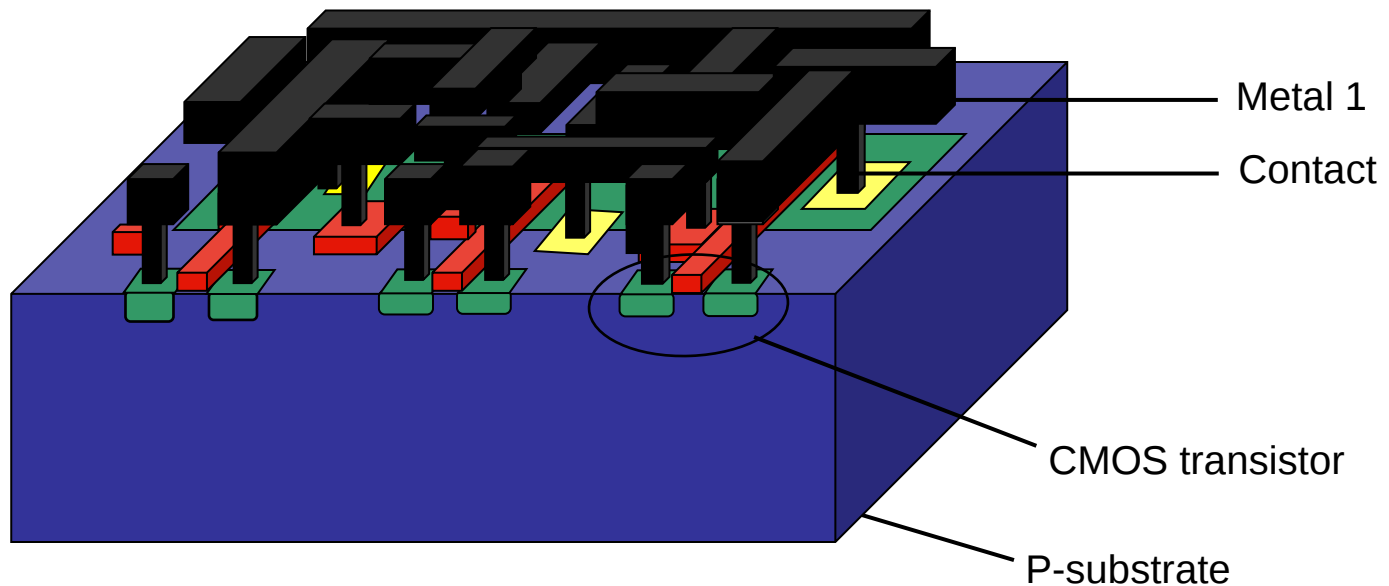
IC as a Multi Layer Structure



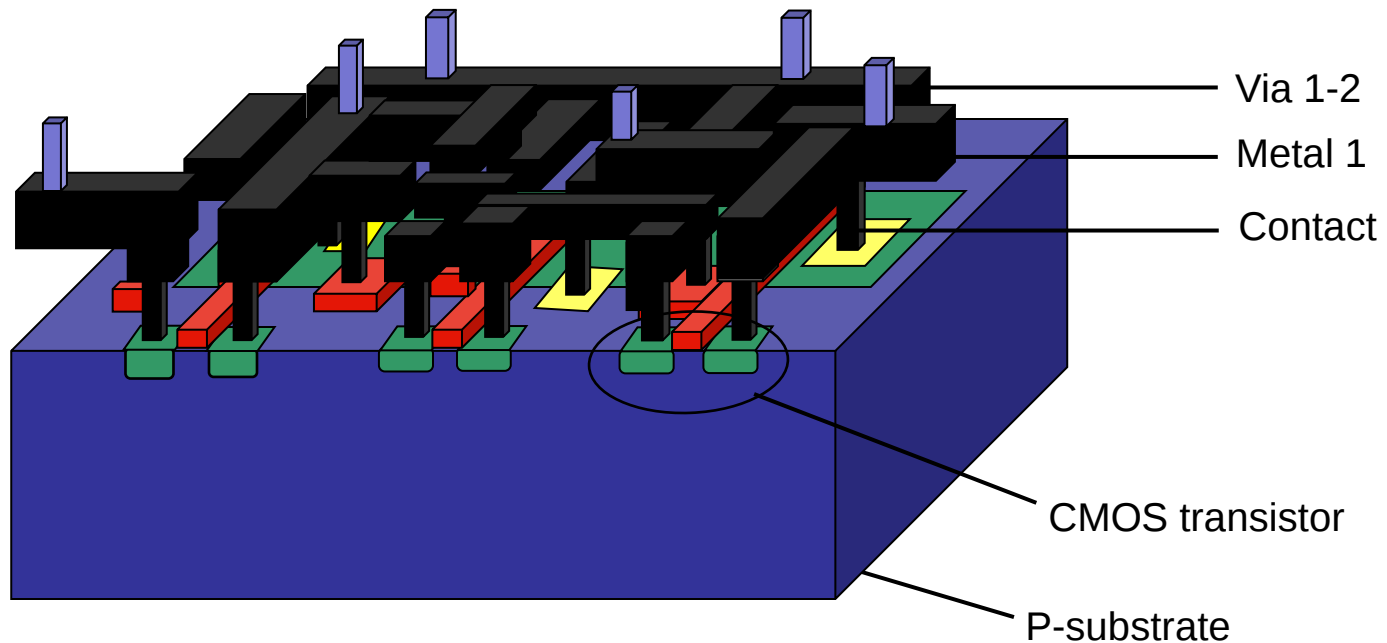
IC as a Multi Layer Structure (2)



IC as a Multi Layer Structure (3)



IC as a Multi Layer Structure (4)



IC as a Multi Layer Structure (5)

