L16 - part 2
8/8/2021

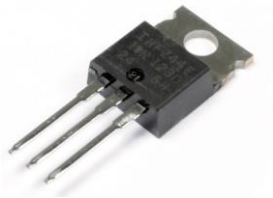
ENEE2360 Analog Electronics

T9:
Field Effect Transistor- FET

Instructor : Nasser Ismail

2

FET Vs conventional Transistors (BJT)

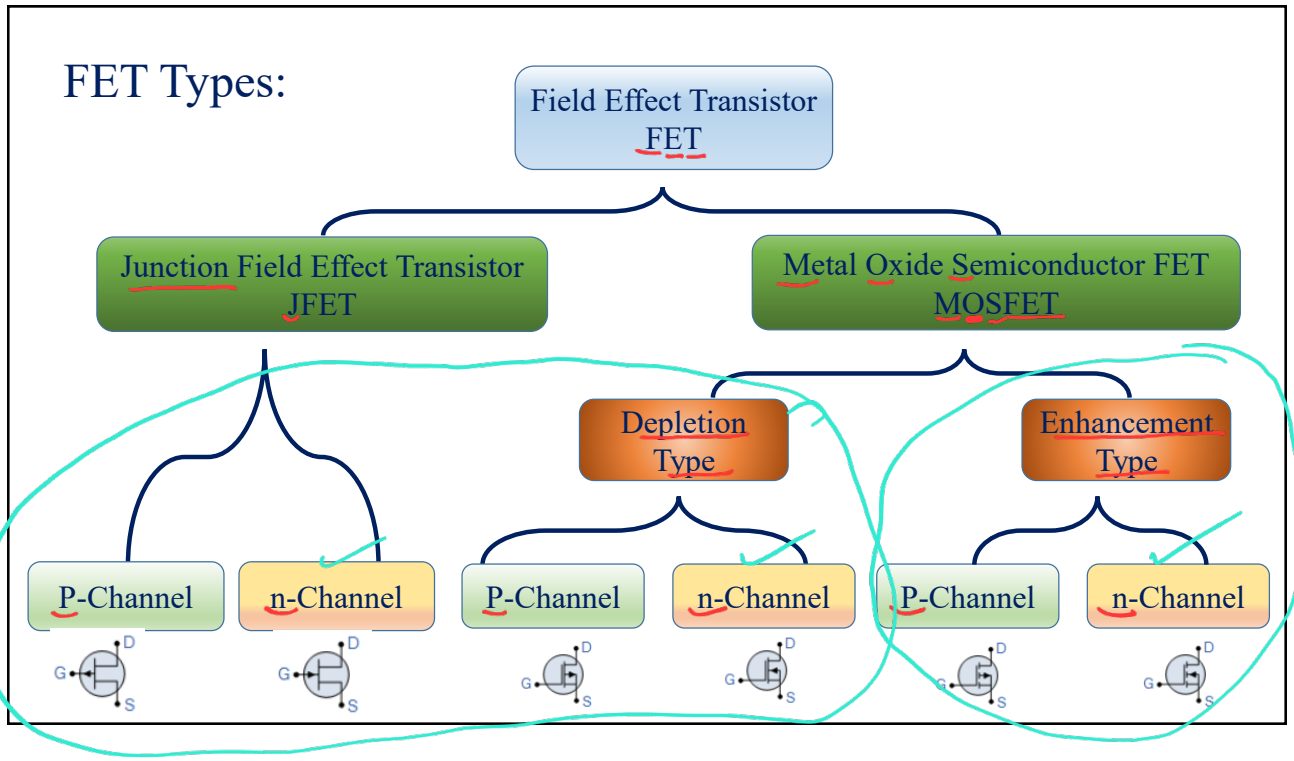


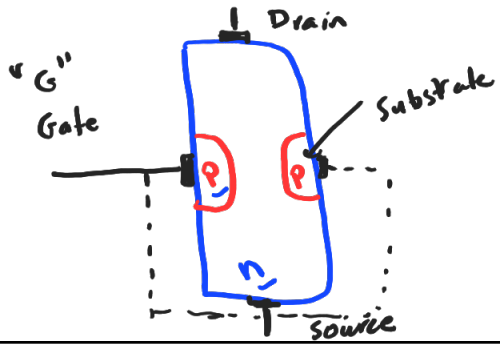
Advantages

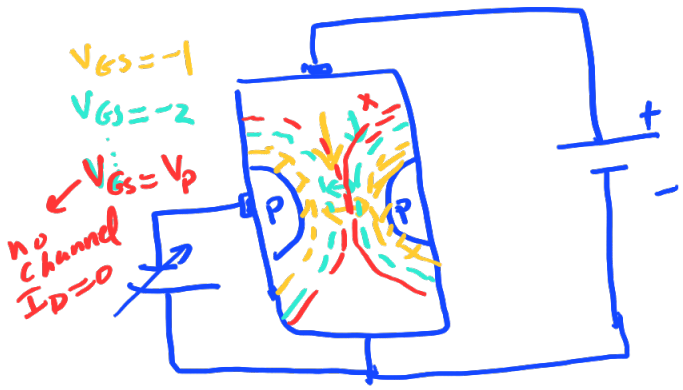
1- High input impedance ; ~100 M !
2- Fewer steps in manufacturing process.
3- More devices can be packaged into smaller area for integrated circuit **IC**

Disadvantages

1- Low values of voltage gain.
2- Poor high frequency performance.
3- Sensitivity to Electro-static Discharge (ESD) and special handling is required.



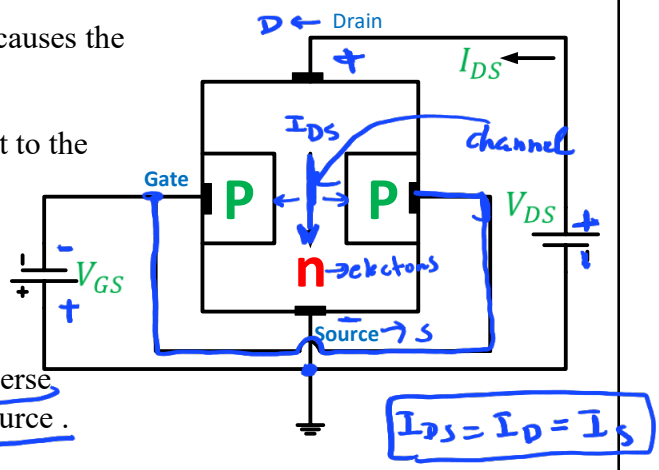




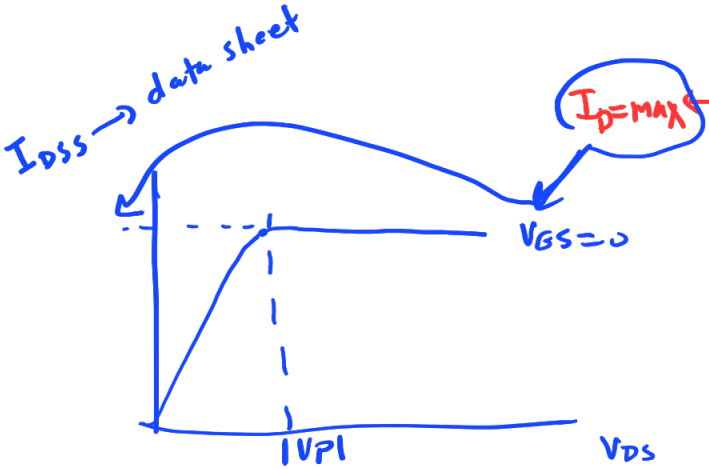
Junction Field Effect Transistor JFET

JFET construction:

n-channel JFET



- ✓ Reverse biasing the gate to source junctions causes the formation of the depletion region
- ✓ The drain has the proper polarity with respect to the source to establish the drain current I_{DS}
- ✓ The value of I_{DS} depends on the width of the channel.
- ✓ The width of the channel is controlled by reverse biasing the pn-junctions between gate and source .
- ✓ If the channel width increases I_{DS} increases .

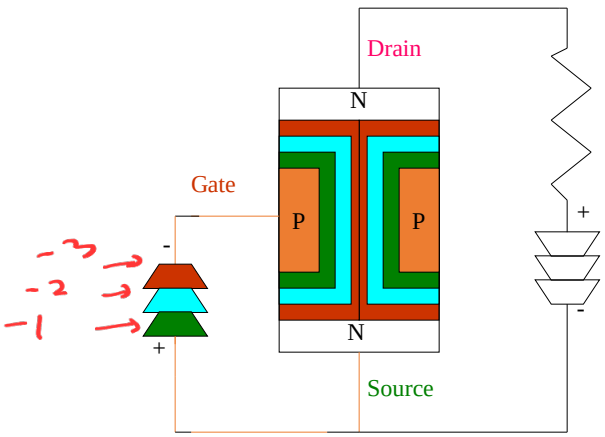


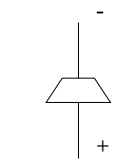
$0 \le V_{GS} \le V_P$

↓ maximum channel width

↓ min. channel width, X closed, $I_D=0$

Operation of a JFET

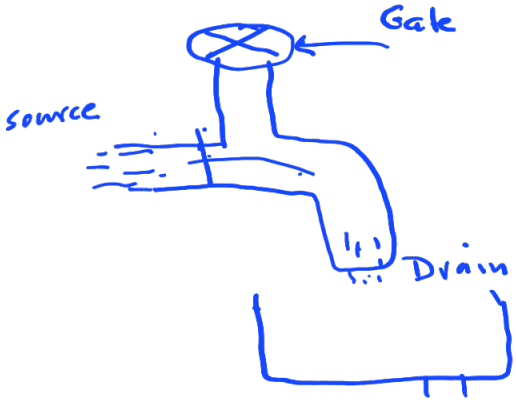




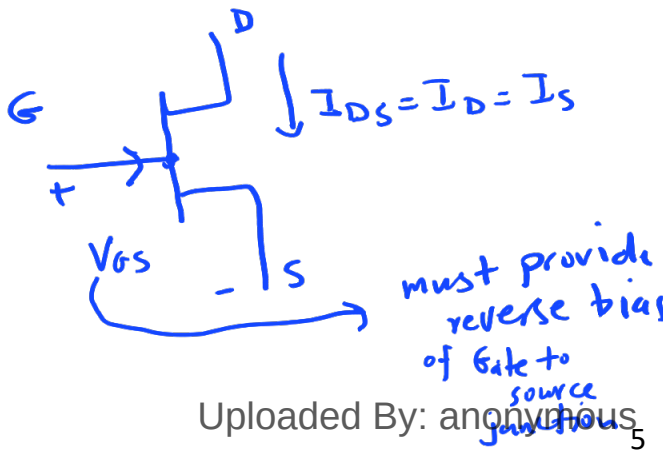
DC Voltage Source

animation

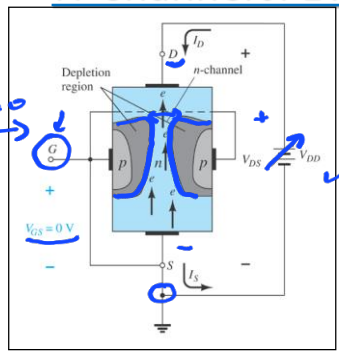
http://www.learnabout-electronics.org/fet_03.php

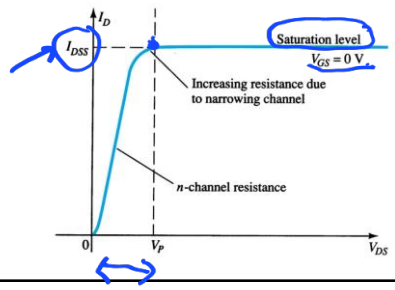


$I_D = f(V_{GS})$



N-Channel JFET Operation → characteristic



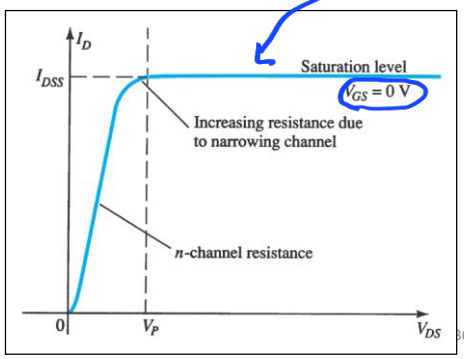


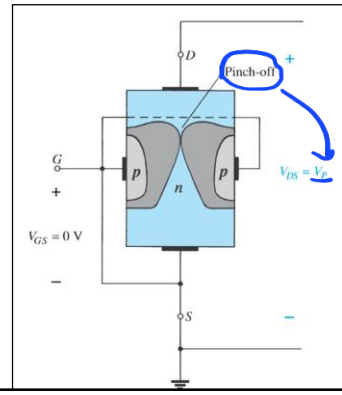
-When V_{DD} is applied , electrons are drawn to the drain terminal establishing drain current I_D
-Drain and source currents are equivalent (I_D=Is)
-I_D is limited by the resistance of the n-channel between the drain and source
-I_G=0 (due to the fact that the pn junction is reverse biased)
-As V_{DS} is increased , I_D will also increase according to ohms law

N-Channel JFET Operation

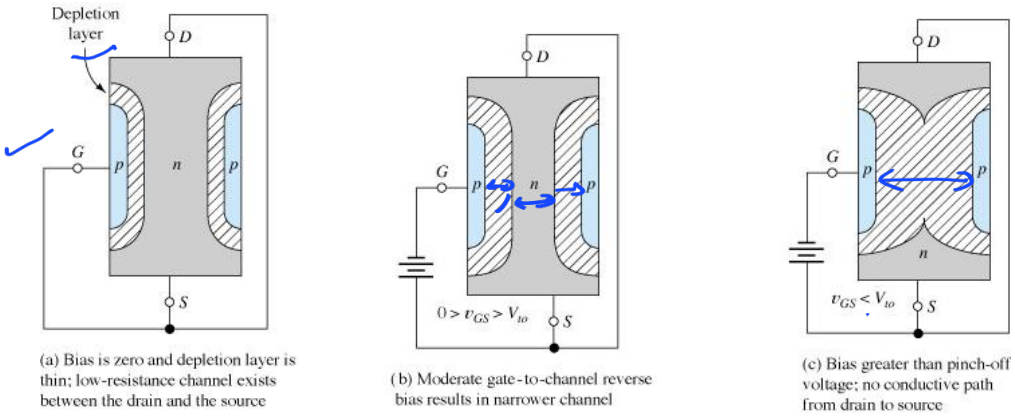
- As V_{DS} is increased towards a value V_P (pinch off voltage) , the depletion region is widened and channel width is reduced increasing resistance to I_D and the two depletion regions will appear as touching each other

-These two effects result in I_D being kept almost constant



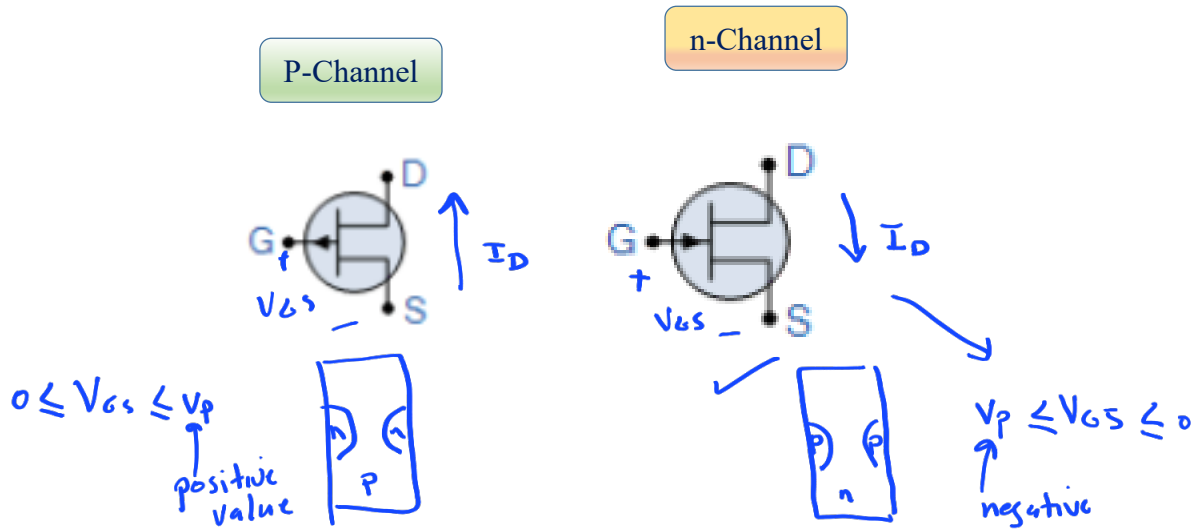


N-Channel JFET Operation

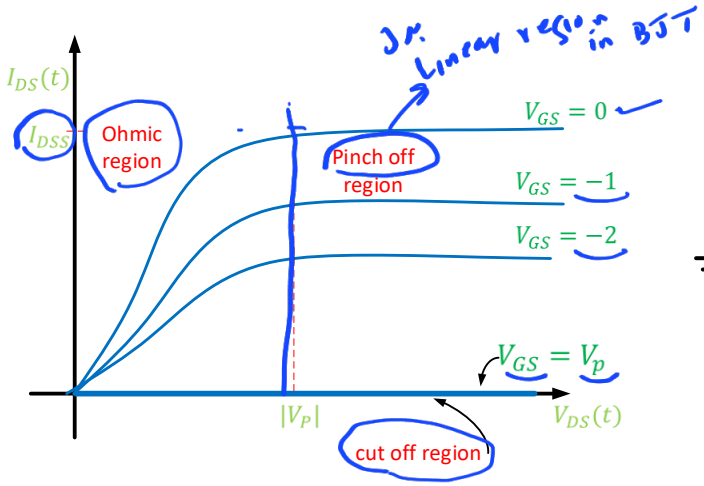


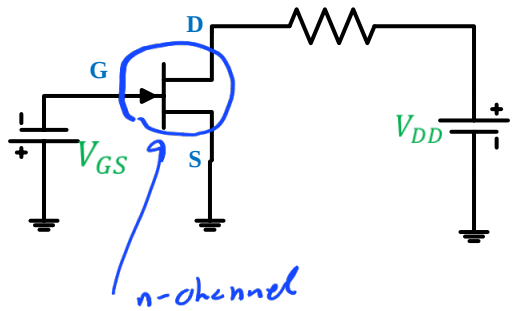
The nonconductive depletion region becomes thicker with increased reverse bias. (*Note:* The two gate regions of each FET are connected to each other.)

JFET Circuit Symbol:



JFET output characteristic:



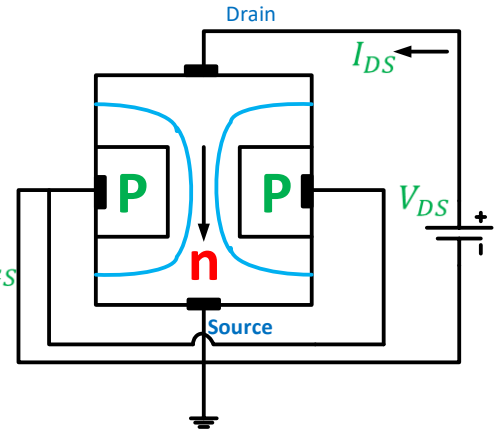


Pinch of voltage V_P:

For $V_{GS} = 0$,the value of V_{DS} at which I_{DS} becomes essentially constant
Is the absolute of the pinch of voltage $V_{DS} = |V_P|$

Some literature refer to Vp as $V_{GS(off)}$

$$V_P = \begin{cases} negative\ value\ for\ n\_channel \\ positive\ value\ for\ p\_channel \end{cases}$$



JFET Transfer characteristic curve:

$$I_D = I_{DS}(t) = I_{DSS}\left(1 - \frac{V_{GS}(t)}{V_P}\right)^2$$

data sheet

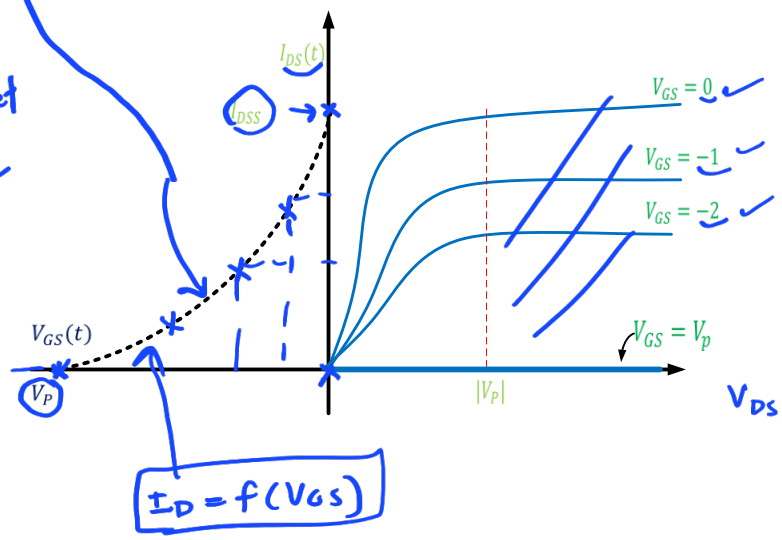
In pinch off region:

$$V_P < V_{GS} \leq 0$$

$$|V_{DS}| > |V_P| - |V_{GS}|$$

for both n & p channel

$I_D = I_{DS} = I_S$



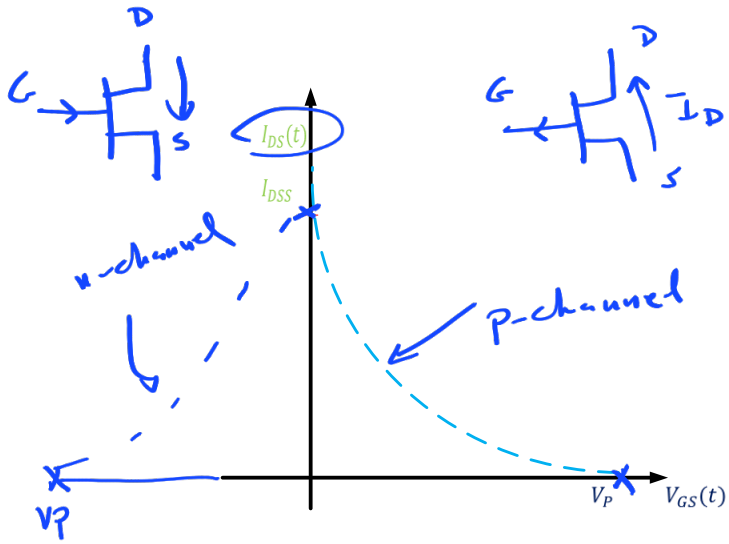
P-channel JFET

$$I_{DS}(t) = I_{DSS}\left(1 - \frac{V_{GS}(t)}{V_P}\right)^2$$

In pinch off region:

$$|V_{DS}| > |V_P| - |V_{GS}|$$

$$V_P > V_{GS} \geq 0$$



Summary: Pinch off voltage:

- ✓ The voltage that cusses the depletion region to touch and close the channel is called pinch off voltage
- ✓ For the n-channel JFET to be in the pinch off region:

$$V_P < V_{GS} \leq 0$$

$$|V_{DS}| > |V_P| - |V_{GS}|$$

- ✓ For the p-channel JFET to be in the pinch off region:

$$|V_{DS}| > |V_P| - |V_{GS}|$$

$$V_P > V_{GS} \geq 0$$

End of L16

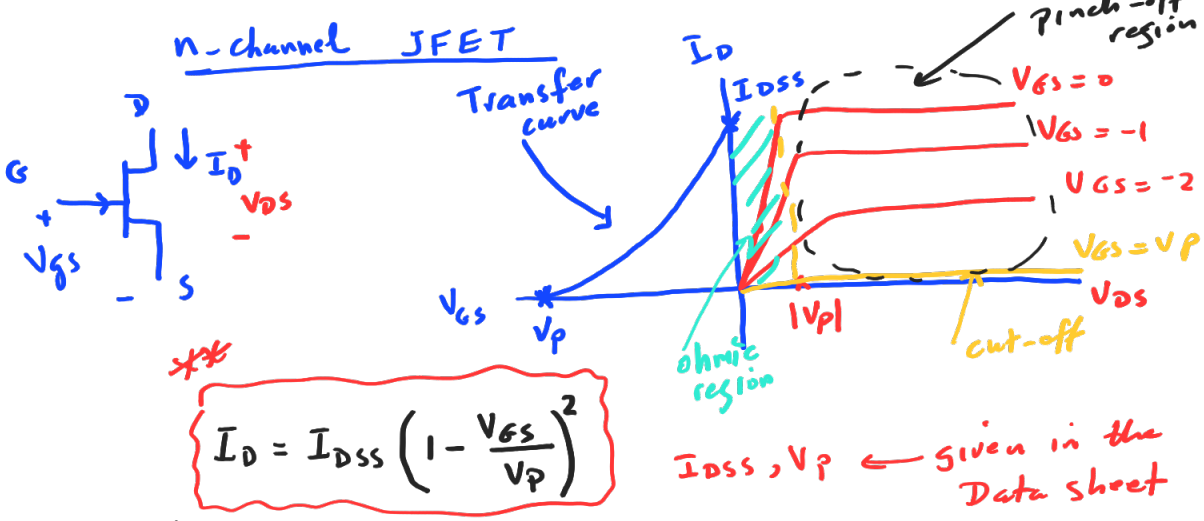
L17
10-8-2021

Common JFET Biasing Circuits

DC

- Fixed-Bias
- Self-Bias
- Voltage-Divider Bias

pinch-off mode ↓ active mode



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

I_{DSS}, V_P ← given in the Data sheet

Basic Current Relationships

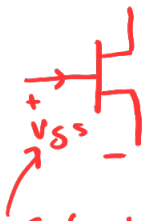
For all FETs:

$I_G \cong 0\ \text{A}$ *

$I_D = I_S = I_{DS}$

For JFETS

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



Gate-to-source junction is reverse biased

1)

Fixed-Bias Configuration

KVL 2

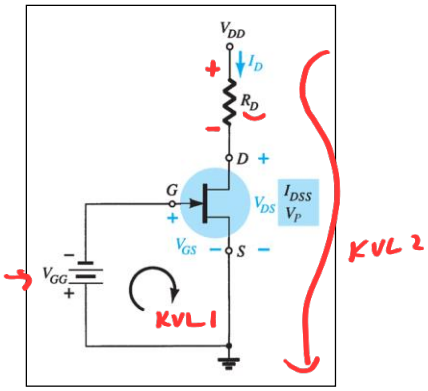
$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0\ \text{V}$$

$$\therefore V_D = V_{DS}$$

$$\therefore V_{GS} = -V_{GG}$$

KVL 1



Find V_{GS} & I_D ?

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$I_G = 0 \rightarrow$ KVL1

$1.5 + V_{GS} = 0 \Rightarrow V_{GS} = -1.5\ V$

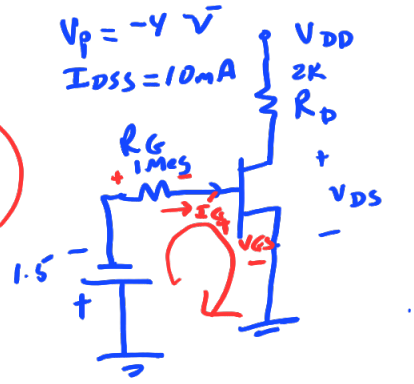
$I_D = 10mA\left(1 - \frac{-1.5}{-4}\right)^2$

$= 3.9\ mA$

KVL2

$16 = I_D R_D + V_{DS} \rightarrow V_{DS} = 16 - 3.9mA \times 2K$

$= 8.2\ V$



Example

$V_{GS} = V_G - V_S = -1.5 - 0 = -1.5\ \text{V}$

Assuming JFET is in pinch off region

1) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$= 10\ \text{mA}\left(1 - \frac{-1.5}{-4}\right)^2$

$= 3.9\ \text{mA}$

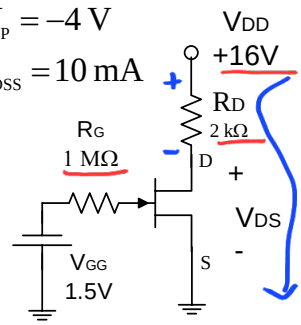
2) $V_{DS} = V_{DD} - I_D R_D$

$= 16 - ((2\text{k})(3.9\ \text{mA}))$

$= 8.2\ \text{V}$

$V_P = -4\ \text{V}$

$I_{DSS} = 10\ \text{mA}$



3) check for $|V_{DS}| > |V_P| - |V_{GS}|$?

to make sure JFET is in pinch-off region

$|8.2| > |-4| - |-1.5|$

assumption is true

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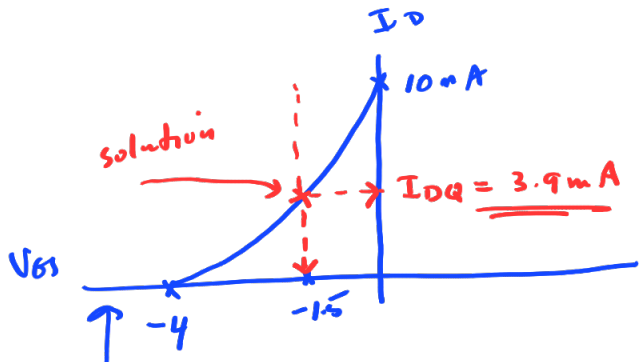
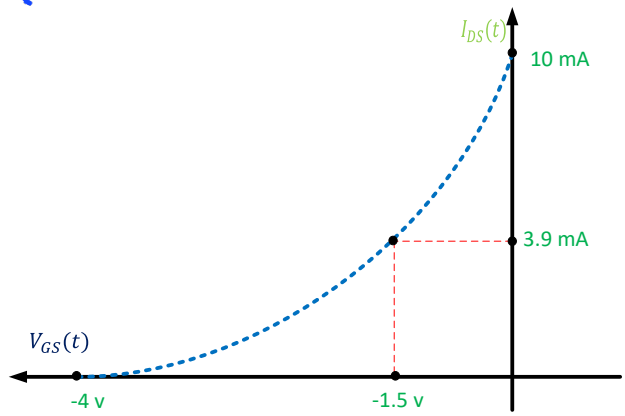


Graphical method:

- $I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
- V_{GS} = **-1.5 v** **Fixed**



$V_S = I_D R_S$

$V_D = V_{DD} - I_D R_D$

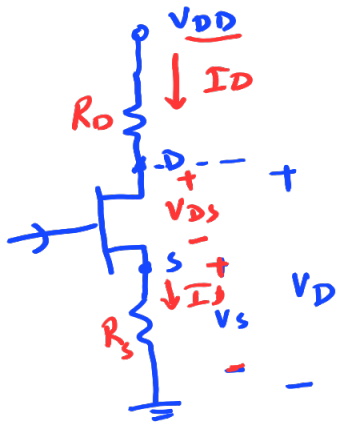
OR

$V_{DS} = V_D - V_S$

$V_D = V_{DS} + V_S$

never

$V_D = I_D R_D \neq V_S$



$V_S = I_D \cdot R_S$

Self-Bias Configuration

KVL 1

$$V_{GS} = V_G - V_S = 0 - V_S = -V_S$$

$$V_S = I_D R_S$$

f(ID) ← $$V_{GS} = -I_D R_S \quad (1)$$

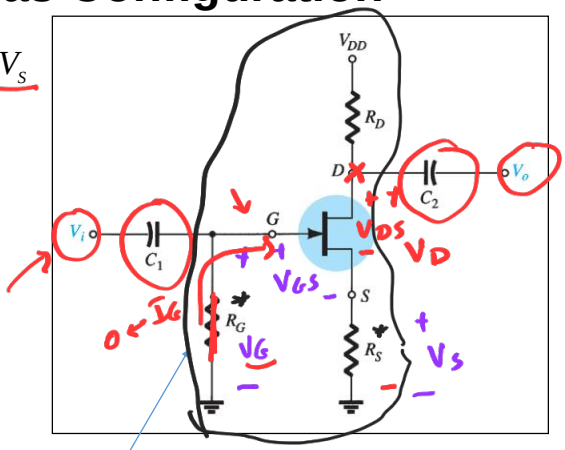
KVL 2

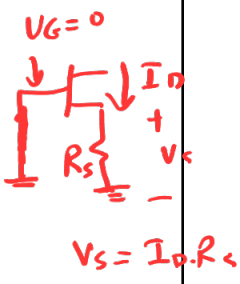
$$V_D = V_{DD} - I_D R_D$$

$$V_{DS} = V_D - V_S$$

$$= V_{DD} - I_D R_D - I_D R_S$$

$$= V_{DD} - I_D (R_S + R_D)$$





RG is important to isolate the ac signal from ground in amplifier circuits

Find V_{GS}, I_D, V_{DS} ?

Solution

$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$

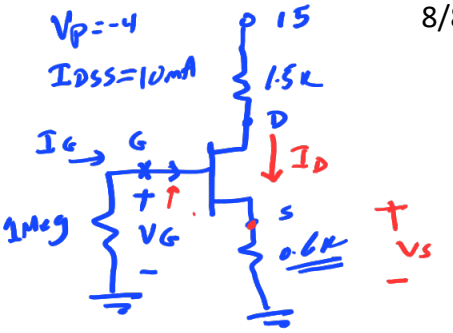
$V_G = 0 \quad (I_G = 0)$

$V_S = I_D R_S$

assume pinch-off region

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$I_D = 10\,mA\left(1 - \frac{-I_D R_S}{-4}\right)^2$ ← quadratic equation



Example

$V_P = -4\,V$

$I_{DSS} = 10\,mA$

$V_{GS} = V_G - V_S = 0 - V_S = -V_S$

$V_S = I_D R_S = 600\,I_D$

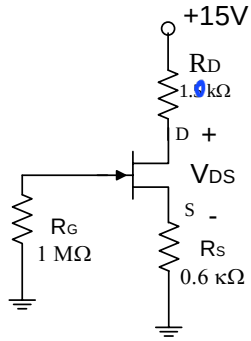
$V_{GS} = -600 I_D$

$R_S = 0.6\,k$

1) $I_D = 10\,mA\left(1 - \frac{-600 I_D}{-4}\right)^2$ ← $X = I_D$

$ax^2 + bx + c = 0$

$x_{1,2} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$



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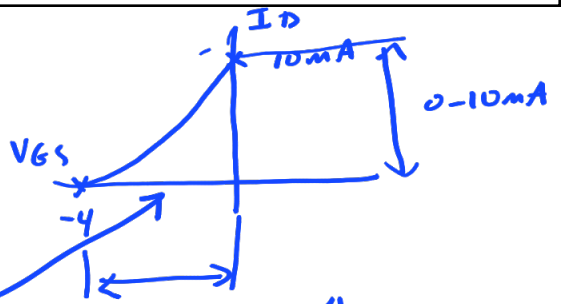
X $I_{D1} = 14.7\,mA$ X > I_{DSS}

$I_{D2} = 3\,mA$

$V_{GS} = -I_D \times R_S$

$= -3\,mA \times 0.6\,k\Omega$

$V_{GS} = -1.8\,V$



OR

$I_D = 3\,mA, V_{GS} = -1.8\,V$

Example-continued

solving for I_D :

$I_{D1} = 14.77\ \text{mA} > I_{DSS}$ and this solution is not possible

$I_{D2} = 3\ \text{mA}$ ⇐ this is the correct solution

2) $\therefore V_{GS} = -600 I_D = -600 \text{ x } 3\text{mA} = -1.8\text{V}$

$V_D = V_{DD} - I_D R_D$

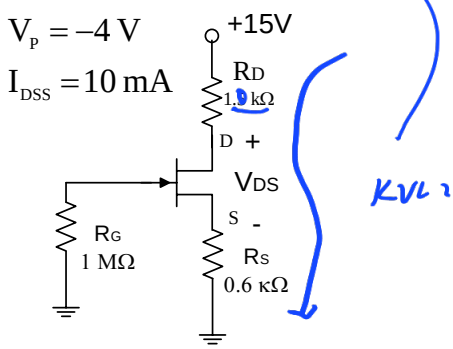
$V_{DS} = V_{DD} - I_D(R_S + R_D)$

$= 15 - 3\text{mA}\,(1\text{k} + 0.6\text{k}) = 10.2\ \text{V}$

3) check for $|V_{DS}| > |V_P| - |V_{GS}|$?

$|10.2| > |-4| - |-1.8|$

⇒ assumption is true



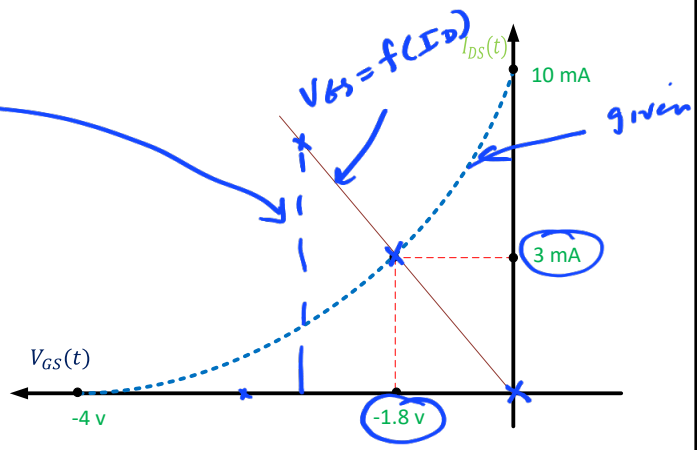
Graphical method

- $I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ → curve

V_{GS} = -(0.6K) I_{DS}

when V_{GS}=0 → I_{DS}= 0mA

when V_{GS}= -3v → I_{DS}= 5mA

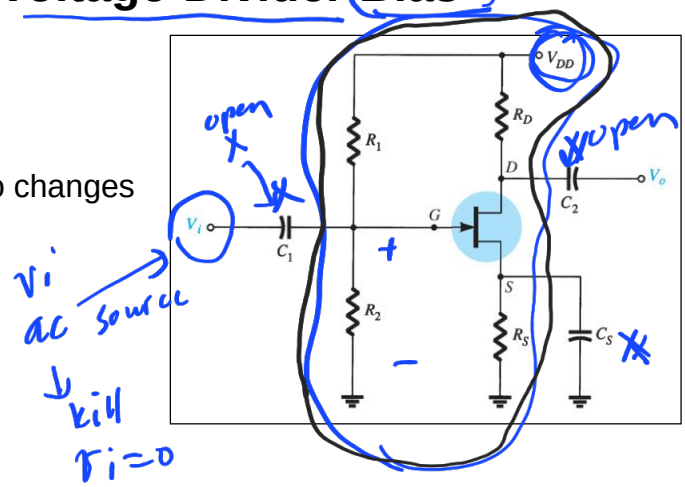


L18
11-8-2021
sec 1

Voltage-Divider Bias → DC

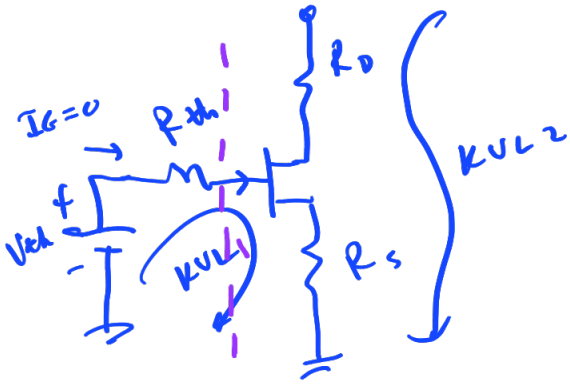
$I_G = 0$ A

I_D responds to changes in V_{GS}.



open
open
+
−
Vi ac source
↓ kill
$r_i = 0$

dc
caps → open



Voltage-Divider Bias Calculations

$I_G = 0$ A

V_G is equal to the voltage across divider resistor R_2:

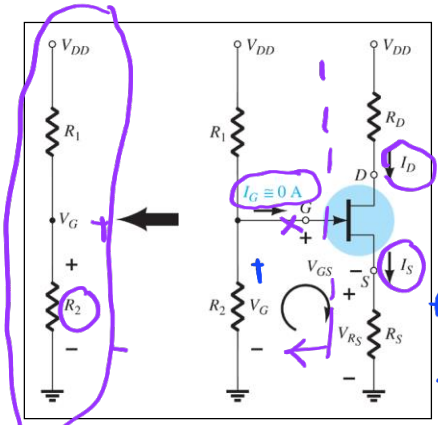
$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = V_{th}$$

$$V_S = I_D R_S$$

Using Kirchhoff's Law:

$$V_{GS} = V_G - I_D R_S$$

$$V_{GS} = \frac{R_2 V_{DD}}{R_1 + R_2} - I_D R_S$$



$I_D = I_S$

$V_S = I_D R_S$

The Q-point is established by plotting a line that intersects the transfer curve.

(1) ...

$$V_{GS} = V_G - V_S = V_G - I_D R_S = \frac{R_2}{R_1 + R_2} V_{DD} - I_D R_S$$

const

(2) ...

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Sub (1) in (2)

$$I_D = I_{DSS}\left(1 - \frac{V_G - I_D R_S}{V_P}\right)^2$$ ← معادلة تربيعية

I_{D1} → ? → ? only one correct solution
I_{D2} →

V_{GS}

Example

V_S must be more positive than V_G to keep the gate – source junction reverse biased

1) V_P & I_{DSS} are not given
2) $V_D = 7$ V

$$V_S = I_D R_S$$

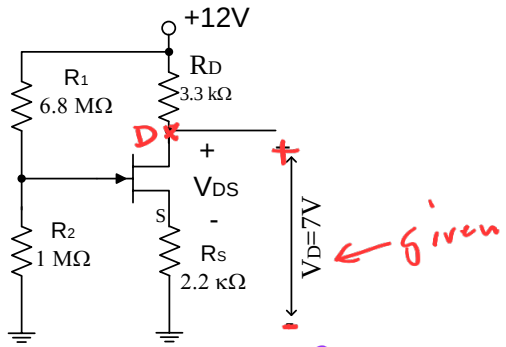
$$V_{GS} = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{GS} = \frac{R_2 V_{DD}}{R_1 + R_2} - I_D R_S$$

$$V_D = V_{DD} - I_D R_D = 7\ \text{V}$$

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12 - 7}{3300} = 1.52\ \text{mA}$$



← given

$V_D = V_{DD} - I_D R_D$?

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$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$? ?

→ if V_{DS} was known instead of V_D?

$V_{DS} = V_{DD} - I_D R_D - I_D R_S$ → $I_D = \frac{V_{DD} - V_{DS}}{R_D + R_S}$

→ if V_S was known

$V_S = I_D R_S$ → $I_D = \frac{V_S}{R_S}$

Example

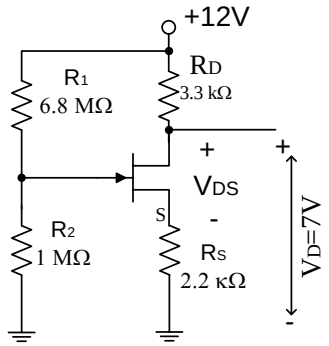
$$V_S = I_D R_S = (1.52\text{mA})\,(2.2\text{k}\Omega) = 3.34\text{ V}$$

$$V_G = \frac{1\text{ M}}{1\text{ M} + 6\text{ M}} 15 = 1.54\text{ V}$$

$$V_{GS} = 1.54 - 3.34 = -1.8\text{ V} < 0 \Leftarrow \text{OK}$$

also

$$I_D = \frac{V_S}{R_S} = \frac{3.34}{2200} = 1.52\text{ mA}$$



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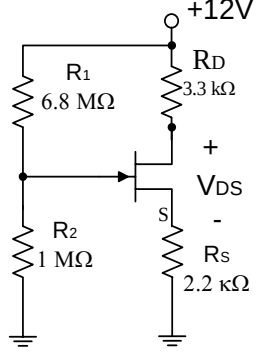
Example-V_D unknown

For the same example, if V_D was not given, then we use the square law rule $I_D = f(V_{GS})$ to find I_D and V_{GS} by substituting the expression for $V_{GS} = \frac{R_2 V_{DD}}{R_1 + R_2} - I_D R_S$ in it and solving for I_D

$$V_{GS} = 1.54 - I_D R_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{1.54 - I_D R_S}{V_P}\right)^2$$



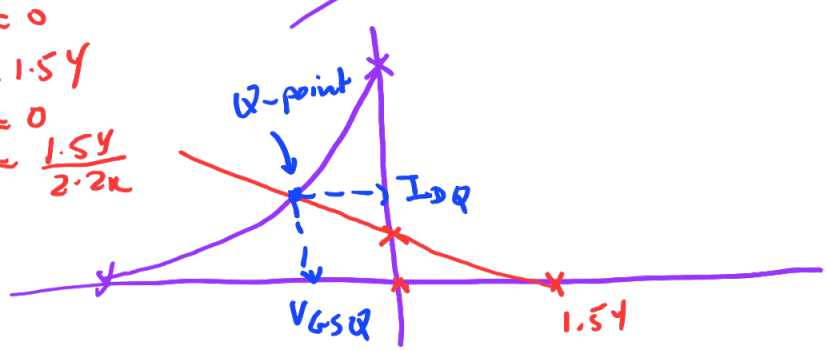
30

HW
assume
$V_P = -4$
$I_{DSS} = 10$ mA
solve
Do not submit

$V_{GS} = 1.54 - I_D R_S$ (2.2 kΩ)

for $I_D = 0$, $V_{GS} = 1.54$

for $V_{GS} = 0$, $I_D = \frac{1.54}{2.2k}$



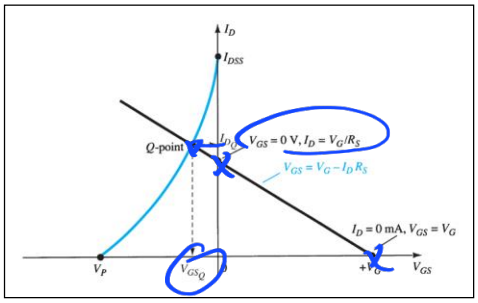
Voltage-Divider Q-Point

Plot the line that is defined by these two points:

$V_{GS} = V_G$, $I_D = 0$ A

$V_{GS} = 0$ V, $I_D = V_G / R_S$

Plot the transfer curve by plotting I_{DSS}, V_P and the calculated values of I_D

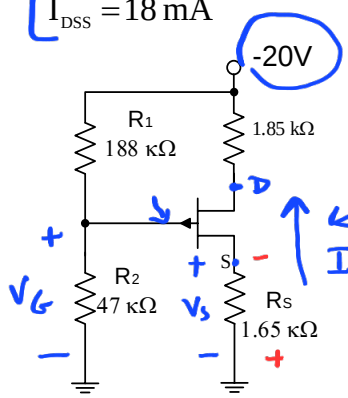


The Q-point is located where the line intersects the transfer curve

Example p-channel

$V_P = 5\,V$ ← positive → P-channel JFET

$I_{DSS} = 18\,mA$



$$V_{GS} = \frac{R_2 \times (-20)}{R_1 + R_2} + I_D R$$

$$V_{GS} = -4 + I_D R_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-4 + I_D R_S}{V_P}\right)^2$$

معادلة من الدرجة الثانية

$V_S = -I_D R_S$

$V_G = \frac{R_2}{R_1 + R_2} \times (-20)$

$$I_D = 18\,\text{mA}\left(1 - \frac{-4 + 1650 I_D}{5}\right)^2$$

- Solving the quadratic equation and finding its roots yields:

$I_{D1} = 4.7\,\text{mA}$ $\qquad$ $I_{D2} = 7.4\,\text{mA}$

both values of $I_D < I_{DSS}$ and are possible solutions

p-channel

$0 \le V_{GS} \le V_p$

$\Rightarrow$ so we verify value of V_{GS} :

$V_{GS1} = -4 + (4.7\text{mA})(1.65\,\text{k}\Omega) = 3.75\,\text{V} < V_p \angle$ correct solution

$V_{GS2} = -4 + (7.4\text{mA})(1.65\,\text{k}\Omega) = 8.21\,\text{V} > V_p \times$ wrong solution

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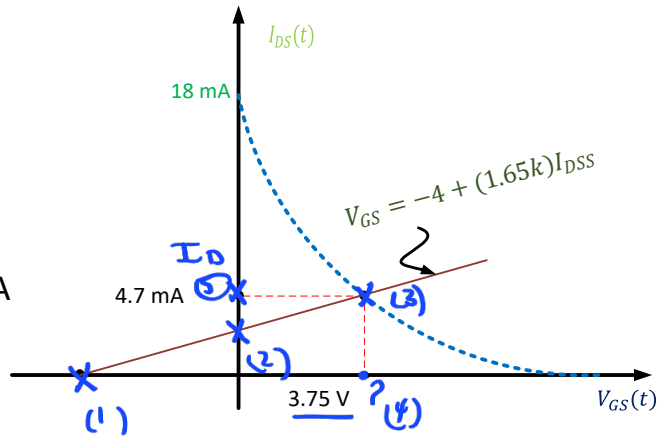
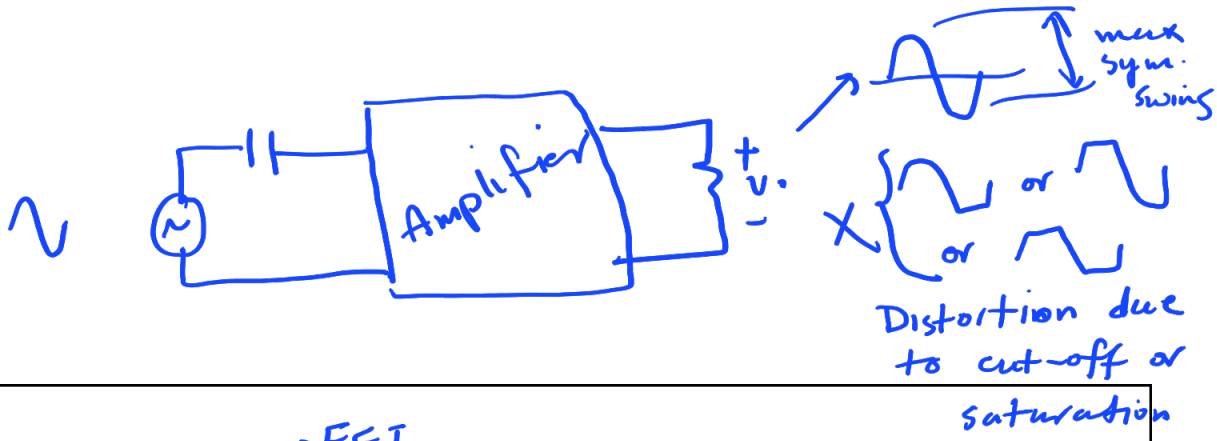
Graphical method

- $I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
- V_{GS} = -4 + (1.65K) I_{DS}

when V_{GS} = -4v $\rightarrow$ I_{DS} = 0mA

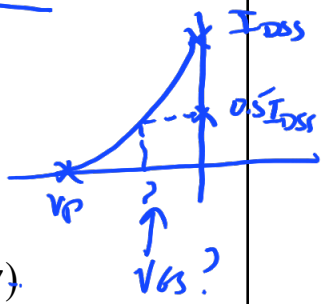
when V_{GS} = 0v $\rightarrow$ I_{DS} = 4.7 mA





Midpoint Bias → FET
For maximum Symmetrical Swing

- Place Q-point in the middle point of the transfer characteristic to allow for maximum swing between I_{DSS} and zero



1) let $I_D = 0.5I_{DSS}$

$$0.5I_{DSS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$0.5 = \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\sqrt{\frac{1}{2}} = 1 - \frac{V_{GS}}{V_P}$$

$$\frac{V_{GS}}{V_P} = 1 - \sqrt{\frac{1}{2}}$$

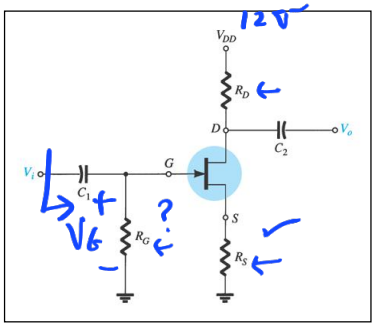
$$V_{GS} = V_P(1 - 0.707)$$

$$= V_P(0.2928)$$

$$\therefore V_{GS} \cong \frac{V_P}{3.41}$$

2) let $V_D = 0.5V_{DD}$

Example



$V_P = Vgs(off) = -3\,V$

$I_{DSS} = 12\,mA$

Choose R_D and Rs for mid point bias

$I_D = 0.5 I_{DSS} = 6\,mA$

$V_D = 0.5 V_{DD} = 6\,V$

$$V_{GS} = \frac{V_{GS(off)}}{3.4} = \frac{-3}{3.4} = -0.882\,V$$

$$Rs = \frac{Vs}{I_D} = \frac{0.882}{6\,mA} = 147\Omega$$

$V_G = 0$

$\rightarrow V_S = V_G - V_{GS}$

$= 0 - (-0.882)$

$= 0.882$

$= I_D R_S$

$$V_{DD} - I_D R_D - V_D = 0$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = 1k\Omega$$

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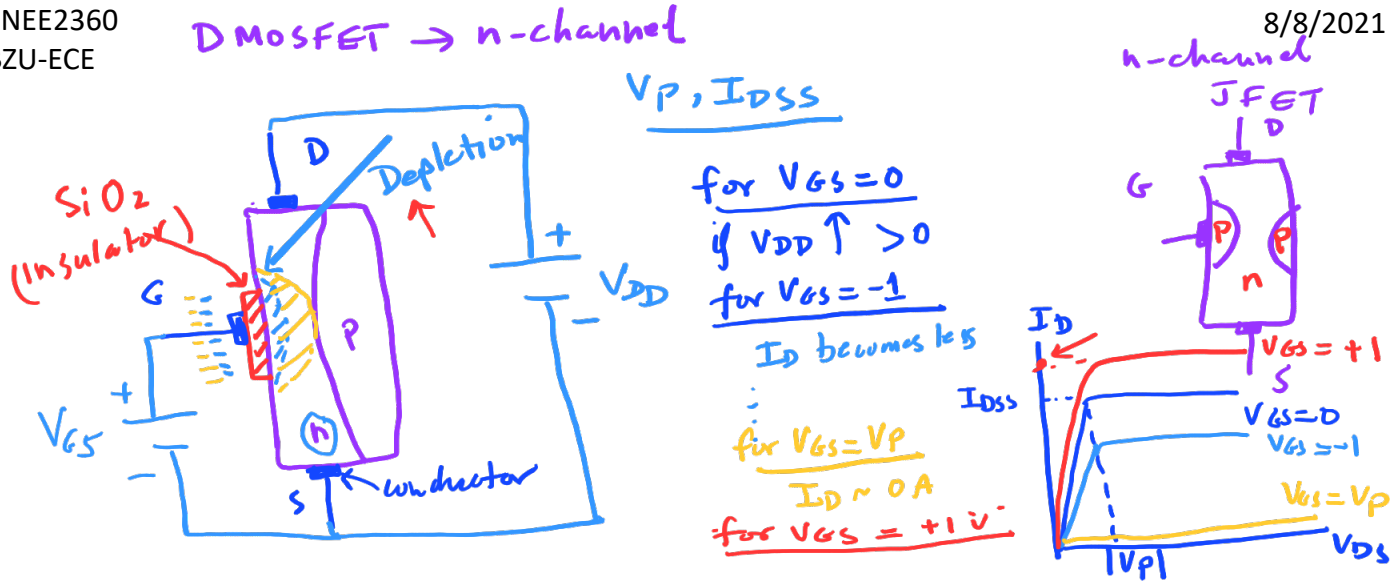
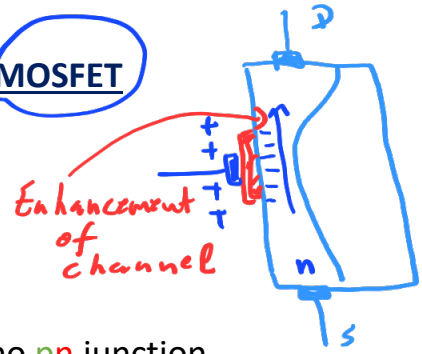
$R_G \rightarrow$ cannot be found from dc analysis

must be high



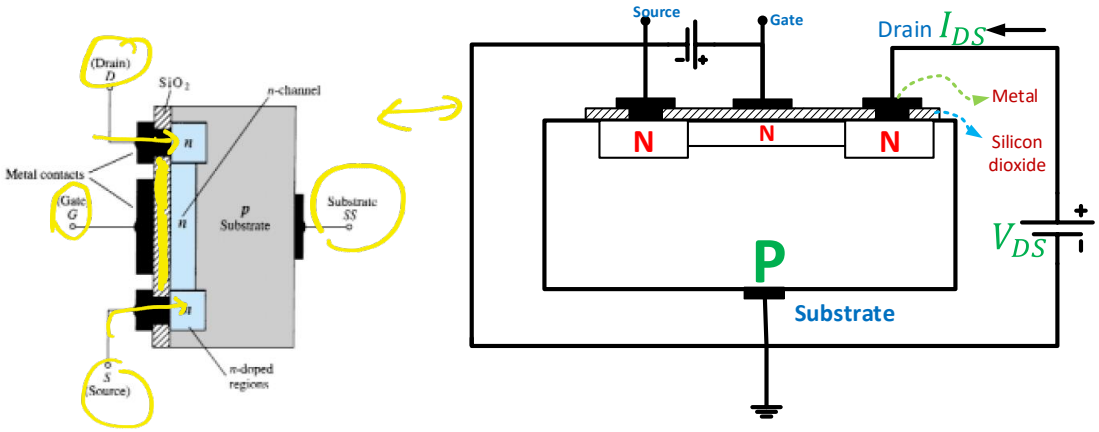
Metal Oxide Semiconductor Field Effect Transistor MOSFET



- 1) Depletion type MOSFET: DMOSFET
- 2) Enhancement type MOSFET: EMOSFET
- The MOSFET differs from the JFET in that it has no pn junction structure; instead, the gate of the MOSFET in insulated from the channel by a silicon dioxide (S_iO_2) large.
- Due to this the input resistance of MOSFET is greater than JFET.

Depletion type MOSFET:

- Construction of n-channel DMOSFET:



Operation , characteristic and parameters of DMOSFET

♦ **n-channel DMOSFET**

- On the application of V_{DS} and keeping V_{GS}=0 electrons from the n-channel are attracted towards positive potential of the drain terminal .

- This establishes current through the channel to be denoted as I_{DSS} at V_{GS}=0 .

- If we apply negative gate voltage ($V_{GS}< 0$) the negative charge on the gate repel electrons from the channel . The number of repelled electrons depends on the magnitude of the negative voltage V_{GS}.

- The greater the negative voltage applied at the gate , the level of drain current will be reduced until it reaches zero ; $V_{GS}= V_P$.

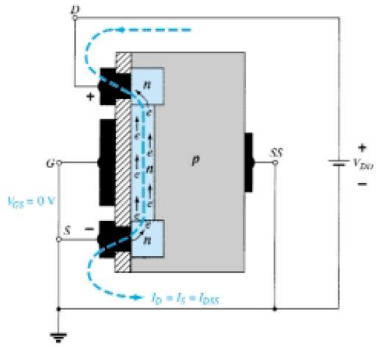


Figure 5.24 n-Channel depletion-type MOSFET with $V_{GS} = 0$ V and an applied voltage V_{DD}.

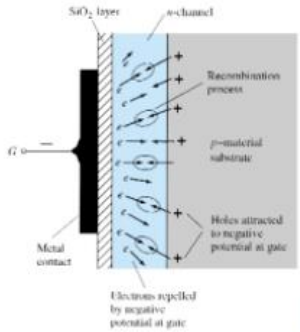


Figure 5.26 Reduction in free carriers in channel due to a negative potential at the gate terminal.

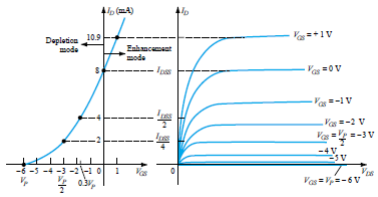
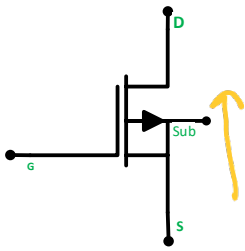
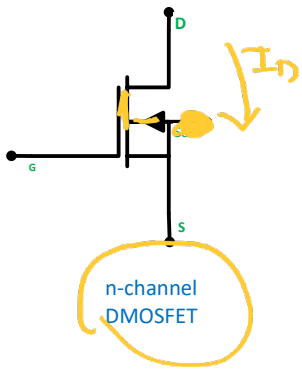


Figure 5.25 Drain and transfer characteristics for an n-channel depletion-type MOSFET.

- For positive value of V_{GS}, the positive gate will draw additional electrons from the p-type substrate and the drain current increases .

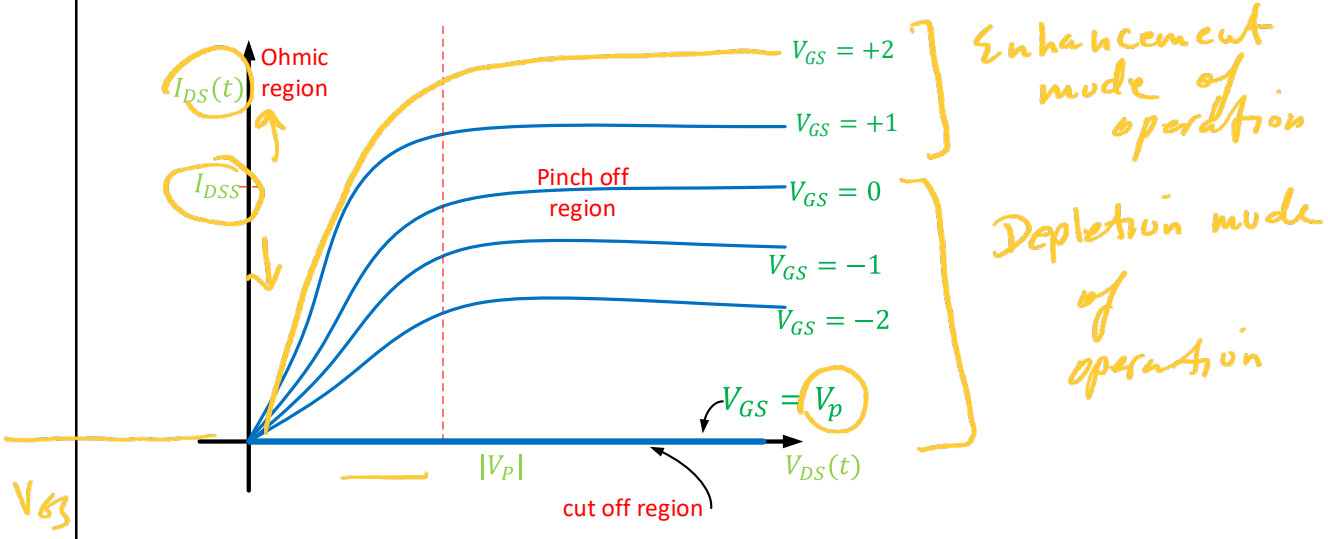


P-channel
DMOSFET

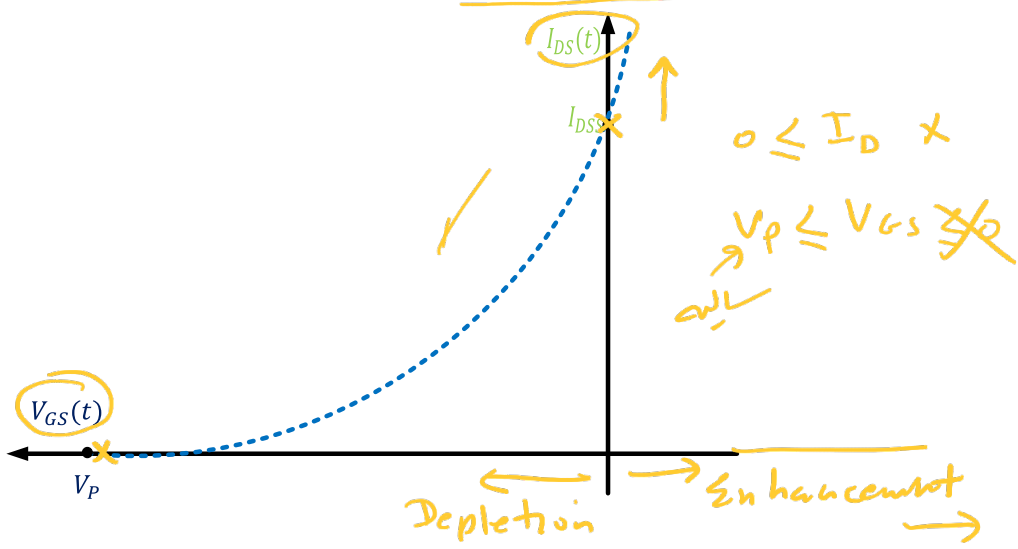


n-channel
DMOSFET

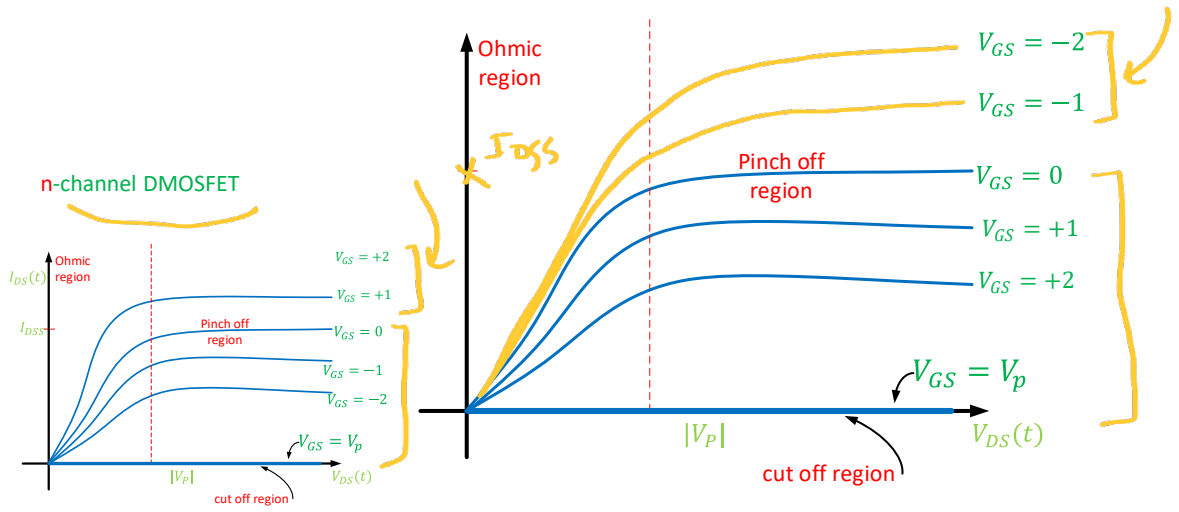
Drain characteristics for an n-channel DMOSFET



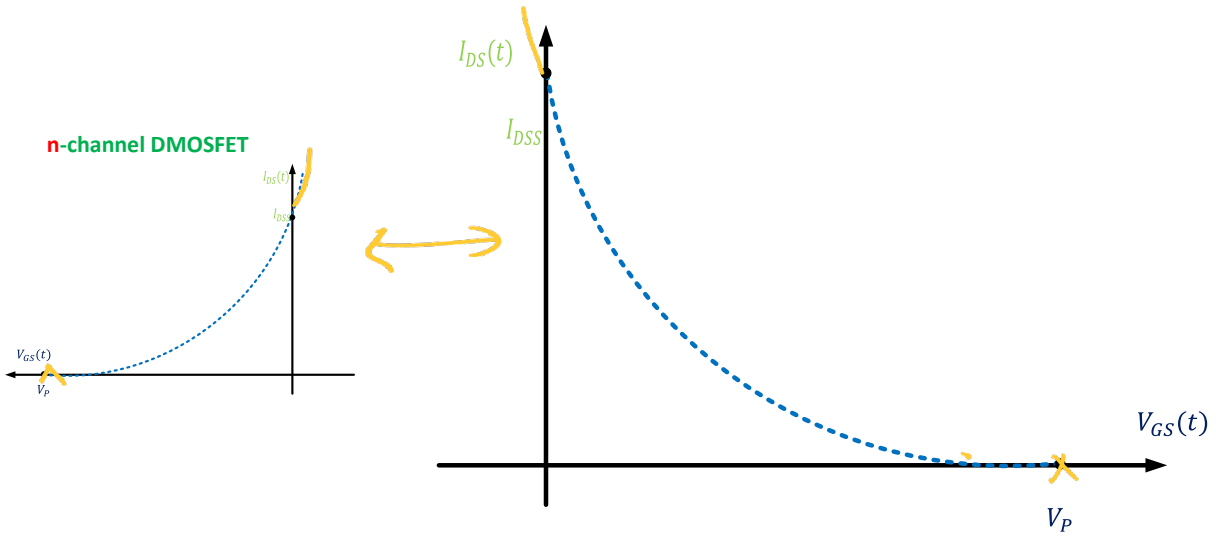
Transfer characteristics for an n-channel DMOSFET



Drain characteristics for an p-channel DMOSFET



Transfer characteristics for an p-channel DMOSFET



In the pinch off region

$$i_{DS}(t) = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

→ Depletion mode

$V_P \le V_{GS} \le 0$, $0 < I_D \le I_{DSS}$

→ Enhancement Mode

$V_{GS} > 0$

$I_D > I_{DSS}$

*

♦ **For the n- channel**

$V_{GS} > V_P$ (negative)

$V_{DS} > V_{GS} - V_P$

♦ **For the p- channel**

$V_{GS} < V_P$ (positive)

$V_{DS} < V_{GS} - V_P$

Example

Suppose that the DMOSFET is in the pinch off region

$I_{DS} = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$ 1

$V_{GS} = V_G - V_S = V_G$

$V_G = \frac{11M}{11M+100M}(12) = 1.19$ v 2

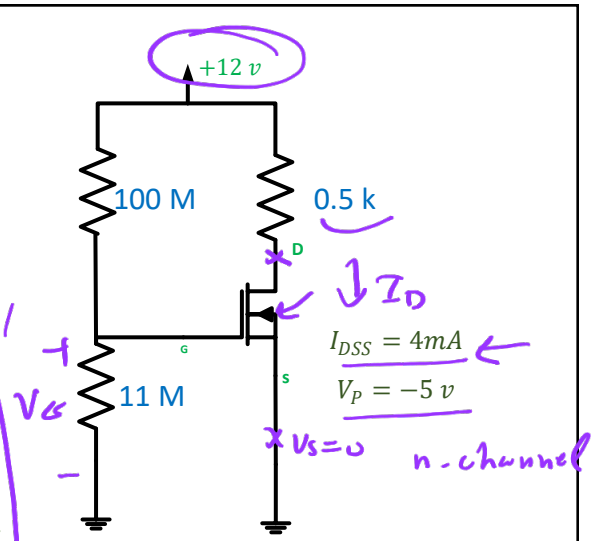
sub 2 into 1 , we obtain

$I_{DS} = 6.13$mA $> I_{DSS}$!! THIS IS POSSIBLE AND DMOSFET WILL OPERATE IN ENHANCEMENT MODE

$V_{DS} = V_{DD} - 0.5K\ I_{DS} = 8.93$ v

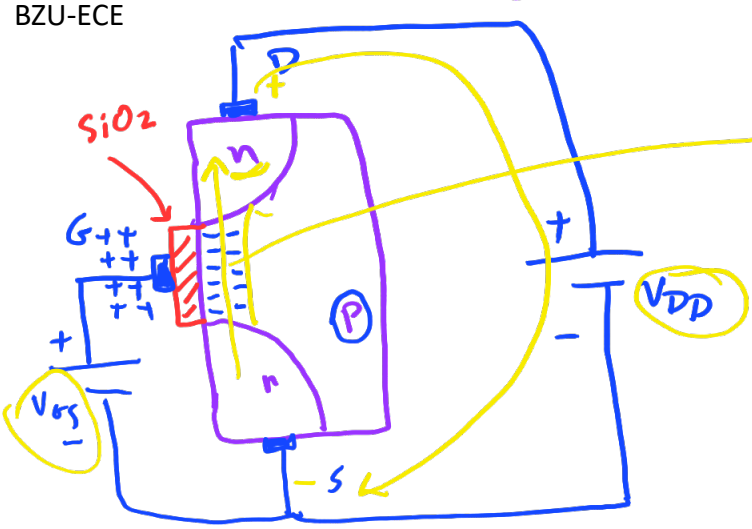
$V_{DS} >^{?} V_{GS} - V_P = 6.19$ v

pinch off region



$I_{DSS} = 4$mA $V_P = -5$ v

E MOSFET (n-channel)



→ no physical channel

→ we will have an induced channel due to VGS

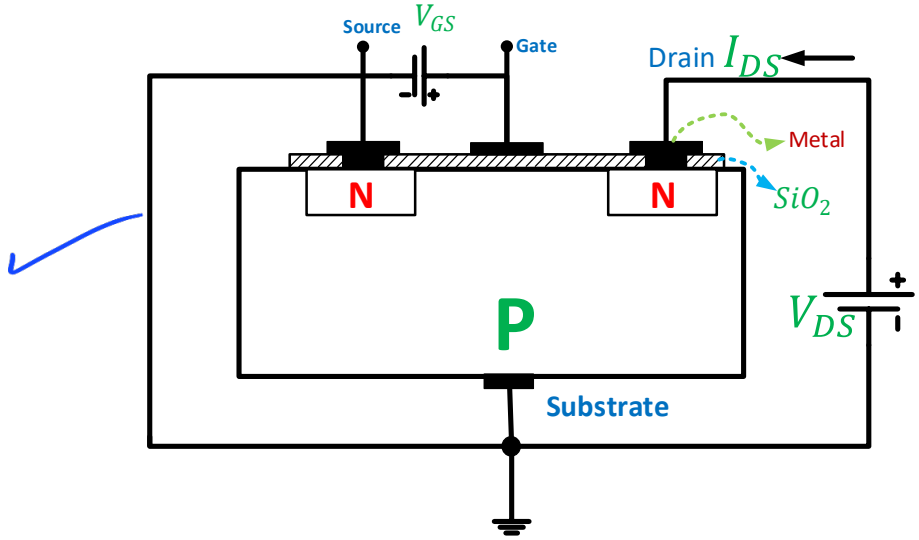
$V_{GS} > V_{GS(th)} = V_T$

→ gate-to source threshold voltage.

→ This is the minimum required voltage to have an induced channel (carriers near the gate)

Enhancement Type MOSFET

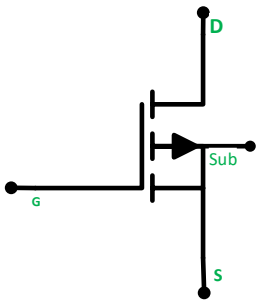
- Construction of n-channel EMOSFET:



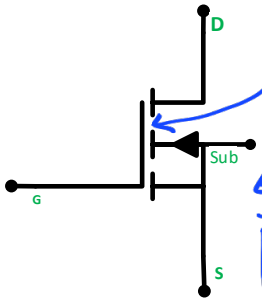
Operation , characteristic and parameters of EMOSFET

- On the application of $V_{DS}$and keeping V_{GS}=0 practically zero current flows .
- If we increase V_{GS} in the positive direction the concentration of electrons near the SiO_2 surface increases ,
- At particular value of V_{GS} there is a measurable current flow between drain and source ; I_{DS} .
- This value of V_{GS} is called threshold voltage denoted by V_T or $V_{GS(TH)}$
- A positive V_{GS} above V_T induce a channel and hence the drain current (I_{DS}) by creating a thin layer of negative charges (electrons) in the substrait adjacent to the SiO_2 large .

The conductivity of the channel is enhanced by increasing V_{GS} and thus pulling more electrons into the channel .

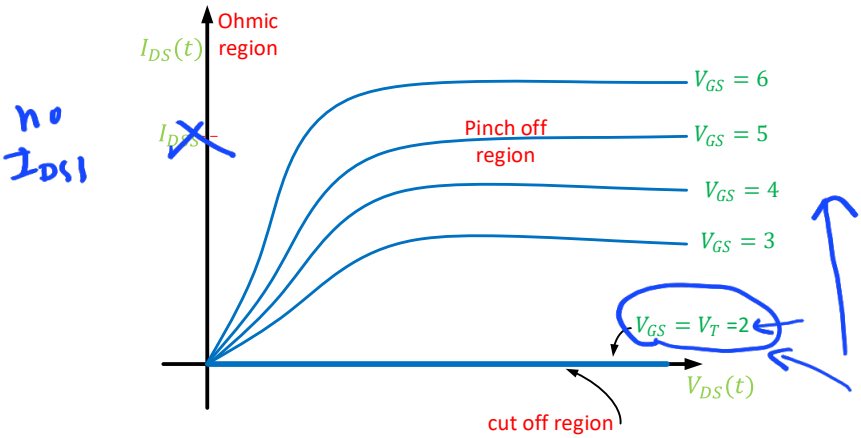


P-channel
EMOSFET

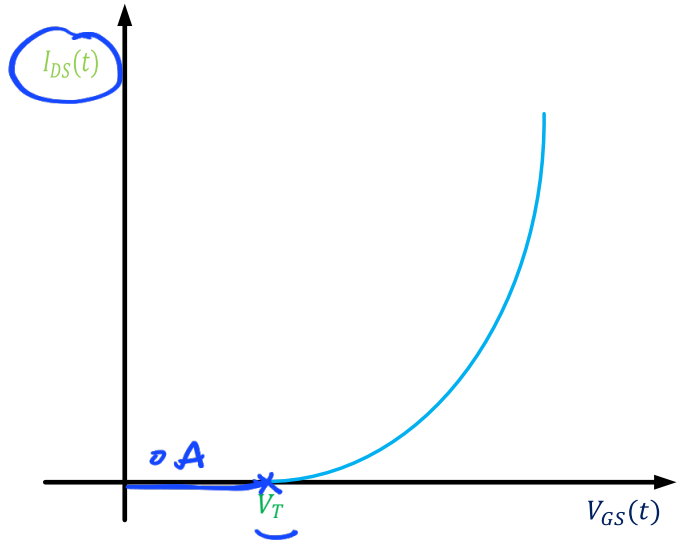


n-channel
EMOSFET

Drain characteristics for an n-channel EMOSFET

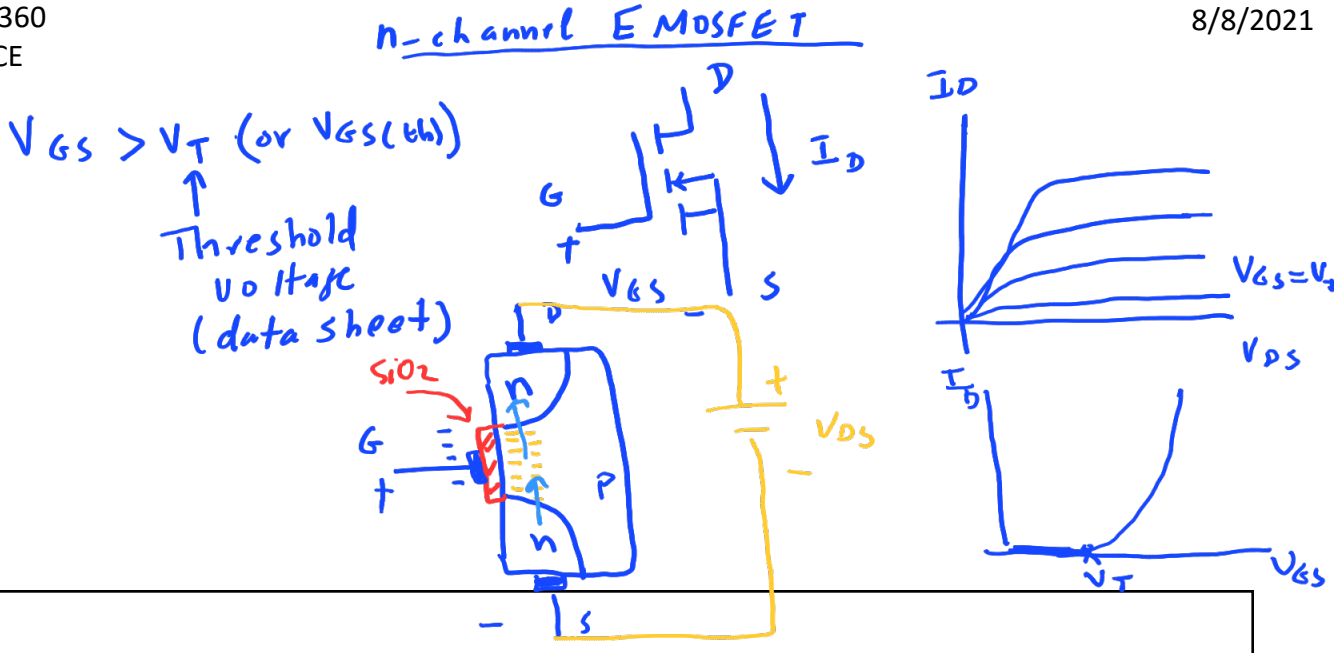


Transfer characteristics for an n-channel EMOSFET



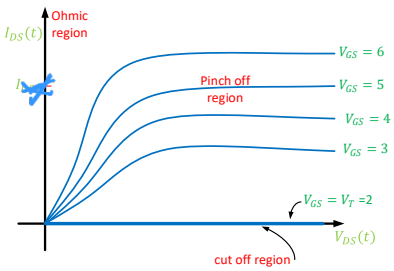
End of L18
sec 1

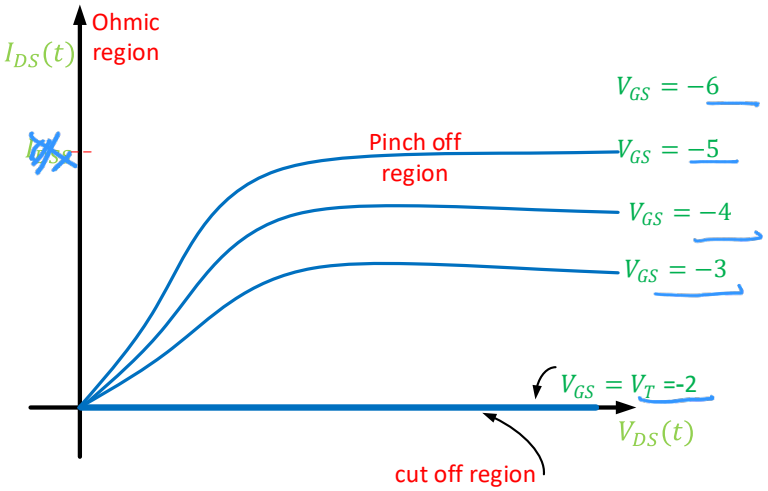
L19
12-8-2021



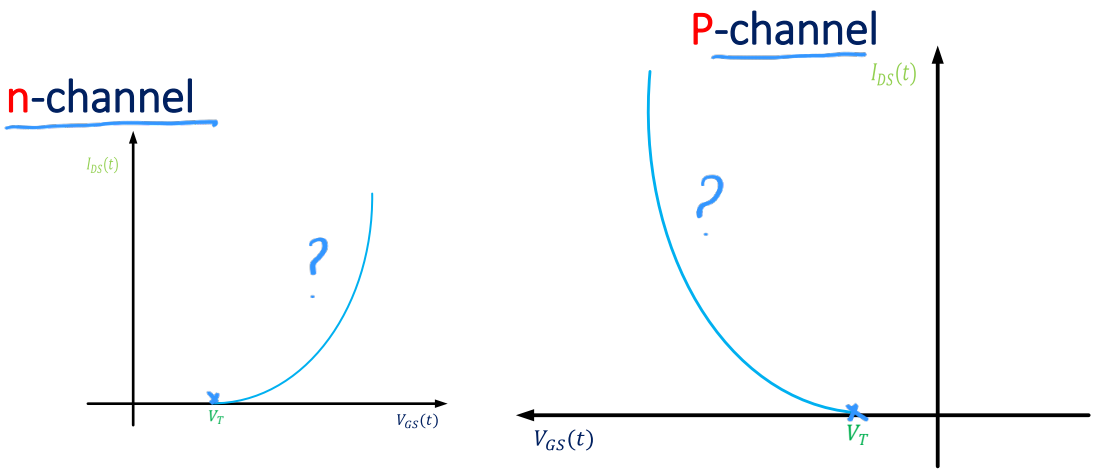
Drain characteristics for an p-channel EMOSFET

n-channel





Transfer characteristics for an p-channel EMOSFET



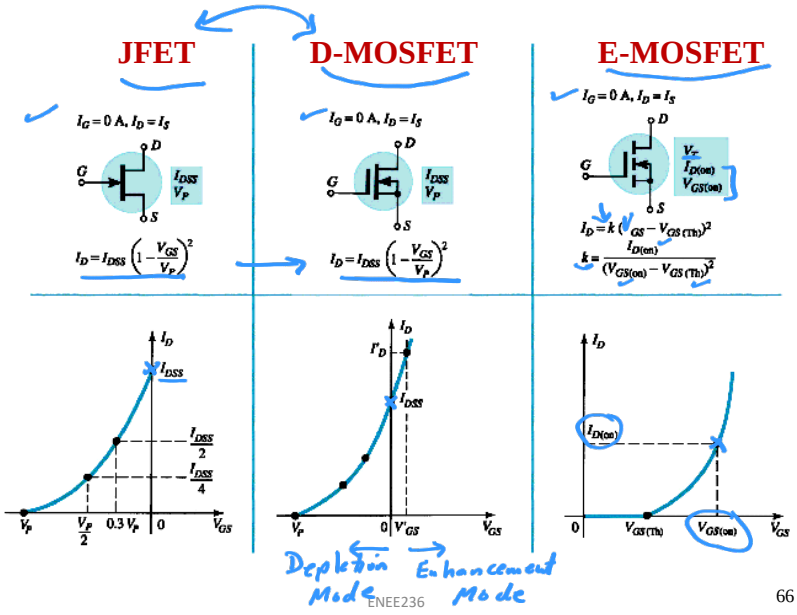
$I_D = f(V_{GS})$?

$$I_D = K_n \left(V_{GS} - V_T\right)^2 \Longrightarrow I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

↑ EMOSFET

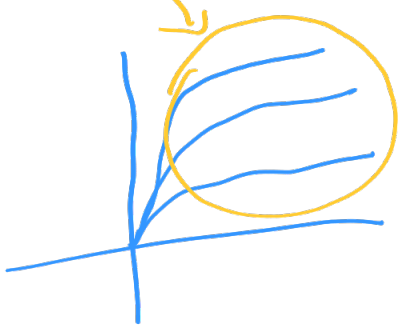
↑ JFET DMOSFET

Summary Table



In the pinch off region- EMOSFET

$$i_{DS}(t) = K_n (V_{GS}(t) - V_T)^2$$



$$|V_{DS}| > |V_{GS} - V_T|$$

both n-channel p-channel

$V_{GS} > V_T$	;	n- channel
$V_{GS} < V_T$	;	p- channel

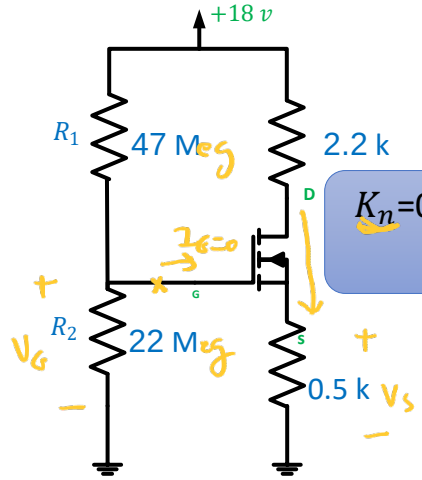
$I_{DS} = I_D = I_S$

Example → Find V_{GS}, I_D, V_{DS} ?

$I_D = I_{DS} = K_n(V_{GS} - V_T)^2$ 1

$V_{GS} = V_G - V_S$

$V_G = \frac{22M}{22M+47M}(18) = 5.74v$



$K_n = 0.25X10^{-3} A/V^2$
$V_T = 2$ v

EMOSFET

$I_D = \frac{5.74 - V_{GS}}{500}$

$I_D = K_n (V_{GS} - V_T)^2$ → تعالله تربيعيه V_{GS}

$V_S = (0.5K)\, I_{DS}$

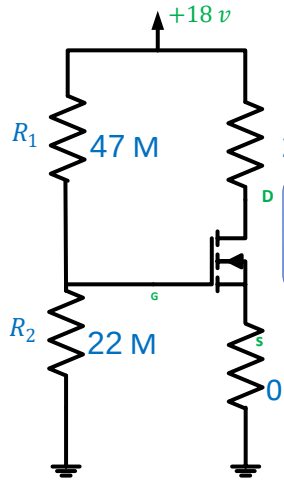
$V_{GS} = 5.74 - (0.5K)\, I_{DS}$.....2

$V_G - V_S$

solving for V_{GS}:

$V_{GS} = 4.78v$ √

$= -8.78v$ X $< V_T$



$K_n = 0.25X10^{-3} A/V^2$

$V_T = 2$ v

$I_{DS} = 1.92m$ A $= I_D$

$V_{DS} = 12.82 > |V_{GS} - V_T|$

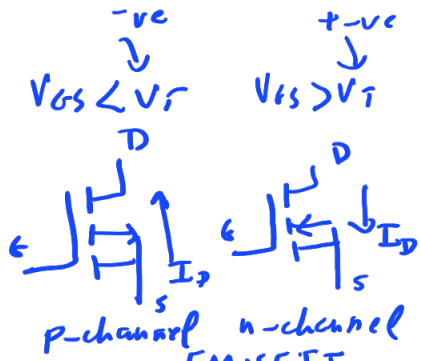
$|4.78 - 2| = 2.78$

$V_{GS} > V_T$

$V_{DS} = 18 - I_D(2.2K + 0.5K)$

$= 18 - 1.92m(2.7K)$

$= 12.82$ ✓



Complementary MOS (cmos) inverter

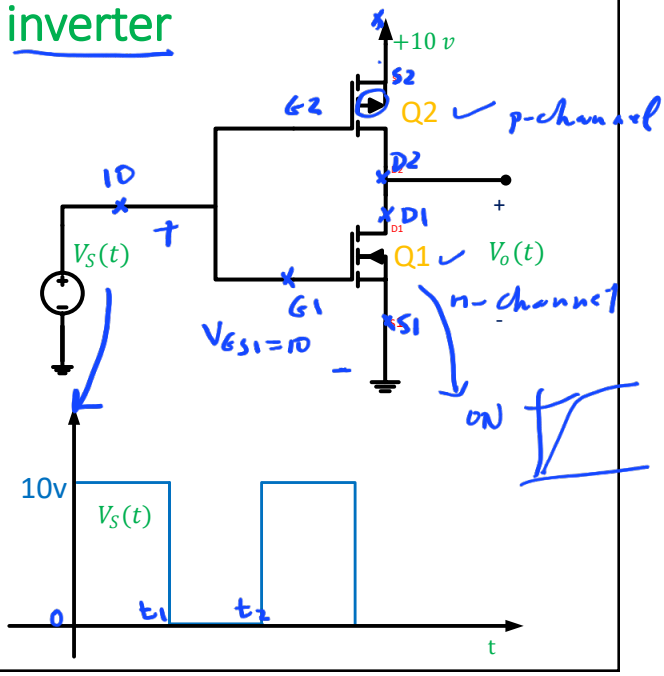
$V_{GS1} = V_{G1} - V_{S1} = 10\text{-}0 = 10\text{ v} > V_{T1}$ ✓ ON

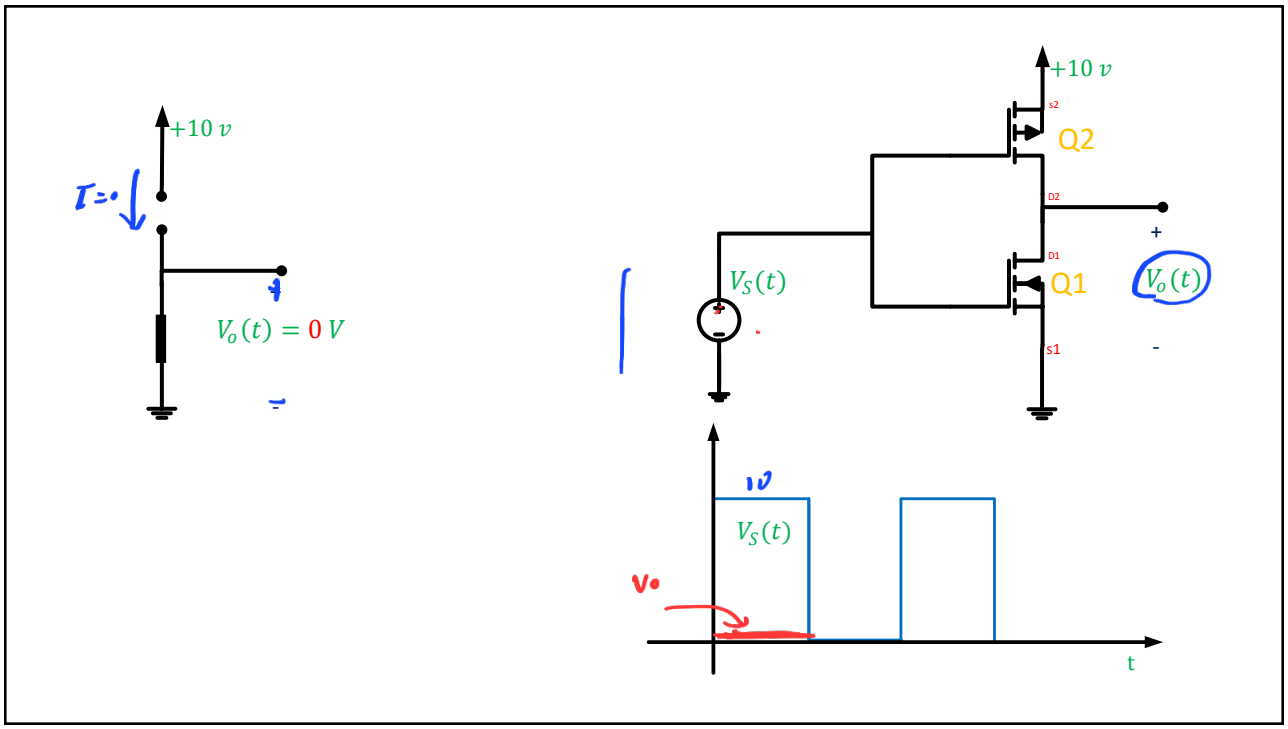
1) Let $V_S(t) = 10$ v [0, t_1]

$V_{GS2} = V_{G2} - V_{S2} = 10\text{-}10 = 0\text{ v} > V_{T2}$ ✗ OFF

Q_1 is on , replaced with short circuit

Q_2 is off , replaced with open circuit





$[t_1 - t_2]$

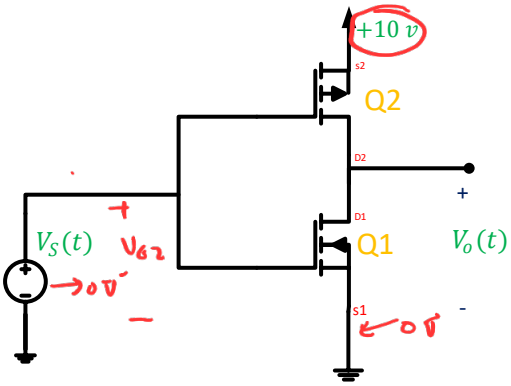
2) Let V_S(t) = 0 v

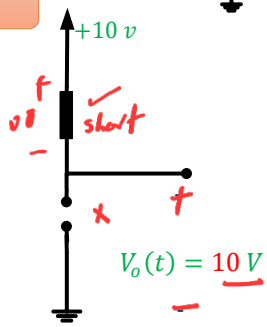
$V_{GS1} = V_{G1} - V_{S1} = 0 = 0\ v < V_{T1}$ → OFF

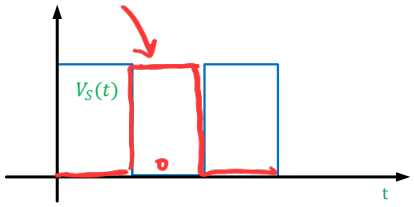
Q_1 is off , replaced with open circuit

$V_{GS2} = V_{G2} - V_{S2} = 0\text{-}10 = -10\ v < V_{T2}$ → ON

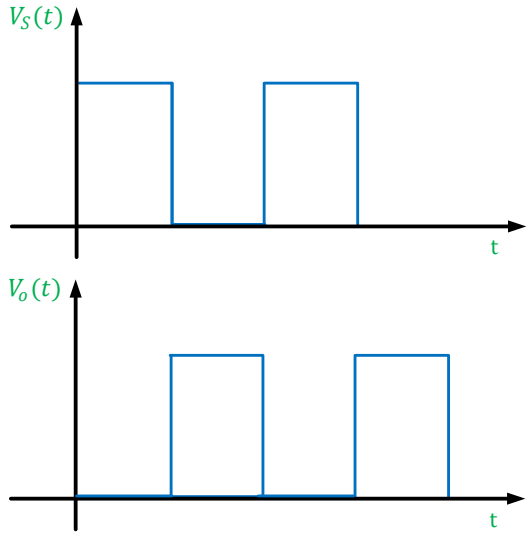
Q_2 is off , replaced with short circuit







Inverter = NOT GATE



CMOS - inverter