

Faculty of Engineering and Technology

Department of Electrical and Computer Engineering

Digital Electronics and Computer Organization

ENCS 2110

**Experiment No. 3 - Encoders, Decoders, Multiplexers, and Demultiplexers**

Post Lab 3

Student Name: alaa moqade

Student ID : 1211910

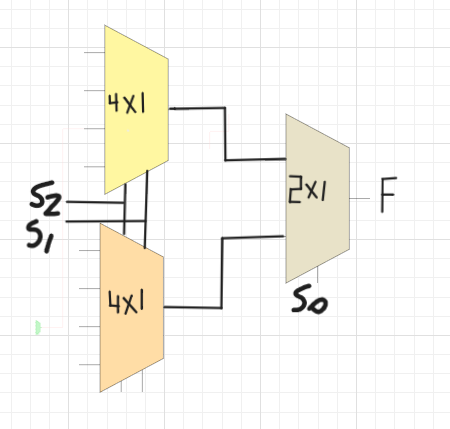
Partner ID: 1221630 Amal Qadah , 1170049

Instructor : Jamal Seyam

T.A : Haleema Hmedan

Section : 1

1. **Implement 8x1 Multiplexer using lower order Multiplexers Show how to solve t.**



**Q2) Design a Majority Circuit; a circuit that takes 4 inputs A, B, C, D and 1 output Y. Its output equals 1 when 3 or 4 of the inputs are 1. You can only use two 4×1 multiplexers.**



1. **The truth table :**

0

0

0

D

0

D

D

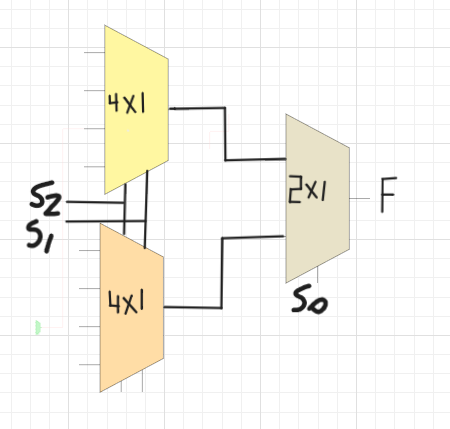
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|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | D | Output(Y) |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

B) so y(A,B,C,D) = ∑ (7,11,13,14,15)

C ) the chart :



0

D

D

1

0

0

0

D