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TuTh 9:30-11am

EECS 141: SPRING 03—FINAL

For all problems, you can assume the following transistor parameters (unless otherwise mentioned):

NMOS: V_{Tn} = 0.4V, k_n' = 115μA/V^2, V_{DSAT} = 0.6V, λ = 0, γ = 0.4V$^{1/2}$, $2\Phi_F$ = -0.6V

PMOS: V_{Tp} = -0.4V, k_p' = -30μA/V^2, V_{DSAT} = -1V, λ = 0, γ = -0.4V$^{1/2}$, $2\Phi_F$ = 0.6V

NAME	**SOLUTION** Last First

SID	

Problem 1 (10):

Problem 2 (15):

Problem 3 (14):

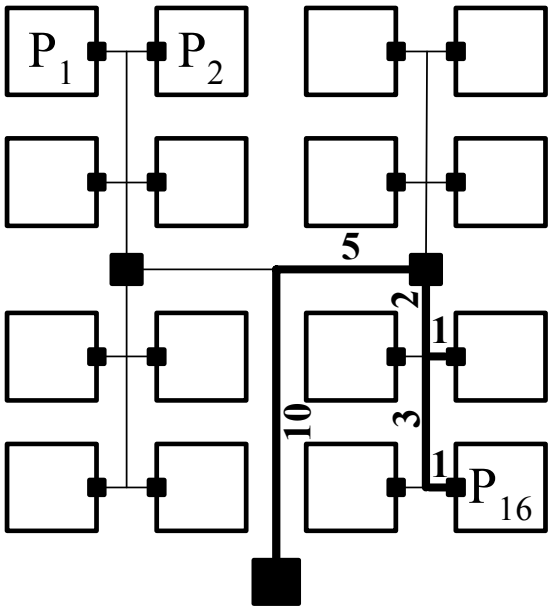
Problem 4 (18):

Problem 5 (18):

Total (75)	

Problem 1: Timing and Clocking (10 pts)

In order to boost profits, Intel has decided that their next-generation microprocessor has to have ultimate performance. To achieve the desired performance, 16 processors are integrated on the same die (the chip is hence called *seidecium* – for obvious reasons). The designer of the clocking architecture has come up with the strategy shown in the Figure below. A single clock signal is distributed over the complete chip. Three levels of buffering are used as shown by the black boxes in the Figure.



Important parameters:

$r_{wire} = 0.1(k\Omega)/(cm)$

$c_{wire} = 0.1(pF)/(cm)$

$t_{pbuffer}$ (level 1,2,3) = 0.1ns

FIG. 1 Seidecium processor clock distribution network. The numbers annotated on the figure indicate the lengths of the wiring segments (in cm).

a) Determine the maximum skew between the different processor modules. **(4 pts)**

(1 pt) max skew determined by (2+3+1)cm and (2+1)cm wire segments

(1 pt) wire delay: $t_{pwire} = 0.38rcL^2$

(1 pt) max skew = difference in wire delay

(1 pt) max skew = $0.38rc(6^2-3^2)$ = 102.6ps

max skew:	**102.6ps**

b) The goal of the designers is to reach a 4 GHz clock speed. Determine the maximum delay of the logical function blocks given that 20% of the clock period is due to the delay of registers. Also, note that the maximum internal skew within a processor module equals 20 ps. **(3 pts)**

(1 pt) $T_{Clk} = 1/f_{Clk} = 250ps$

(1 pt) $T_{Clk} = t_{logic}(max) + t_{REG} + skew(external) + skew(internal)$

(1 pt) $t_{logic}(max) = 0.8T_{Clk} - skew(external) - skew(internal)$
$t_{logic}(max) = 200 - 102.6 - 20 = 77.4ps$

t_{logic}(max)= 77.4ps

c) The Intel designers forgot to account for one thing though. Due to the parameters variations over the die, it is observed that the delay of the clock buffers can vary over 25% (in both positive and negative directions). Determine the worst-case clock speed due to these variations. **(3 pts)**

(1 pt) $T_{Clk}^{PV} = T_{Clk} + variation$

(1 pt) $variation = 4*0.25*t_{pbuffer} = 100ps$
(factor of 4 is from 2 levels of buffers going in opposite directions)

(1 pt) $f_{Clk}(min) = 1/T_{Clk}^{PV} = 2.86GHz$

f_{clock}(min)= 2.86GHz

Problem 2: Interconnect (15 pts)

a) A driver-receiver pair in CMOS technology is shown in Figure 2.

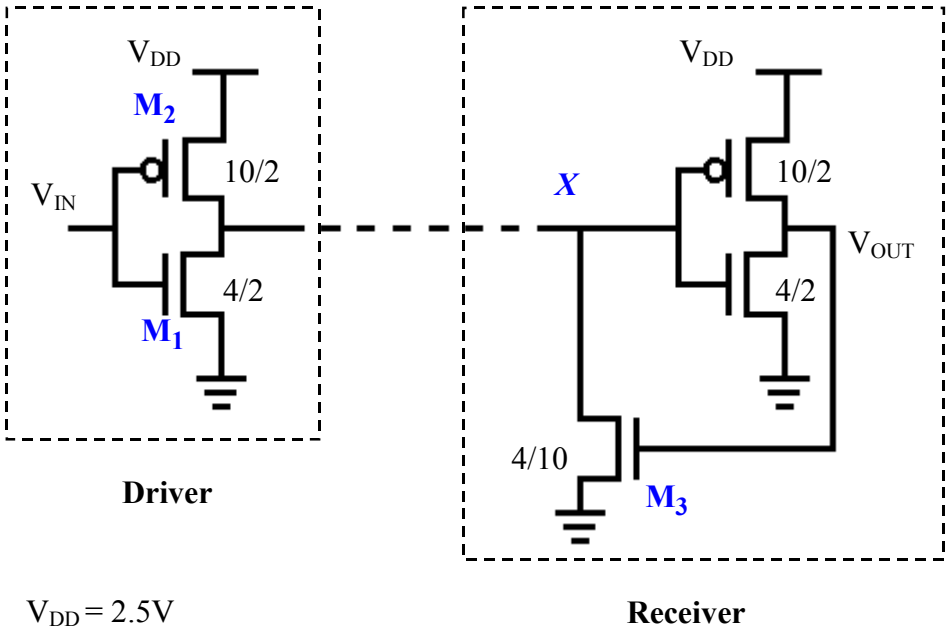


FIG. 2 Driver and receiver. Numbers on transistors indicate (W/L) ratios.

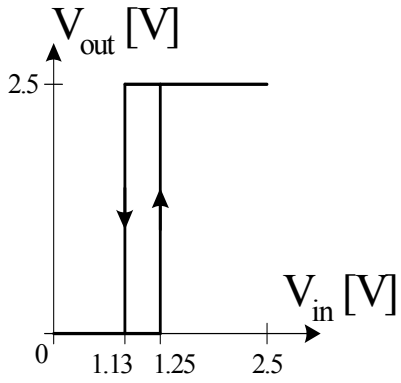
Assume that all transistors are short-channel devices. V_M of the driver inverter equals $V_{DD}/2$. Draw the voltage transfer characteristic V_{OUT} versus V_{IN} when the driver is **directly** attached to the receiver. Write down circuit analysis equations and calculate the break points on the VTC. **(4 pts)**

(1 pt) V_{M+}: initially $V_{in} = 0$, $V_{out} = 0$ (M_3 off), therefore $V_{M+} = V_{DD}/2 = 1.25V$

(1 pt) $V_{in} = V_{out} = V_{M-}$: $V_x = V_{DD}/2$, therefore M_1, M_2, M_3 are vel. saturated

(1 pt) from $I_D(M_3)+I_D(M_1) = I_D(M_2)$ we obtain $V_{M-} = 1.13V$

(1 pt) VTC using calculated data



b) The driver and receiver in a) can be used to drive intermediate circuits. Briefly comment on the advantage and disadvantages of this driving scheme from the perspectives of performance and power. **(3 pts)**

(1 pt) Advantage:

+ noise robust

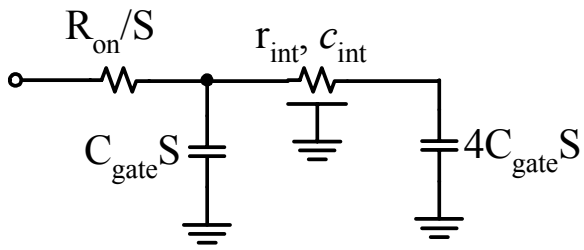
(2 pts) Disadvantages:

- high power

- low speed

c) Derive a global expression of the **typical gate (being an inverter) delay** in the presence of wiring with a length equal to L_{net} followed by a fanout of 4 equivalent gates. Make sure to include all components of delay. You may assume that the following parameters are given: C_{gate} and R_{on} of driver (per unit width), r_{int} and c_{int} of interconnect (per unit length). You may assume that the diffusion capacitance at the output of the gate is approximately equal to its gate capacitance. **Clearly state all other assumptions you are making (e.g. wire model). This question is not related to parts a) and b). (4 pts)**

(1 pt)



(3 pts) $\text{delay} = 0.69R_{on}/S*C_{gate}S + 0.69R_{on}/S*c_{int}*L_{net} + 0.38r_{int}*c_{int}*L_{net}^2$
$+ 0.69(R_{on}/S + r_{int}*L_{net})*4C_{gate}*S$

(each term in the equation is worth one point)

d) Discuss how you would reduce the delay if the capacitive load of the fanout is the dominant factor and discuss the minimum value of the delay. **(2 pts)**

(2 pts) minimum sizing (S = 1 in the delay formula from previous page)

e) Discuss how you would reduce the delay if the interconnect delay is the dominant factor. Derive an expression for the minimum delay. **(2 pts)**

(2 pts) differentiate the delay expression with respect to S and set to zero

solution: $S = \sqrt{(R_{on}c_{int})/(4C_{gate}r_{int})}$

Problem 3: Memory (14 pts)

The Figure below shows a novel 2T-DRAM cell to be used in a low-voltage application. **The supply voltage is fixed at 1 V**. *WBL* is the write bit-line, *RBL* is the read bit-line. **Assume initially that node P is fixed at GND**.

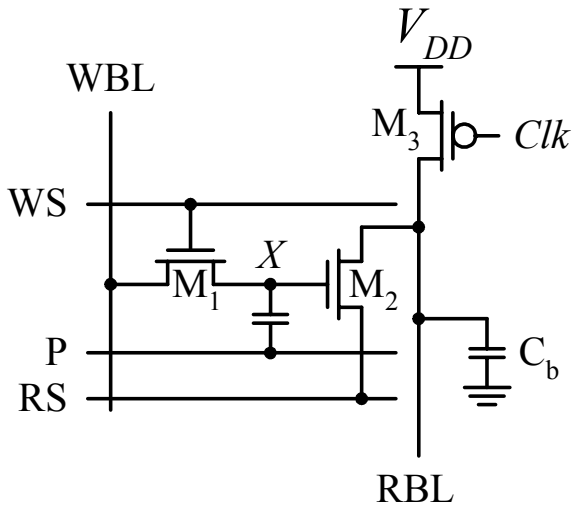


FIG. 3 A 2-T DRAM cell.

a) Determine the signal levels (V_{DD} or GND) that have to be applied to the control signals (WS, RS) to perform a write operation into and a read operation from the cell? **(4 pts)**

WS (Wr): **V_{DD}**

RS (Wr): **V_{DD}**

WS (Rd): **GND**

RS (Rd): **GND**

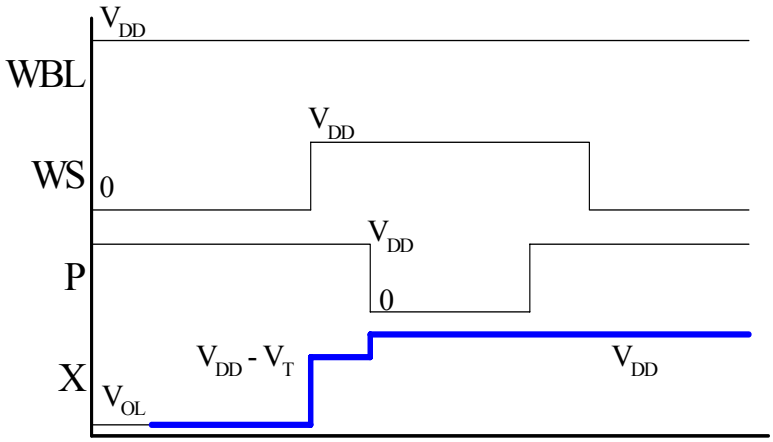
(each signal is worth one point)

b) Explain why this scheme has some major problems. **(2 pts)**

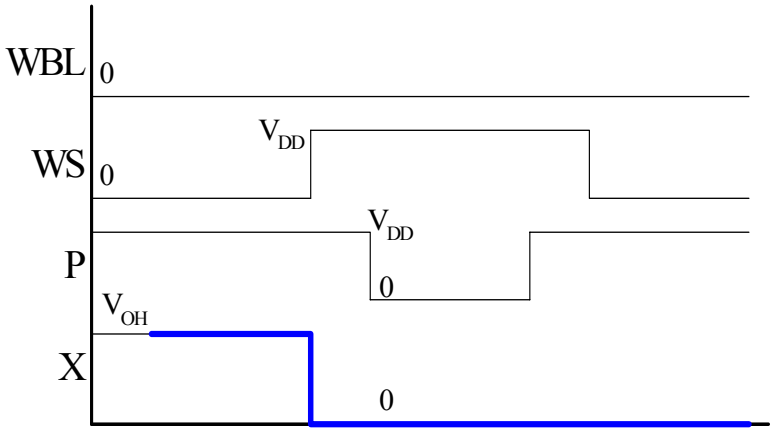
reduced voltage swing at node *X*

(also reduced reliability)

c) Instead of node *P* being fixed at GND, we apply a waveform as shown in figure below. Fill in the timing diagrams for the write operation. Denote the voltage levels in terms of V_{DD} and V_T. Assume there is enough time to let the transient effects settle out (no need to draw them). Explain why this approach is substantially better. **(6 pts)**



(2 pts)



(2 pts)

This aproach is better because:

(2 pts) full voltage swing at node *X*

d) Does the memory cell require refresh? Why or why not? **(2 pts)**

(2 pts) Yes. (because the cell is dynamic)

Problem 4: Multivibrator Circuits (18 pts)

a) Shown in the Figure below is a design of a **Schmitt trigger**. Determine the (W/L) ratio of transistor M_1 so that $V_{M+} = 3V_{Tn}$. $V_{DD} = 2.5V$. You may ignore the body effect in this question. You may also assume a long channel device. Clearly state your other assumptions. **(6 pts)**

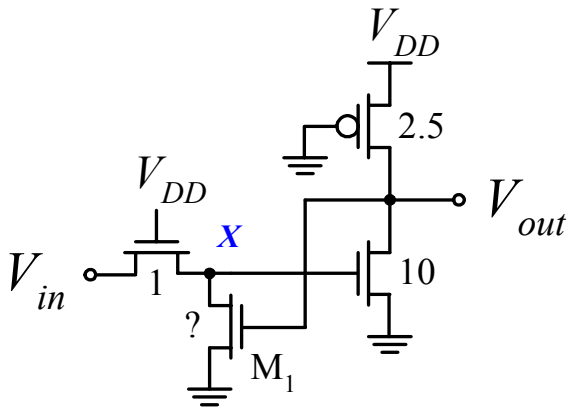


FIG. 4 Schmitt trigger. Numbers on transistors indicate (W/L) ratios.

(1 pt) first determine V_X from the output stage

(MN and MP are both in *vel. sat*)

(2 pts) $2.5*30*[(2.5 - 0.4)*1 - 1/2] = 10*115*[(V_X - 0.4)*0.6 - 0.6^2/2]$

solution: $V_X = 0.874V$

(1 pt) given V_X and V_{M+}, M_1 is *vel. sat* and input NMOS is *linear*

V_{DS}(input NMOS) = 0.326V

(1 pt) $(2.5 - 0.874 - 0.4)*0.326 - 0.326^2/2 = (W/L)_1*[1.2*0.6 - 0.6^2/2]$

(1pt) solution: $(W/L)_1 = 1.15$

$(W/L)_1$= 1.15

b) Determine **approximately** the value of V_{M-} **(4 pts)**

* initially M_1 is turned off

* input NMOS is in linear region, therefore $V_X \sim V_{in}$

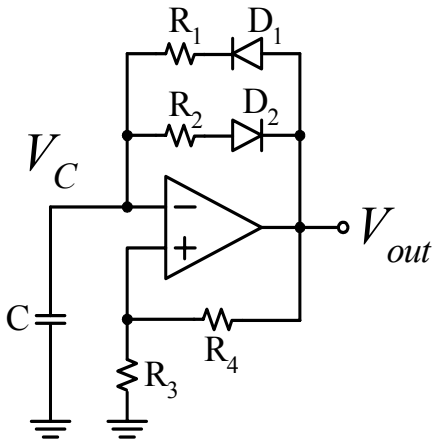
* consider output stage where $V_X \sim V_{in}$ and $V_{out} \sim V_{M-}$

(same equation as in part (a) where we calculated V_X)

* solution: $V_X = 0.874V$ (approximately since M_1 has turned on)

$V_{M-} = 0.874V$

c) Figure 5 shows an astable multivibrator. Calculate and draw voltage waveforms (see next page) at the capacitor V_C and at the output V_{out}. **(6 pts)**



Assumptions:

Ideal amplifier with symmetric supply

($V_{out}^{max} = V_{cc}$, $V_{out}^{min} = -V_{cc}$)

$R_1 = 1k\Omega$, $R_2 = 3k\Omega$, $R_3 = R_4 = 4k\Omega$

$C = 1$ nF, $V_{cc} = 5V$, $V_D = 0.6V$ (ideal diode)

V_{out} ($t = 0^-$) = $-V_{cc}$

FIG. 5 Astable multivibrator.

(1 pt) switching threshold is at +/- $V_{cc}*R_3/(R_3 + R_4)$ = +/- $V_{cc}/2$ = +/- 2.5V

(1 pt) charging C is through D_1, time constant $tau_1 = R_1C$ = 1us

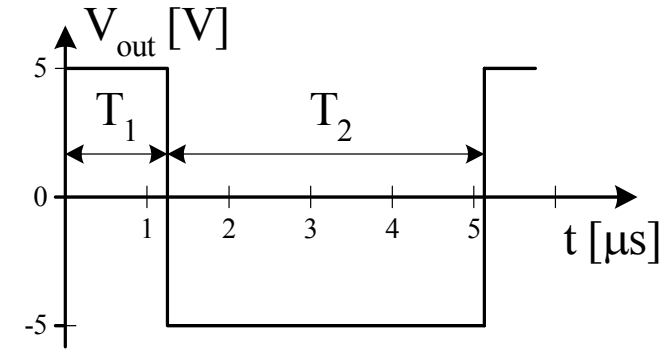
(1 pt) dis-charging C is through D_2, time constant $tau_2 = R_2C$ = 3us

(1 pt) asumptotic value of V_C is +/- (V_{cc} - V_D) = +/- 4.4V

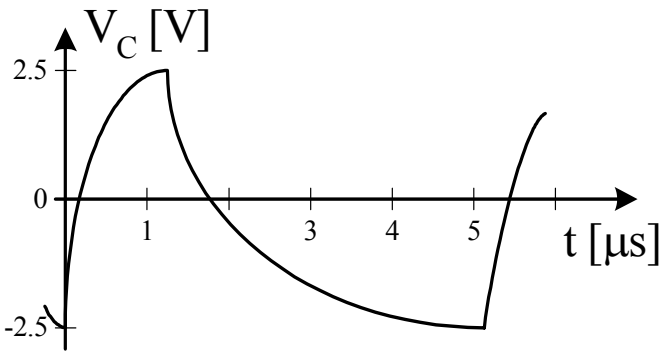
$V_C(t) = V_C(inf.) + [V_C(inf.) - V_C(0)]*exp(-t/tau)$

$T_1 = RC_1*ln((3V_{cc}-2V_D)/(V_{cc}-2V_D)) = 1.29us$

$T_2 = RC_2*ln((3V_{cc}-2V_D)/(V_{cc}-2V_D)) = 3.87us$



(1 pt)



(1 pt)

d) What is the oscillation frequency of the multivibrator in Fig. 5? **(2pts)**

(1 pt) $f_{OSC} = 1/(T_1 + T_2) = 1/((R_1 + R_2)C*ln(3V_{cc} - 2V_D)/(V_{cc} - 2V_D))$

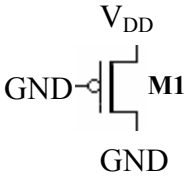
(1 pt) $f_{OSC} = 193.8$ kHz

f_{OSC}= 193.8kHz

Problem 5: Scaling and Overall Knowledge (18 pts)

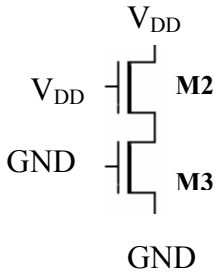
a) Determine the region of operation (Cut off, Linear, Saturation, Vel. saturation) in the following configurations. You may assume that all transistors are short-channel devices and have identical sizes. Ignore body effect. $V_{DD} = 2.5V$.

Explain your reasoning, and show your derivations if needed (5 pts).



$V_{GS} = V_{DS} = V_{DD}$

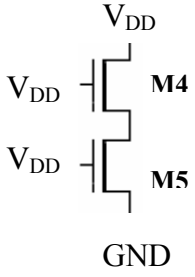
M1 vel. sat **(1 pt)**



$V_{GS3} = 0$

M3 off **(1 pt)**

M2 linear (off) **(1 pt)**



$(V_{DD} - V_{Tn})V_X - V_X^2/2 = (V_{DD} - V_X - V_{Tn})V_{DSAT} - V_{DSAT}^2/2$

solution: $V_X = 0.435V$

M4 vel. sat **(1 pt)**

M5 linear **(1 pt)**

b) The first row of the table given below lists the characteristics of a successful microprocessor designed for desktop systems. A low power version for portable use is desired and several changes are therefore made to the design. Use simple hand calculations to fill in estimates for blank cells in the table. Use the space below to explain your answers (if needed). **All transistors exhibit short-channel I-V characteristics. (7 pts)**

	V_{DD}/V_T (V)	W, L, t_{ox} (relative)	C_{ext}* (nF)	C_{int} (nF)	I_{sat} (mA)	Ext. clock (MHz)	Int. clock (MHz)	Power (W)
Original	2.5 / 0.4	1	3	1	1	300	900	8
Reduced Voltage	1.25 / 0.2	1	3	1	**0.5**	**300**	**900**	**2**
Reduced Dimension	1.25 / 0.2	0.6	3	**0.6**	**0.5**	**300**	**1500**	**2**
Low cap. Packaging	1.25 / 0.2	0.6	2	**0.6**	**0.5**	**450**	**1500**	**2**

*** External C is dominated by packaging. Internal C is dominated by transistor gate cap.**

Basic relationships:

* $I_{sat} = v_{sat}*C_{ox}*W*(V_{GT} - V_{DSAT})$
* $f_{ext} \sim 1/C_{ext}$
* $C_{int} \sim WL/t_{ox}$
* $f_{int} \sim 1/C_{int}$
* $P \sim f_{int}*C_{int}*V_{DD}^2$

(each entry in the table is worth 0.5 pts)

c) For each of the following statements, indicate whether it is true or false (circle one answer). (**6 pts; 0.5 for correct answer; -0.25 for wrong one)**

T (F) (a) The speed of a ring oscillator can **continuously** be improved by increasing the W/L ratio of the inverters.

(T) F (b) Decreasing supply voltage helps to alleviate the velocity-saturation problems.

(T) F (c) The load capacitance of a static CMOS gate has no effect on its VTC.

T (F) (d) A Φn-block dynamic gate will not have **any** charge sharing problems if only 0->1 transitions occur at its inputs during evaluation

T (F) (e) The transistors in a Manchester carry chain should be sized progressively **larger** from the input to output to reduce the propagation delay.

(T) F (f) Low-swing buses save power and reduce propagation delay at the same time. **(true for delay b/c we add a sense amp)**

T (F) (g) The delay of a static inverter is **minimized** if $(W/L)_p/(W/L)_n$ is equal to μ_n/μ_p.

T (F) (h) Silicided poly lines reduce the delay of a wire by decreasing the **capacitance**.

(T) F (i) The minimum propagation delay between two latches determines if a race condition will occur due to clock skew.

T (F) (j) A 3-transistor DRAM cell **requires** a sense amplifier for the cell to be functional.

T (F) (k) A NAND-based ROM structure is typically more compact and **faster** than a NOR-based one.

T (F) (l) Given a fixed characteristic impedance Z_0, the delay of a transmission line is reduced when using Copper instead of Aluminum as interconnect material. **(T-line delay is independent of *r*)**