جامعة بيرزيت

BIRZEIT UNIVERSITY

# ANSWER BOOKLET

Student: advan digital Number 4

Course: Department: ..... Number: .....

Division: ..... Instructor: .....

Date: ..... ..... .....

Day Month Year

For Instructor's Use

| Question | Grade |
|---|---|
| 1 | |
| 2 | |
| 3 | |
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| 5 | |
| 6 | |
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| 10 | |
| 11 | |
| 12 | |
| **Total** | |

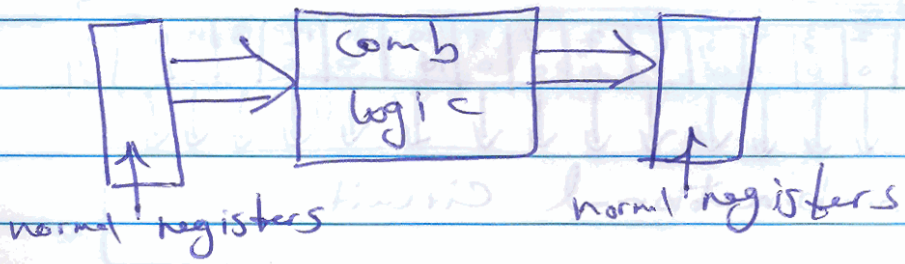
## ⊛ Built In Self Test (BIST)

- When VLSI chips become more complicated, it is good to make these chips self-testing. By this way we can overcome the problem of searching of test vectors and we can apply test inputs at the full speed clock.

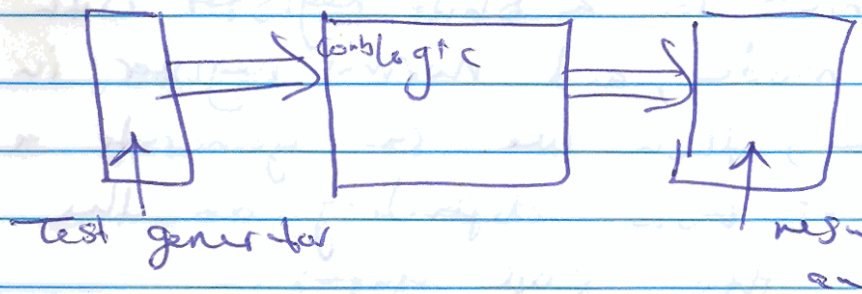
- ICs which are built in self test have blocks of logic embedded in the circuit to generate tests, and to interpret the results.

- In these ICs we also have two modes of operation: normal and test modes.

- In normal mode, the circuit will have the following appearance

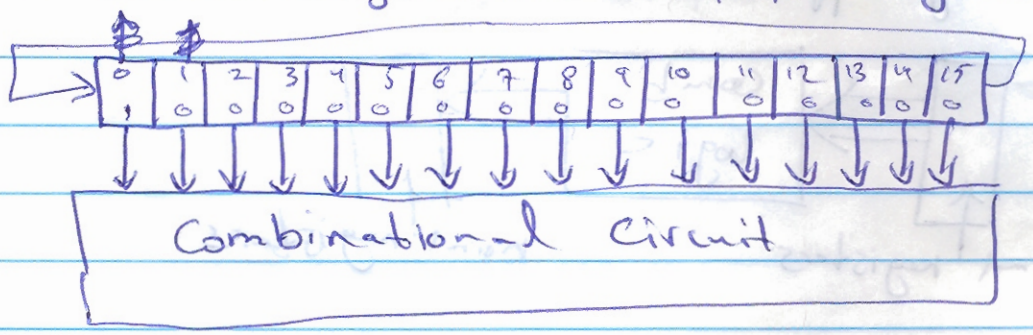



- In test mode, the circuit have the following appearance

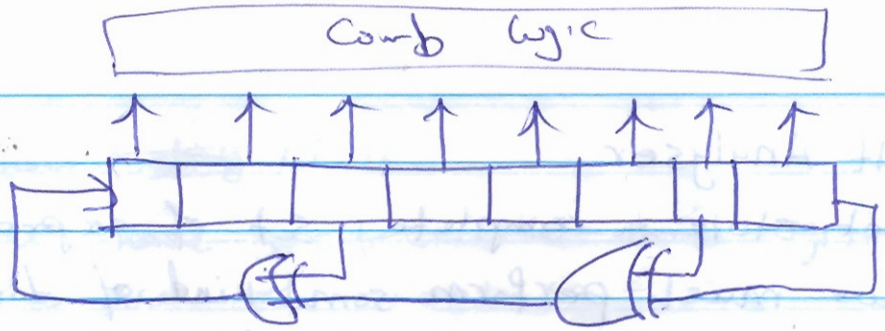


## (*) The test generator

- we need the test generator to be ~~very simple~~ very simple, so we can't figure out a clever set of test vectors.
- The simplest way to get a good fault coverage is to exhaustively test the system (trying to generate a large number of test vectors as possible).
- for example, for a 16 bit input, this will require $2^{16} = 65536$ tests.
  (very large, but it is acceptable because of the high speed clock in the system).
- if we use a 16-bit circular shift register, then we can generate 16 tests only?

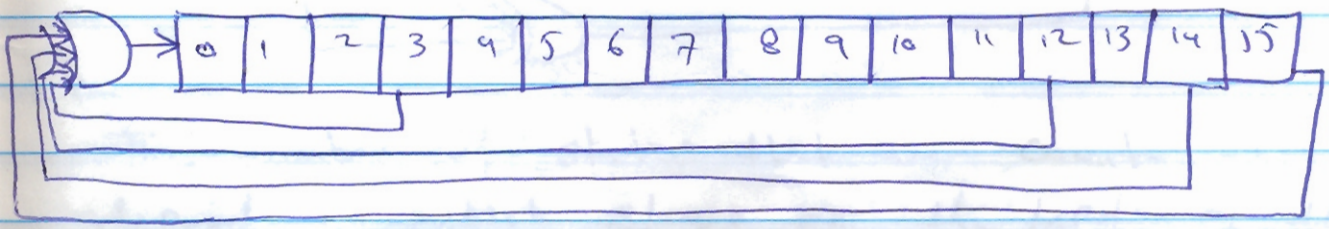



- if we use a linear feedback shift register (LFSR) which is a shift register with xor gates in test mode, and normal register in normal mode, then we can generate a larger number of tests depending on the location of the xor gates




LFSR

- It may be amazing if you know that if we fed back cells 3, 12, 14, and 15 using xor gates to the cell 0 in 16-bit register, then we can get the maximum length LFSR. This LFSR will rotate through all of the possible 65535 possible outputs (output 0000...0 will block the LFSR)




(try this using the simulator).

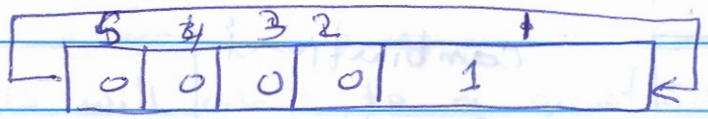
## ⊛ The Result Analyser

- we cannot store a complete set of expected outputs and so we must perform some kind of data compressio on the sequence of outputs to reduce them to a single number.

- The form of data compression used is signature analysis. A good circuit will produce one particular number in response to the entire sequence of test vectors.
- If there is a fault, then the number in the output register will be different from that caused by a good device.

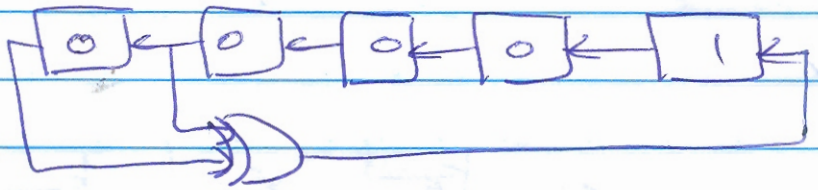
⊛ more about ~~[illegible]~~ LFSR

Ex: if we have 5-bit circular shift register with an initial value of 00001



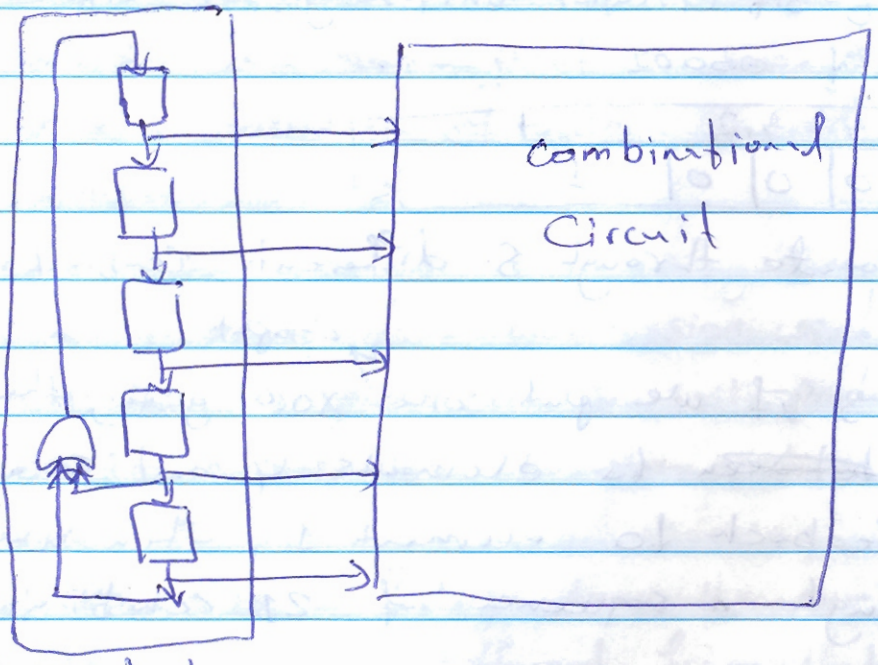

Then we will rotate through 5 different combinations.

But, for example, if we put one 2-input XOR gate, the inputs connected ~~between~~ to elements 4 and 5 and the output is fedback to element 1, then we will rotate through a sequence of 21 combinations




- The number of states that are counted through depends on which stages are the inputs of the XOR gate. And so, if we had made better choice, then we could have got a longer non-repeating sequence
- The best choice will count through 31 possible states ($2^5 - 1 = 31$ (00000 will lock-up the system)

Use of LFSR



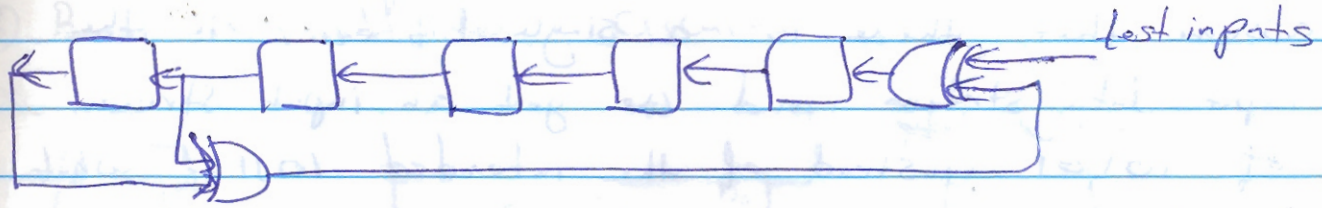

More about signature analysis

When we have a very large number of bits in the outputs, then it is not convenient to use scan path test alone to test these outputs. This problem can be solved through the use of signature analysis.

There are 2 types of signature analysers

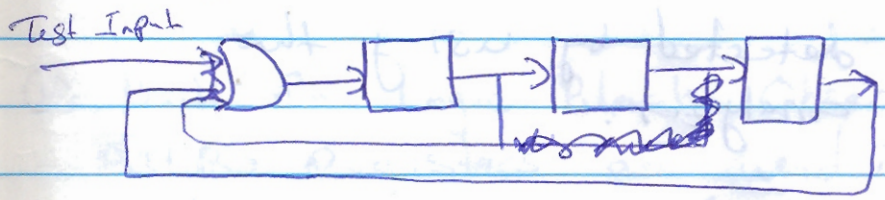
1. Single input signature register (SISR)

This is an LFSR with an additional input. The long stream of test data is fed into this input, and at the end of operation, the number which is left in the register is called signature or the syndrome




- good inputs will reach to a good signature
- any error in the test inputs will lead to different signature.
- sometimes, certain conditions of multiple error can give precisely the same signature as the correct data. (probability = $2^{-n}$)

Ex.




This signature analyzer is initialized to the all-zero state. This analyzer is fed with the data stream 10111, the digits arriving LSB first. What is the resulting signature.

Solution

| | | |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |

⇒ signature is **101**

* assume that there is a sigle bit error in the input data stream and we get an input stream of 10101 instead of the intended 10111. what will be the result signature

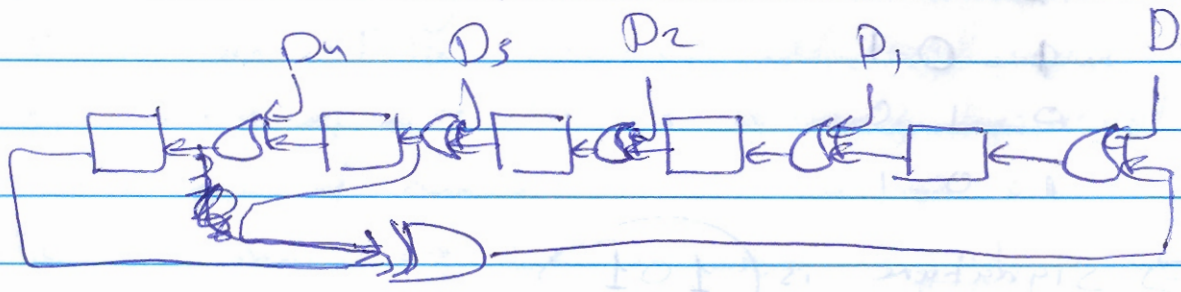
```
1 0 1
1 0 0
1 1 0
0 1 1
1 0 1
1 1 0
```

resulting signature is 110
expected " is 101 (error-free signature)

⇒ error is detected by using the signature analyzer.

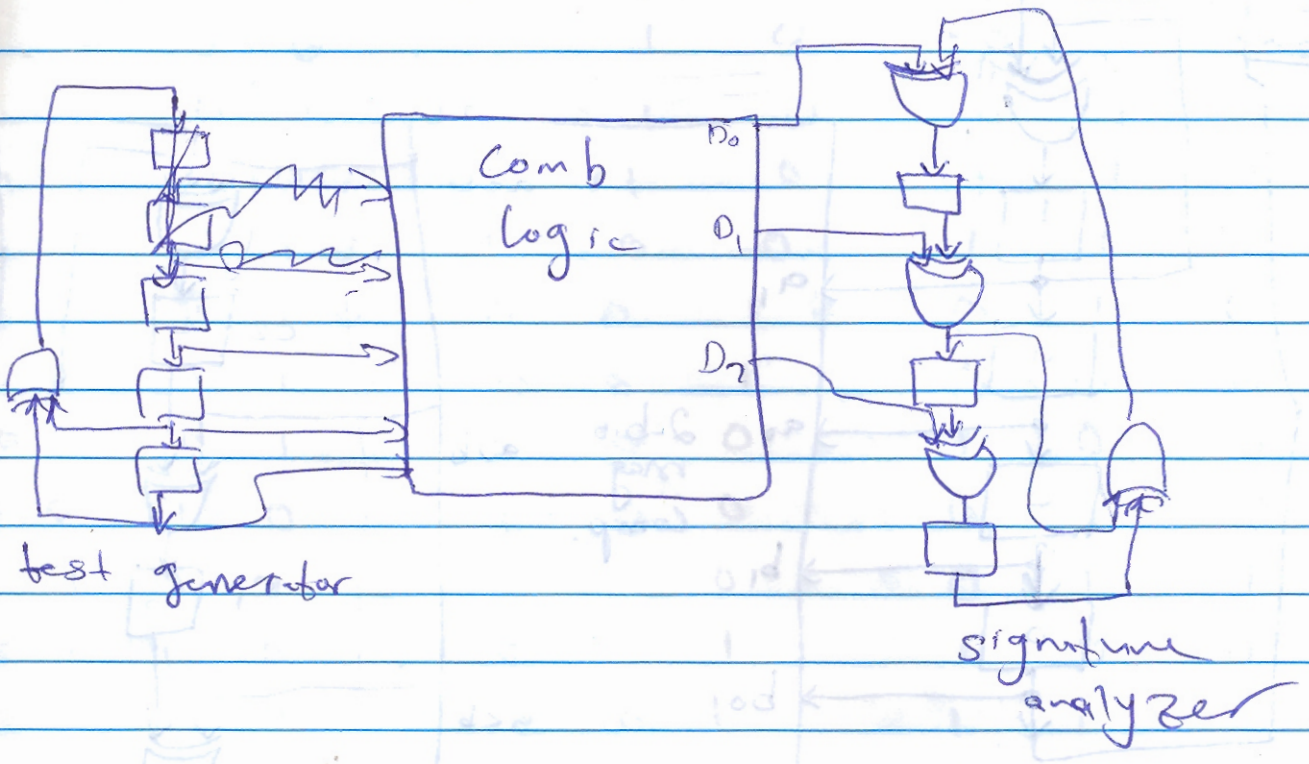
(2) Parallel Loading of signature analysers (Multiple input signature register MISR)

- sometimes we deal with parallel data not with a stream of serial test data. This is can be done with MISR



*

(*) Built in self test circuit




(*) Built In Logic Block Observation (BILBO)

BILBO Registers are used in two modes: normal mode and test mode.

In normal mode BILBO works as parallel input parallel output registers.

In test mode, BILBO has many functions: It works as scan path reg. to push initial data in the test generator and to push out the signature stored inside the signature analyser. also it works as test generator for the inputs of the system, and signature analyzer for the output of the system.