BIRZEIT UNIVERSITY

Faculty of Engineering and Technology
Electrical and Computer Engineering Department

ENCS 234 Digital Systems

Summer Semester 2023/2024

Course Catalog

3 Credit hours (3 h lectures).

Number Systems. Boolean Algebra. Logic gates. Simplification of Boolean functions. Design of Combinational Logic. Sequential logic: latches, flip-flops, state diagrams and excitation tables. Registers, counters, and sequential systems, derivation of state tables and state diagrams. Memory units. Introduction to Programmable Logic Devices, and Hardware Description Languages.

Text Book(s)

Title	Digital Design
Author(s)	M. Morris Mano and Michael D. Ciletti
Publisher	Prentice Hall
Year	2012
Edition	5th Edition

References

Books	1. Fundamentals of Logic Design, Charles Roth, Jr., Brooks Cole. 7th Edition, 2013 2. Digital Design: Principles and Practices, John F. Wakerly, 4th Edition, Prentice Hall.2005

Instructors

Instructor	**Abdallatif Abuissa, Aziz Qaroush**
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Office Hours
Check Ritaj for the office hours of your instructors

Prerequisites	
Prerequisites by course	COMP230 or COMP132 or COMP142

Topics	**Chepters in Text**
Binary Systems	Chapter 1
Boolean Algebra and Logic Gates	Chapter 2
Gate-Level Minimization	Chapter 3
First Exam	
Combinational Logic	Chapter 4
HDL for combinational logic	
Synchronous Sequential Logic	Chapter 5
Second Exam	
Registers and Counters	Chapter 6
HDL for Sequential Logic	

Mapping of Course Objectives to Program Outcomes	**Assessment method**
1. Understand and practice number representation and conversion in different number systems and perform different arithmetic operations in different number systems.	Exams
2. Recognize, manipulate, simplify, and implement Boolean functions using Boolean algebra theory, K-map and Tabulation Method.	Exams
3. Analyze and design combinational logic circuits using Boolean algebra and logic gates and logic blocks.	Exams
4. Analyze and design computer arithmetic units (full adder, half adder, subtractor, and multiplier).	Exams
5. Analyze and design sequential logic circuits.	Exams
6. Use the Verilog Hardware Description Language (HDL) and use its different modeling techniques for combinational and sequential circuit description.	Assignments

ABET Outcome
a: Ability to apply mathematics, science and engineering principles. c: Ability to design a system, component, or process to meet desired needs. e: Ability to identify, formulate and solve engineering problems.

Evaluation		
Assessment Tool	**Expected Due Date**	**Weight**
First Exam (Ch1-Ch3)	TBA	20 %
Second Exam (Ch4- ch5)	TBA	25 %
HDL Assignments	TBA	10 %
Final Exam	According to the University final examination schedule	45 %

Policy	
Attendance	Attendance is very important for the course. In accordance with university policy, students missing more than 10% of total classes are subject to failure. Penalties may be assessed without regard to the student's performance. Attendance will be recorded at the beginning or end of each class.
University Policies	Academic honor policy will be enforced, so please read the (honor code). Cheating will not be tolerated, but working together is encouraged
Exams	All exams will be CLOSE-BOOK; necessary algorithms/equations/relations will be supplied as convenient. The date of the Exams will be scheduled later.

ميثاق شرف الأمانة الأكاديمية

بموجب التسجيل في هذا المساق يلتزم الطالب باحترام أنظمة وقوانين الجامعة وخاصة تلك المتعلقة بالأمانة العلمية وعدم الغش .ويتحمل الطالب مسئولية ذاتية، أدبية وقانونية، عن المحافظة على الأمانة العلمية وذلك بالامتناع عن الغش في الامتحانات والوظائف والتقارير، وعدم السماح لغيره من الطلاب بأن ينقلوا عنه في الامتحانات والوظائف والتقارير.

يستوجب الغش أو محاولة الغش التوبيخ والإجراءات القانونية المنصوص عليها في تعليمات الأمانة الأكاديمية التي أقرها مجلس الجامعة بتاريخ 5 تموز 2006 وتشمل ما يلي:

1. **العقوبة الأكاديمية: يقررها مدرس المساق وقد تصل إلى علامة رسوب في المساق.**
2. **العقوبة التأديبية: تقررها لجنة النظام في الكلية وقد تصل إلى الفصل المؤقت أو النهائي من الجامعة.**

بموجب تسجيلي في هذا المساق واستلامي لهذا الميثاق أتعهد أمام الله أن أحافظ على الأمانة الأكاديمية بأن أمتنع عن الغش، وأن لا أتسامح مع أي محاولة للغش من قِبل الآخرين.