



DEPARTMENT OF COMPUTER SYSTEM ENGINEERING

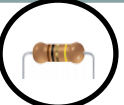
Digital Integrated Circuits - ENCS333

Dr. Khader Mohammad

Lecture #1- Circuits & Layout

- Review: Basic R, L, and C
- IC Manufacturing and Design Metrics CMOS -Ch1 Sec 1.3, Ch2 Sec 2.2

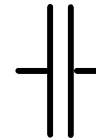
Basic Elements of Electronic Circuits

Transistor – is the switch		
Diode – is the rectifier		
Resistor - slows down electricity		
Capacitor - stores electricity		
Inductor - determines the magnitude of the electromagnetic force		
Connecting them with interconnects, an IC is obtained.		

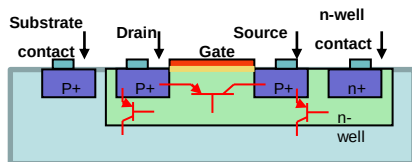
*The elements, being prepared by discrete technology, are shown.

Types of IC Elements

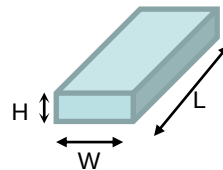
Useful



Parasitic

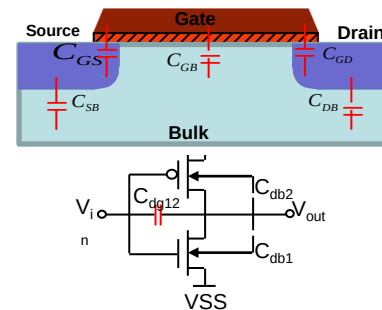


Bipolar Transistors

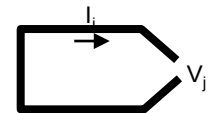
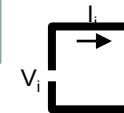


$$R = \frac{\rho L}{HW}$$

Resistances



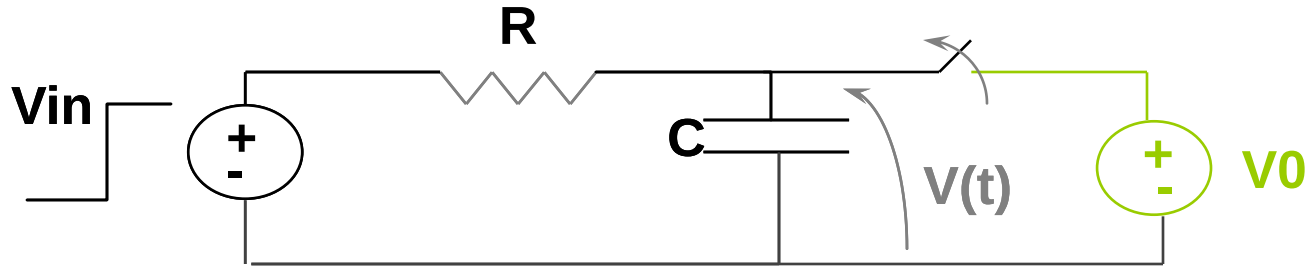
Capacitances



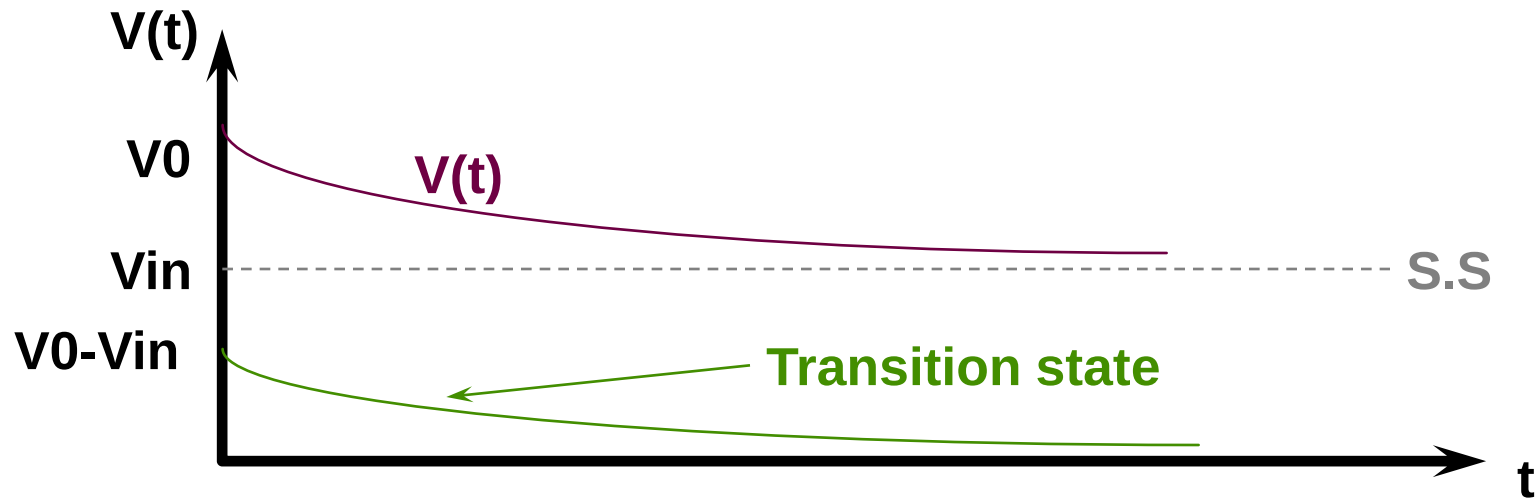
$$L_{ij} = \frac{\mu}{4\pi} \cdot \frac{1}{a_i a_j} \cdot \frac{1}{|I_i|} \oint_{\text{loop}_i} \oint_{\text{loop}_j} \frac{1}{r_{ij}} d\mathbf{l}_i d\mathbf{l}_j da_i da_j$$

Inductances

Line model (RC Model)



- $$V(t) = V_0 e^{-t/rc} + V_{in} (1 - e^{-t/rc})$$



Interconnect Parasitics

- Parasitic = unwanted natural electrical elements
- Metal Resistance
 - metals have a linear resistance and obey Ohm's law
 - $V = IR$
 - generate parasitic interconnect resistance, R_{line}

$$R_{line} = \frac{l}{\sigma A} = \frac{\rho l}{A}$$

$$- A = wt$$

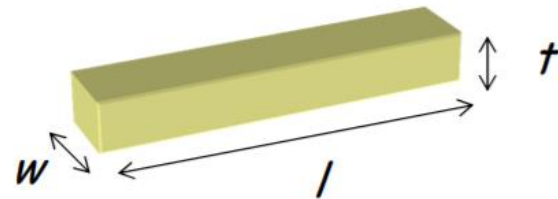
- ρ = resistivity, σ = conductivity

- defined by **sheet resistance**

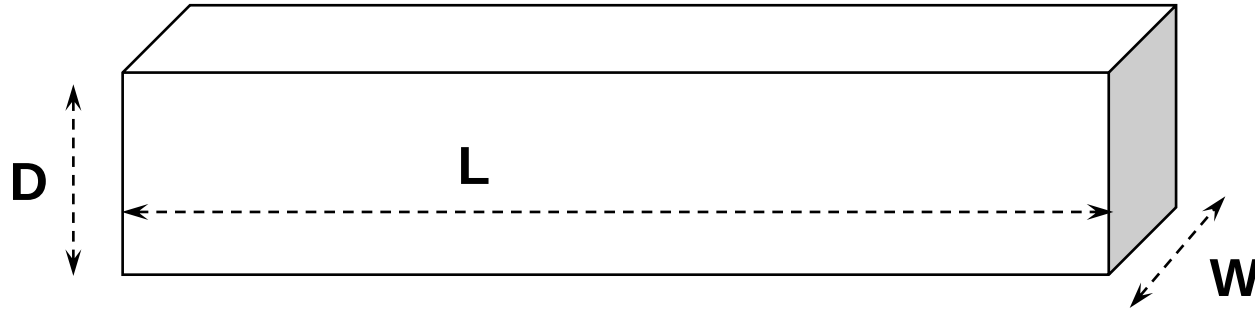
$$R_s = \frac{1}{\sigma t} = \frac{\rho}{t}, \text{ resistance per unit square [ohms, } \Omega \text{]}$$

$R_{line} = R_s$
when
 $l = w$

$$R_{line} = R_s \frac{l}{w}, R_s \text{ determined by process, } l \text{ \& } w \text{ by designer}$$



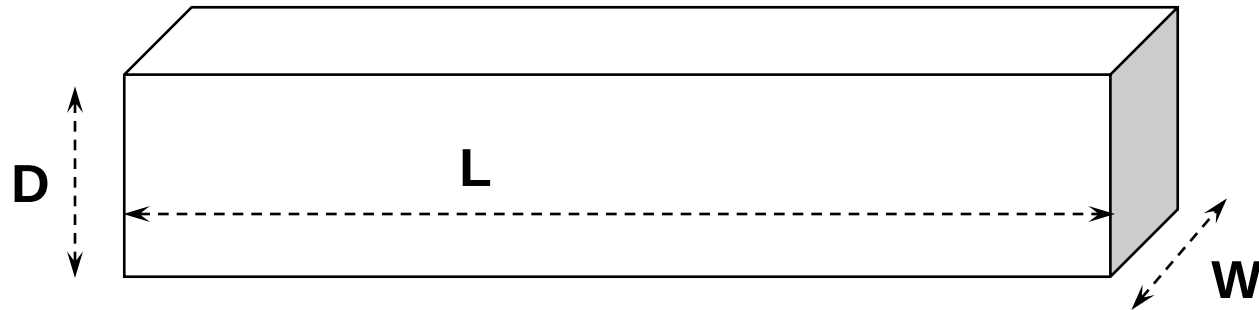
Line Resistance Simple Model



$$\underline{R = \text{Rho} * L / (W * D)}$$

- “D” is a process fixed number per layer
- We can set the Length “L”, and Width “W” of each segment
- This model does not include any temperature effect !!!

Segment Resistance Model



$$R = \text{Rho} * \text{SQR} * \text{Tscal}$$

Resistor per square
given in process
File (include D)

$\text{Len}/(\text{Wid} + \text{dlr})$
Number of Squares in
segment.

$1 + (t_e * (\text{Temp} - 25))$
Temperature Coefficient
Process file parameters
are given for "25C"

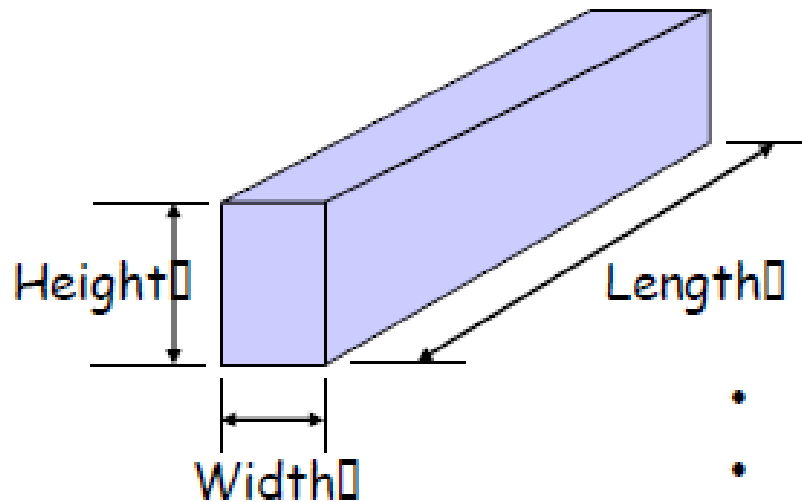
Segment Resistance Model

Example

- The process files has two models for each metal layer
 - Undegraded: A model for normal operation mode
 - Degraded: A model of the line after **100,000 Hours** of work under the **Worst RV** conditions

Metal layer	Rho	t_e	dIr
Metal 6 over Metal 5	4.22000e-05	5.53000e-01	-1.46800e-01
Metal 4 over Metal 3	8.35000e-05	3.64000e-01	-1.03000e-01
Metal 2 over Metal 1	1.08200e-04	2.92000e-01	-6.48000e-02

Wire Resistance



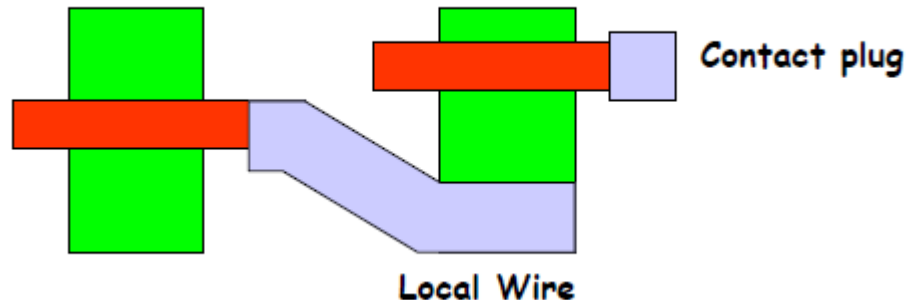
$$\text{resistance} = \frac{(\text{length} \times \text{resistivity})}{(\text{height} \times \text{width})}$$

- bulk aluminum $2.8 \times 10^{-8} \Omega\text{-m}$
- bulk copper $1.7 \times 10^{-8} \Omega\text{-m}$
- bulk silver $1.6 \times 10^{-8} \Omega\text{-m}$

- Height (Thickness) fixed in given manufacturing process
- Resistances quoted as Ω/square
- TSMC 0.18 μm 6 Aluminum metal layers
 - M1-5 0.08 Ω/square (0.5 μm $\times$ 1mm wire = 160 Ω)
 - M6 0.03 Ω/square (0.5 μm $\times$ 1mm wire = 60 Ω)

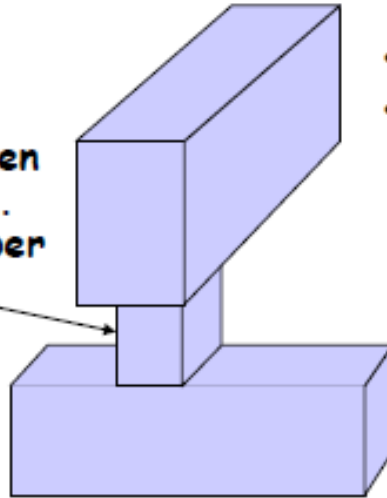
Local Interconnect

- Use contact material (tungsten) to provide extra layer of connectivity below metal 1
- Can also play same trick with silicided poly to connect gates to diffusion directly in RAMs
- Typically used to shrink memory cells or standard cells
- Contacts directly to poly gate or diffusion



Via Resistance

Vias made from Tungsten in Aluminum processes.
Vias are Copper in Copper processes



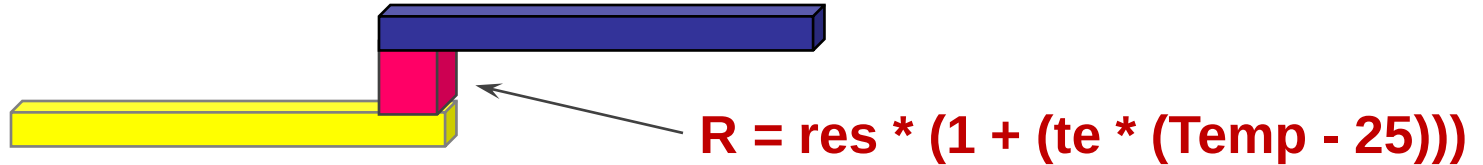
- Via resistance significant

- TSMC 0.18 μ m 6-A1

Diff-M1	11.0 Ω
Poly-M1	10.4 Ω
M2-M1	4.5 Ω
M3-M1	9.5 Ω
M4-M1	15.0 Ω
M5-M1	19.6 Ω
M6-M1	21.8 Ω

- Resistance of two via stacks at each end of M1 wire equivalent to about 0.1 mm wire ($\sim 20 \Omega$)
- Resistance of two via stacks at each end of M6 wire about the same as 1 mm narrow M6 wire ($\sim 60 \Omega$)!!!
- Use multiple vias in parallel to reduce effective contact resistance
- Copper processes have lower via resistance

Via Resistance Model



te, res : Are process file parameters
given for a specified Via model

Parasitic Line Capacitances

- Capacitor Basics

- $Q = CV$, C in units of Farads [F]

- $I = C \, dV/dt$

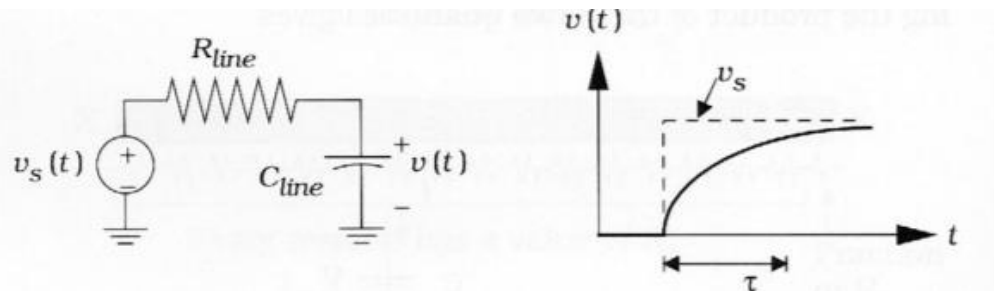
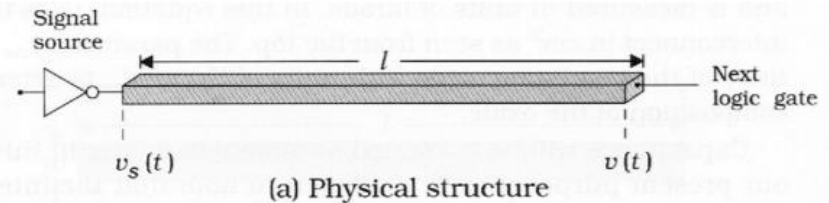
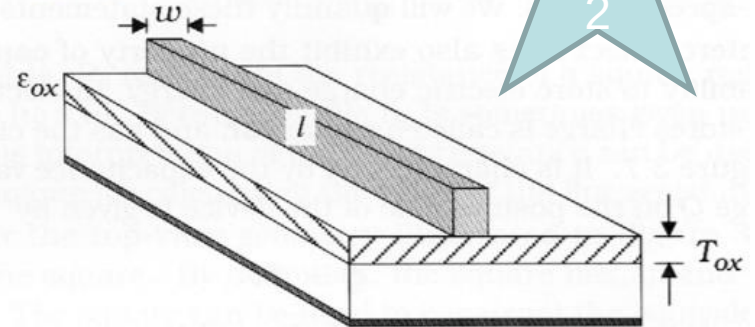
- Parallel plate capacitance

- $C_{\text{line}} = \frac{\epsilon_{\text{ox}} w l}{t_{\text{ox}}} \text{ [F]}, w l = \text{Area}$

- $\epsilon_{\text{ox}} = \text{permittivity of oxide}$

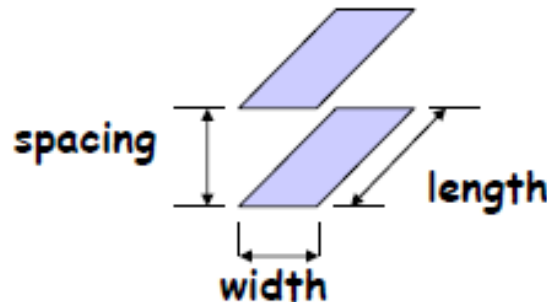
- RC time constant of an interconnect line

- $\tau = R_{\text{line}} C_{\text{line}}$



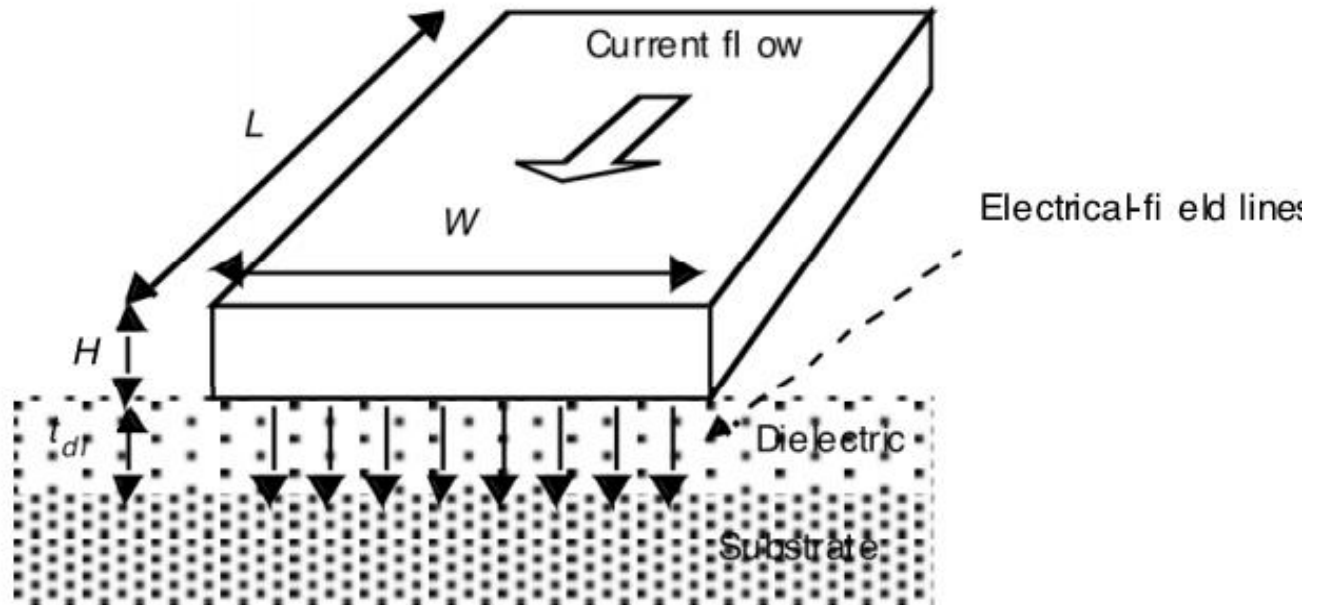
Capacitance Scaling

$$\text{parallel plate capacitance} \propto \frac{\text{width}}{\text{spacing}} \times \text{length}$$



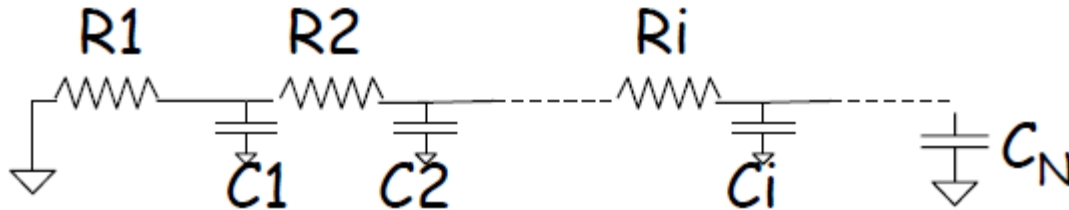
- Capacitance/unit length ~constant with feature size scaling (width and spacing scale together)
 - Isolated wire sees approx. 100 fF/mm
 - With close neighbors about 160 fF/mm
- Need to use capacitance extractor to get accurate values

Capacitance: The Parallel Plate Model



$$C_{int} = \frac{\epsilon_{di}}{t_{di}} WL$$

RC Delay Estimates

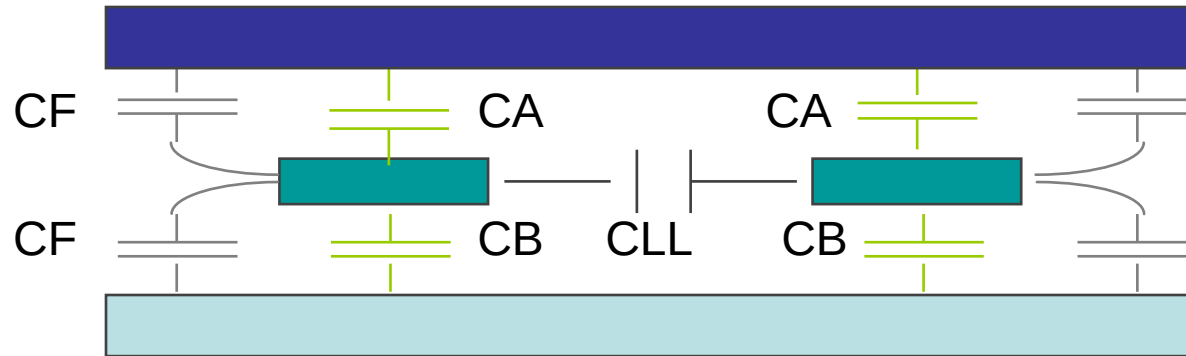


Penfield-Rubenstein model estimates:

$$\text{Delay} = \sum_i \left(\sum_{j=1}^{j=i} R_j \right) C_i$$

Capacitance

Interconnect Capacitance



CLL Line to Line Capacitance.

CA, CB Capacitance to Other Plane.

CF Fringing Capacitance.

Solving a speed path.

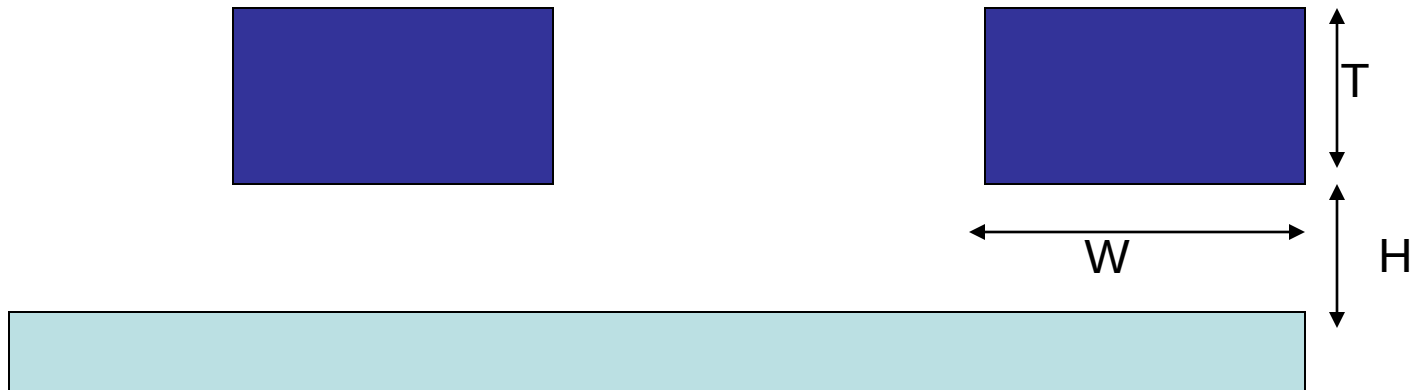


What happened to R?

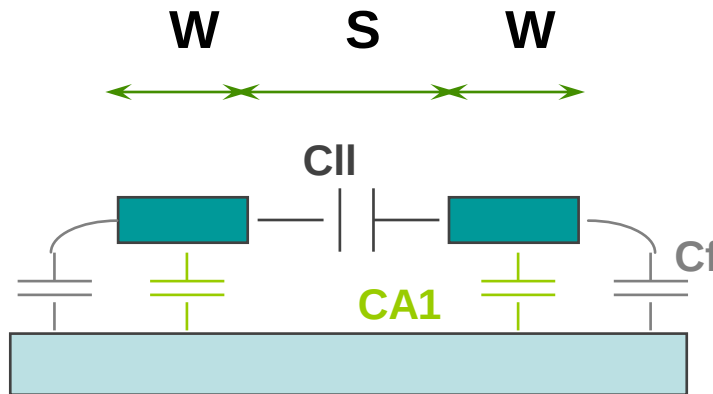
What happened to C?

Fringe Capacitance

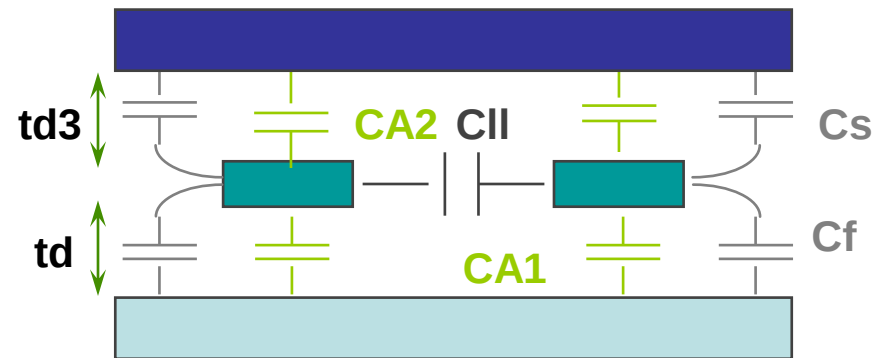
- As the process dimensions get smaller, the interconnect ratio (T/W) and (T/H) increases, since T has to increase to get a better resistance. Therefore Fringe capacitance becomes more and more significant.



Line Capacitance Calculation



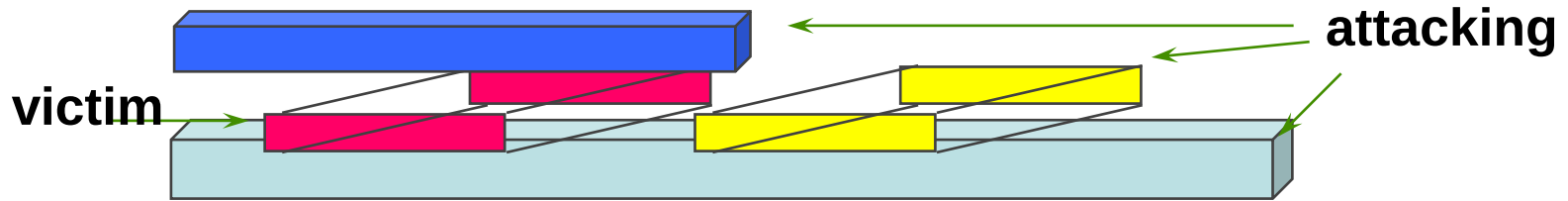
Pizza model



Sandwich model

$$C_{total} = Ca1 + Ca2 + 2 \cdot CII + 2 \cdot Cf + 2 \cdot Cs$$

Cross Capacitance

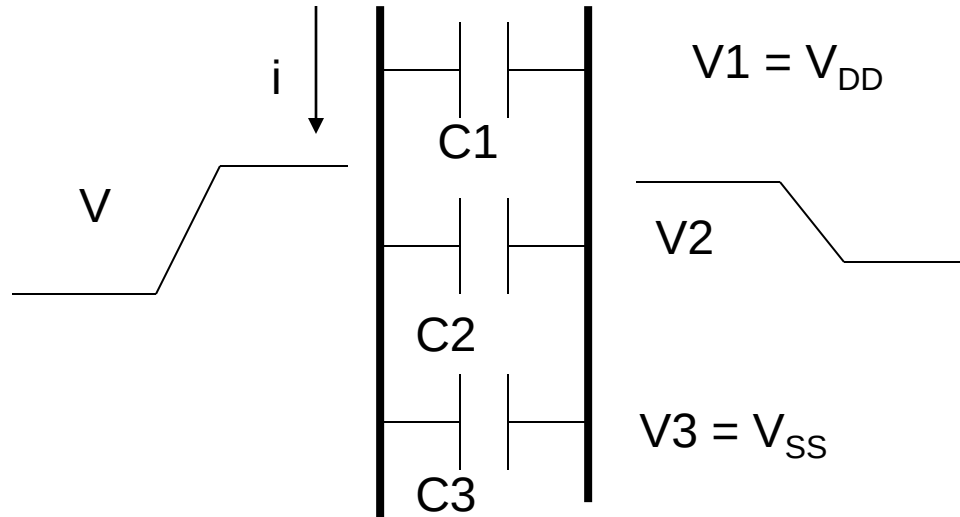


- Cross Capacitance is any capacitance between nets, which are non DC nets.
- In the worst case all the capacitance between nets can be cross capacitance.
- We call the signal that we are analyzing the **victim**, and all the signals that have cross capacitance to it we will call them **attacking** signals.

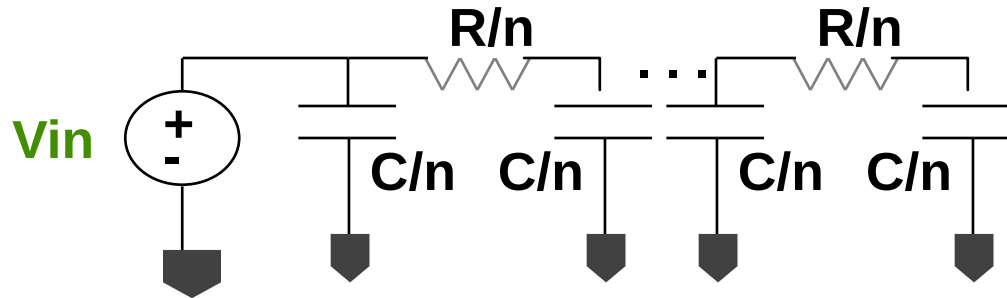
Cross Capacitance & Miller Effect

- Remembering the current-voltage equation for a capacitor
 $i(t) = C * dv(t)/dt$
- In case that the **attacking signal** is also switching, then the $dv(t)/dt$ is actually bigger or smaller than the DC case, depending on the switching directions of the victim and attacking signals.
- In verification tools we always calculate the voltage referenced to the Ground “Vss” which is a DC signal.
- We can see this effect as if the effective capacitance between the line and the Ground changes, this is called the **Miller Effect**.
- Miller Coefficient is the factor that we use to multiply the Xcap in order to model the Miller Effect.

Miller Coupling Mathematics

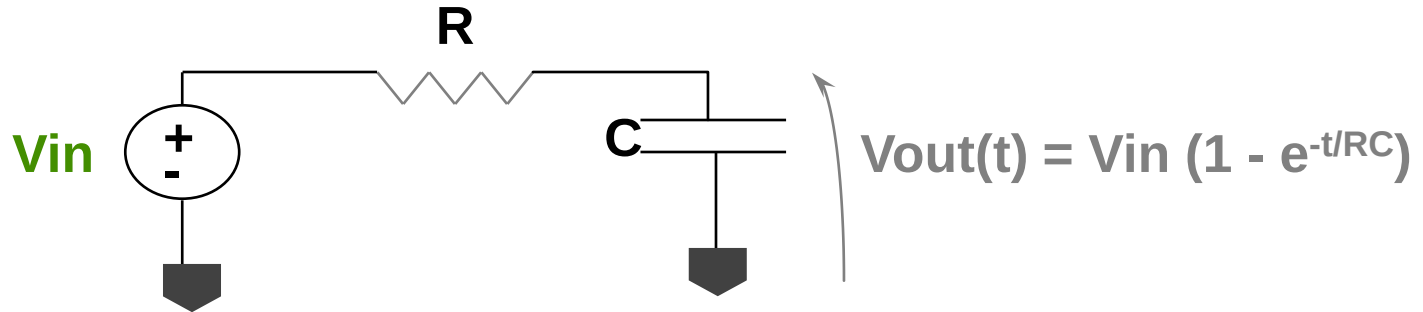


Distributed Line Model



- The distributed line model is a more accurate model which assumes that the line is built out of many segments, when each segment is modeled as a lumped RC model.
- For calculating the RC delay using the distributed model a simulation is needed

Lumped Line Model

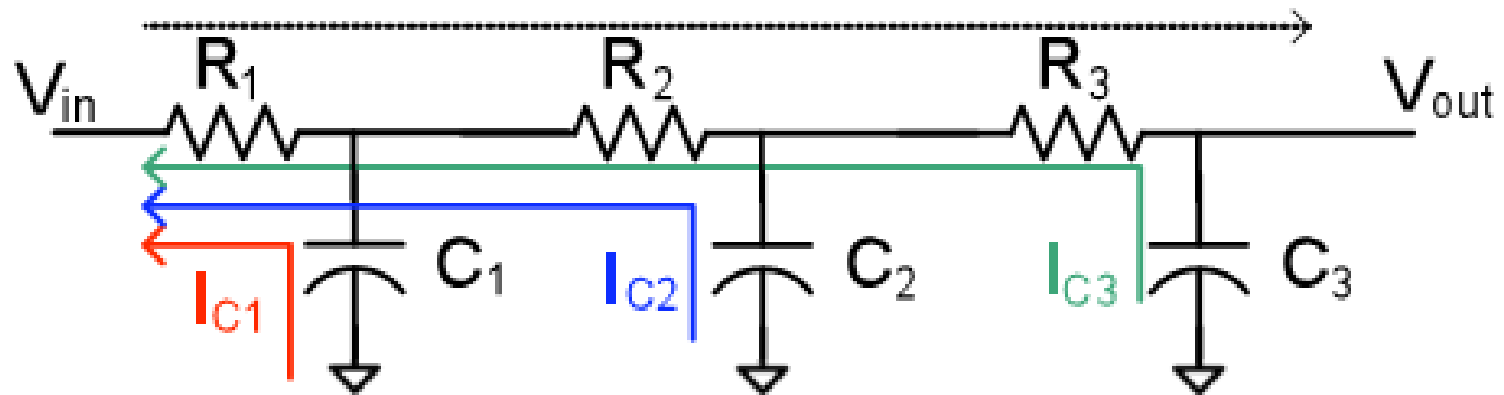


- A lumped model is a pessimistic one, which assumes that all the capacitance, line and load, is located at the end of the line, in other words that the driver “sees” the total load through the total line resistance.
- As the RC delay increases the lumped RC model is less and less accurate.

Classes of Parasitics

- **Capacitive**
- **Resistive**
- **Inductive**

Simplified Model: Elmore Delay



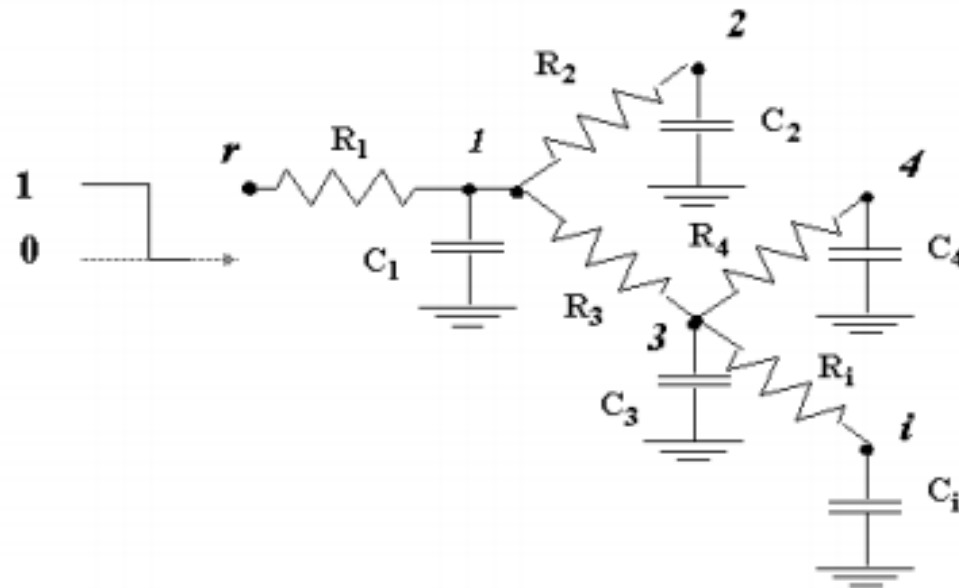
$$\tau_{Elmore} = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2 + R_3) C_3$$

Wire Delay Example

- In 0.18 μ m TSMC, 5x minimum inverter with effective resistance of 3 k Ω , driving FO4 load (25fF)
- Delay = Rdriver $\times$ Cload = 75 ps
- Now add 1mm M1 wire, 0.25 μ m wide
 - R_w = 320 Ω wire + 22 Ω vias = 344 Ω
 - C_w = 160fF

$$\begin{aligned}\text{Delay} &= R_{\text{driver}} \times \frac{C_w}{2} + (R_{\text{driver}} + R_w) \times \left(\frac{C_w}{2} + C_{\text{load}} \right) \\ &= 3\text{k}\Omega \times 80\text{fF} + (3\text{k}\Omega + 344\Omega) \times (80\text{fF} + 25\text{fF}) \\ &= 591\text{ps}\end{aligned}$$

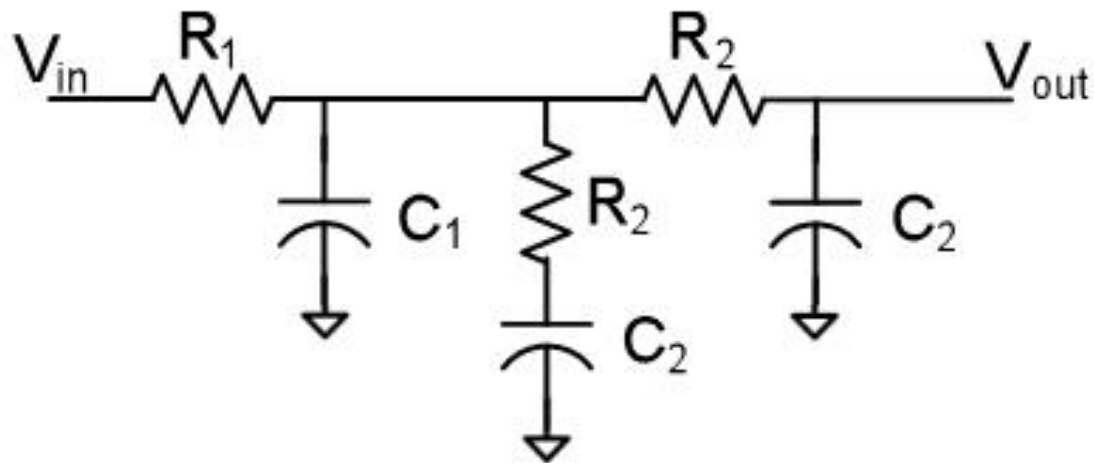
Elmore Delay - Extended



$$R_{ik} = \sum R_j \Rightarrow (R_j \in [path(s \rightarrow i) \cap path(s \rightarrow k)])$$

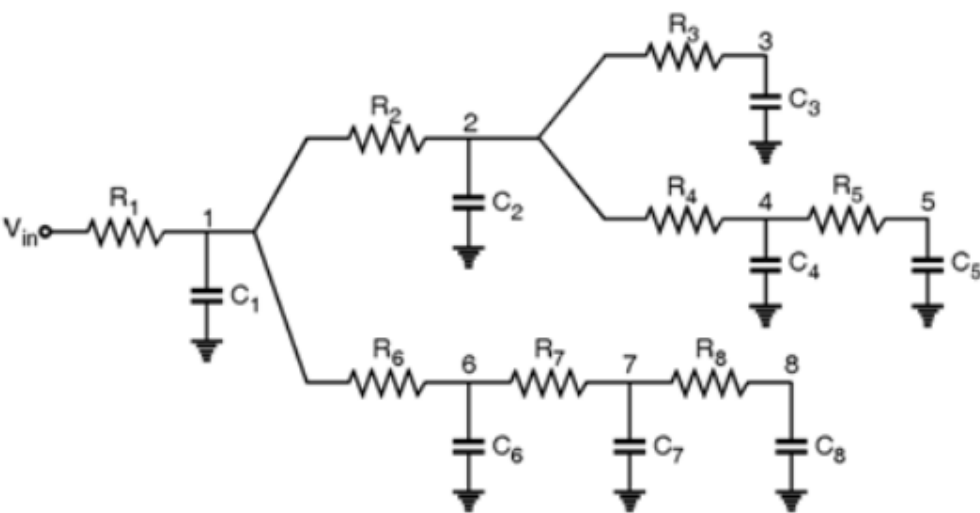
$$\tau_{Di} = \sum_{k=1}^N C_k R_{ik}$$

Another Elmore Delay Example



$$\tau_{Elmore} =$$

Consider RC network shown in Figure below connected in the form of RC segments.



RC tree network

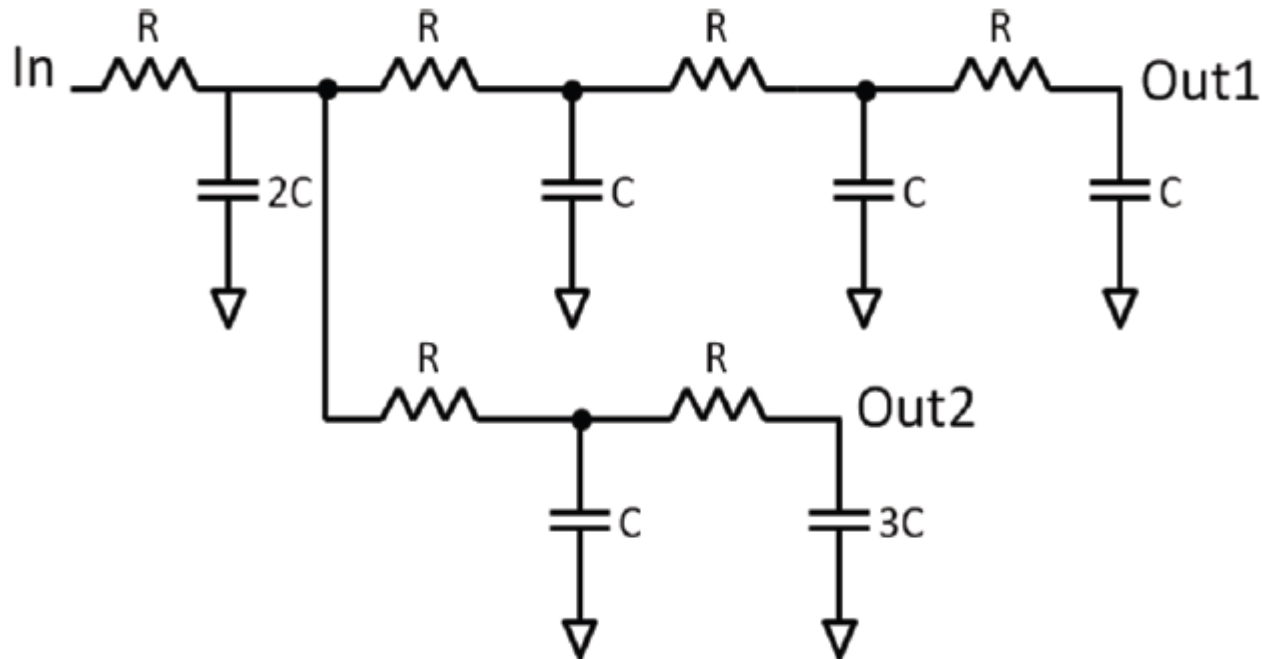
Now, here the Elmore delay at node 7 is calculated as,

$$\tau_{D7} = R_1 C_1 + R_1 C_2 + R_1 C_3 + R_1 C_4 + R_1 C_5 + (R_1 + R_6) C_6 + (R_1 + R_6 + R_7) C_7 + (R_1 + R_6 + R_7) C_8$$

In the same manner, the Elmore delay at node 5 is calculated as,

$$\tau_{D5} = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2) C_3 + (R_1 + R_2 + R_4) C_4 + (R_1 + R_2 + R_4 + R_5) C_5 + R_1 C_6 + R_1 C_7 + R_1 C_8$$

Calculate Elmore delay from In to out1 and from In to out2?

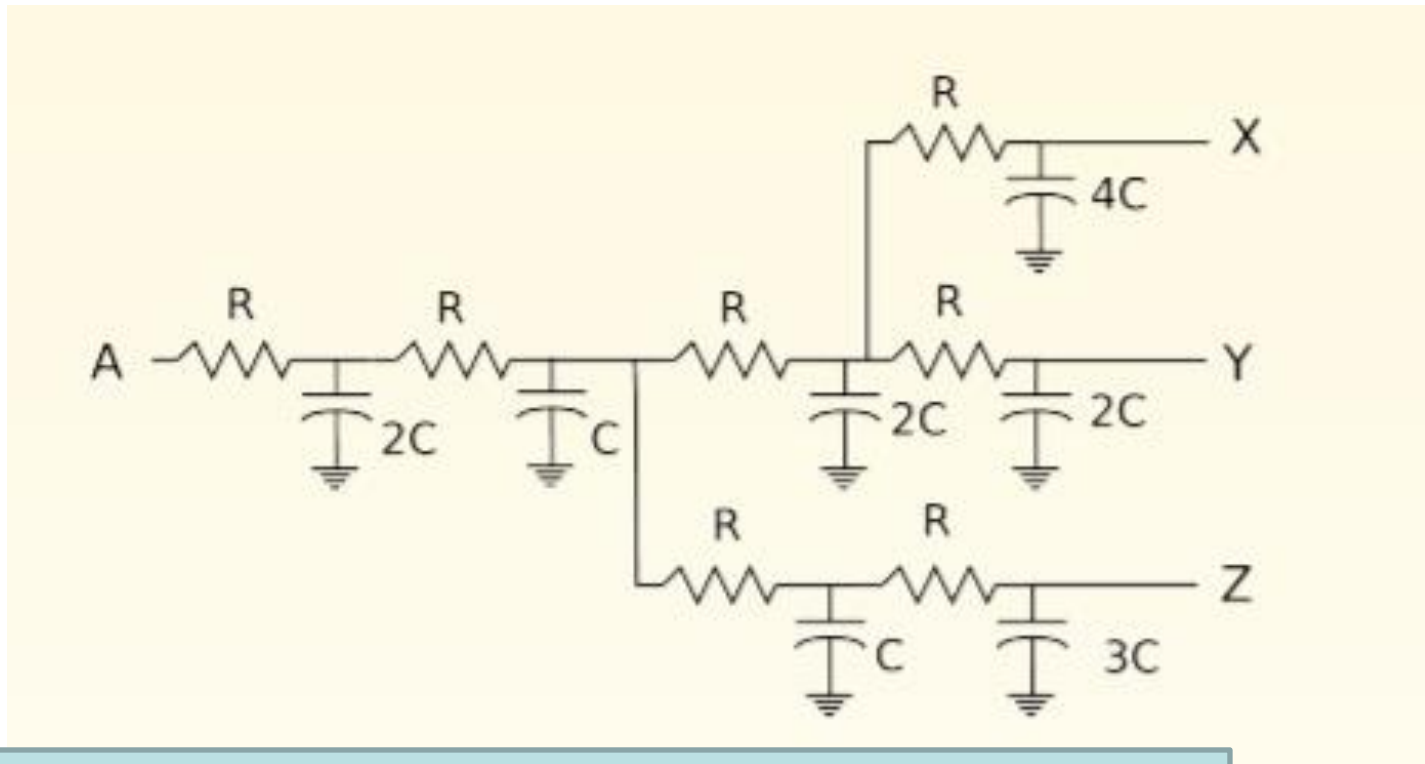


Solution:

Elmore to out1 is $15RC$

Elmore to out2 is $16RC$

Delay from A to Y



Resistance, Capacitance & Inductance

RESISTOR

$$V(t) = R * i(t) , \quad R = V / I = V / A = \Omega$$

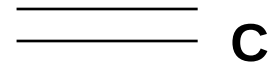


$$P(t) = I^2 R = V^2 / R , \quad W(t_0, t_1) = R \int_{t_0}^t I^2 \partial \tau = \frac{1}{R} \int_{t_0}^t V^2 \partial \tau$$

CAPACITOR

$$Q(t) = CV , \quad C = Q / V = A * Sec / V = FARAD$$

$$I(t) = \partial Q / \partial \tau = \partial (CV(t)) / \partial \tau = C \partial V / \partial \tau$$



$$V(t) = V(t_0) + 1/c * \int_{t_0}^t I(t) \partial \tau \quad P(t) = CV(t) \partial V / \partial \tau$$

INDUCTOR

$$\Phi(t) = L * I(t) , \quad L = \Phi / I = \text{weber} / A = V * Sec / A = \text{Henry}$$

$$V(t) = \partial \Phi / \partial \tau = \partial (LI) / \partial \tau = L * \partial I / \partial \tau$$



$$I(t) = I(t_0) + \frac{1}{L} \int_{t_0}^t V(t) \partial \tau , \quad P(t) = L * I * \partial I / \partial \tau$$