## Faculty of Engineering and Technology
## Department of Electrical and Computer Engineering

**Fall Semester 2024/2025**

# ENCS5331 Advanced Computer Architecture

**Course Syllabus**

**Dr. Ayman Hroub**

| References | |
|---|---|
| **Textbook** | • **Computer Architecture: A Quantitative Approach**, John L. Hennessy and David A. Patterson, Morgan Kaufmann, 6th Edition, 2019 |
| **Other References** | • **Computer Organization and Design: The Hardware/Software Interface**, John L. Hennessy and David A. Patterson, Morgan Kaufmann,6th Edition, 2021<br>• Research papers from the top conferences and journals<br>• Handouts/presentations provided by the instructor |

### Learning Outcomes

At the end of this course the student should be able to:

1. Understand superscalar processors
2. Understand the processor's memory hierarchy design options and performance optimization.
3. Understand parallel computing architectures, cache coherency and bus architectures
4. Understand data level parallelism (DLP) and thread-level parallelism (TLP)
5. Design Domain Specific Architectures (DSA's)
6. Understand the modern trends in computer architecture and technology
7. Understand the principles and technologies of in/near memory computing
8. Aware of computer architecture research community, top journals, top conferences, and research trends
9. Conduct research in computer architecture and write a research paper

| Main Topics |
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| • **Introduction and Motivation** |
| • **Review**<br>○ Out of Order Execution Processors<br>○ Compiler Techniques for Exploiting Instruction Level Parallelism<br>○ Dynamic Branch Prediction |
| • **Superscalar Processors** |
| • **Memory Subsystem**<br>○ Main Memory<br>○ Cache Hierarchy Organization<br>○ Cache Performance Evaluation and Optimization<br>○ Prefetching<br>○ Memory Controllers |
| • **Bus Architectures** |
| • **Parallel Processors and Thread Level Parallelism**<br>○ Motivation for Moving to Parallel Processors<br>○ Parallel Processers' Evolution and Taxonomy<br>○ Overview of Parallel Programming<br>○ On-chip Networks<br>○ Multicore Processor's Cache Hierarchy<br>○ Cache Coherence<br>○ Synchronization |
| • **Data Level Parallelism**<br>○ Vector Processors<br>○ Graphics Processing Units (GPUs) Architectures |
| • **Domain Specific Architectures (DSAs)**<br>○ Introduction to DSAs<br>○ DSAs Design Guidelines<br>○ **Case Study:** Deep Neural Networks Acceleration via DSA's |
| • **Virtual Memory** |
| • **Introduction to Near/In Memory Computing and Emerging Memory Technologies**<br>○ Motivation of Having in/Near Memory Computing<br>○ Technology Basics and Taxonomy |
| • **Introduction to Hardware Security** |

| Grading Scheme | |
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| **Assessment Type** | **Weight** |
| **Paper Review Assignments** | 10% |
| **Midterm Exam** | 20% |
| **Term Paper** | 30% |
| **Comprehensive Final Exam** | 40% |
| **Total** | **100%** |

## Teaching and Learning Methods

- Lectures, assignments, in-class activities, exams, and term paper.
- Mixture of modern learning methods, such as, inductive learning, flipped classroom, learning by project, etc.

| Additional Notes | |
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| **Assignments** | No late assignments |
| **Makeup Exams** | No makeup exam |
| **Office Hours** | Students are highly encouraged to utilize the instructor's office hours |
| **Honor Code** | Students are expected to abide by Birzeit University honor code on all aspects of their academic work. Please review that on Ritaj. Additionally, students are expected to follow the code of conduct for the course appended to this course outline. |
| **Code of Conduct** | By enrolling in this course, students agree to abide by a code of conduct that helps all participants gain the best results in a healthy and pleasant environment, this includes the following rules:<br>• Mutual respect is a must<br>• Students are expected to be in class on time<br>• Cell phones should be switched off<br>• Classroom should be very quiet<br>• Students are expected to stay in the classroom focusing and quiet, and not leaving the class room without asking the instructor's permission |