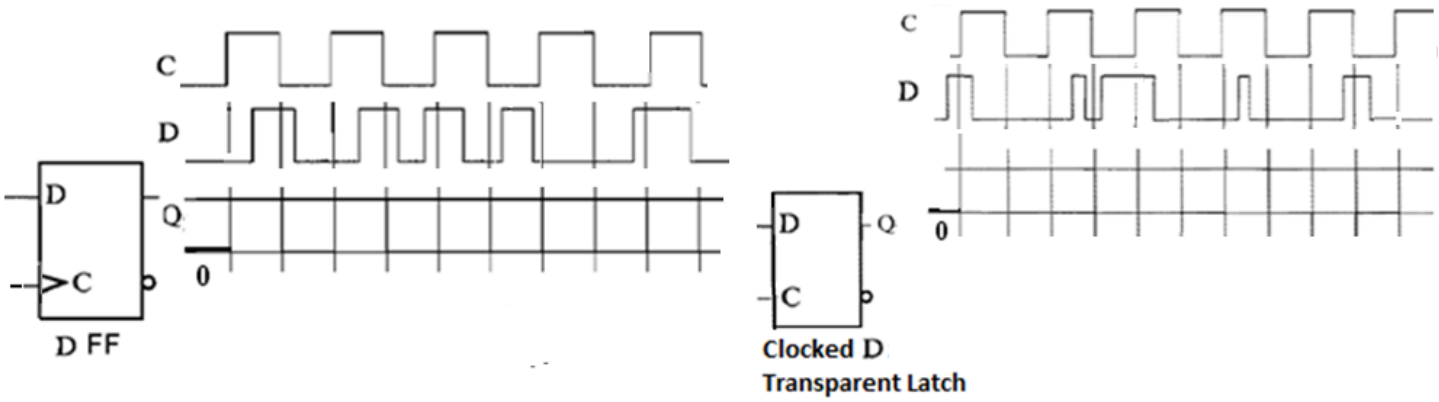
ENCS2340 | Section 2 | Fall 2024/2025
Chapter 5 - Extra Exercises

1. Carefully sketch the Q waveforms for each of the latches/flip flops below for the given input and clock signals. Assume that at all Qs were initially at 0.

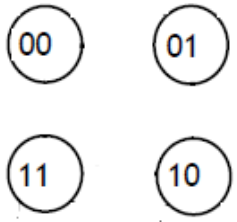


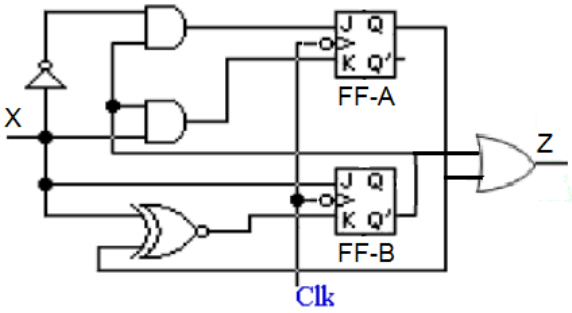
2. Analyze the sequential circuit in the figure opposite and answer the following questions:

a. Is the circuit Mealy or Moore? Justify.

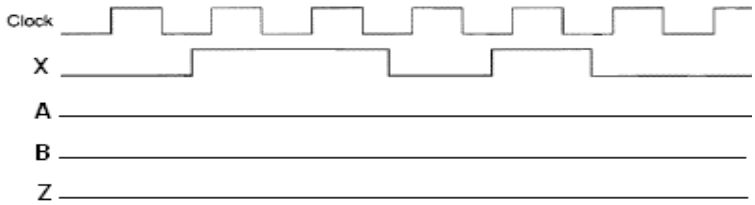
b. Present the circuit performance in the three following formats:

i. One-dimensional state table.
ii. Two-dimensional state table.
iii. State diagram. Must use the state layout shown opposite.





c. Use the state diagram to complete the following timing diagram by adding the waveforms for A, B, and Z. Assume that the circuit was initially at state AB = 00. Note that the FFs are **positive edge**-triggered.



3. A sequential circuit has two D flip flops A and B, two inputs x and y, and one output z. Behavior of the circuit is described by the following next-state and output equations:

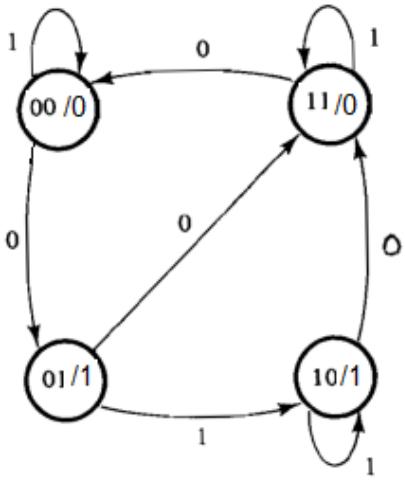
A(t+1) = Ay' + xy
B(t+1) = B'x' + xy'
z = A'(x+y)

a. Determine the circuit type: Mealy of Moore?. Justify your answer.

b. Draw the logic diagram of the complete sequential circuit. Assume that external inputs are available in both true and complemented forms.

c. Give the 1-D state table, and the state diagram using the same state layout specified for problem 2 above.

4. A finite state machine is specified by its state diagram shown below. The circuit uses positive edge triggered D flip flops which also have direct active-low S-R inputs.



a. Determine type (Mealy/Moore), number of external inputs, number of external outputs, state variables, and flip flops required.

b. Derive the 2-dimensional state table and then the 1-dimesional state table. Indicate state as AB (A is the MSB), inputs as X, and Output as Z.

c. Obtain K-map-optimized logic expressions for all outputs of the combinational circuit.

d. Give a complete circuit diagram for the sequential circuit.

e. Add an initialization input INIT such that a brief low (0) pulse on INIT puts the circuit asynchronously in the initial state AB = 01. Show all connections to the S-R inputs of the flip flops.

f. If we start at state AB = 00 and the input X is fixed at 0, after how many clock cycles do we return back to the same state (00)?

5. We would like to design a sequential circuit using D-type FFs that performs as an up/down binary counter. The circuit goes through the **down counting sequence** 6, 4, 2, 0, 6, 4, ... etc. when an input control input X is 0, and through the **up counting sequence** 0, 2, 4, 6, 0, 2, … etc. when the input control X is 1.

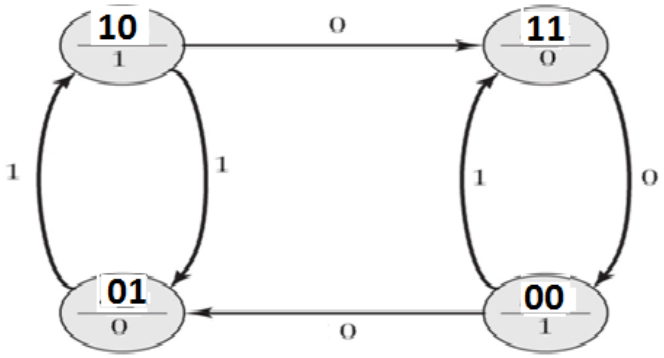
a. Show a complete state diagram indicating the effect of the input on all state transitions.
Note: indicate each counter state using both its decimal and binary values.

b. Derive the 1-dimensional state table. If a state does not occur as a next state, indicate its state vector as a don't care condition (X).

c. Use a K-map to derive an optimized sum of products (SOP) logical expression for the D input of the flip flop providing the MSB of the state vector.

6. Design a sequential circuit that implements the state diagram shown opposite using JK flip flops. Optimize the combinational logic part using K-maps and use AND, OR, NOT gates to implement it.

Note: If an input value is not specified on the state diagram, consider the corresponding target next sate as don't care.



7. We would like to design a Moore sequential circuit that dynamically detects the occurrence of the sequence 1100 on a single external input X. The output of the circuit Y will be normally 0, going to 1 only when the full required sequence is detected. Give:

a. A symbolic state diagram, marking states as A, B, C, etc, where A is the initial (Square 1) state.

b. The number of states, state variables, and flip flops required, and number of unused states if any.