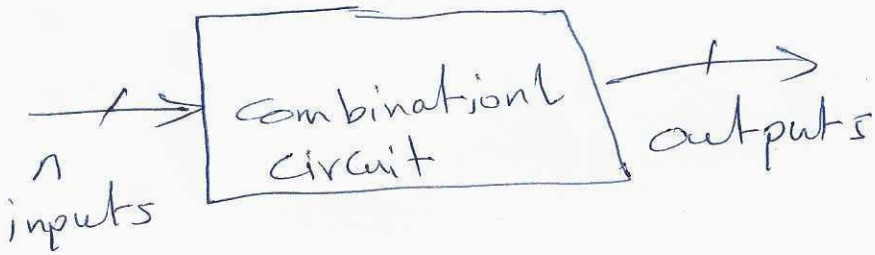
Chapter 5 :- Synchronous Sequential Logic

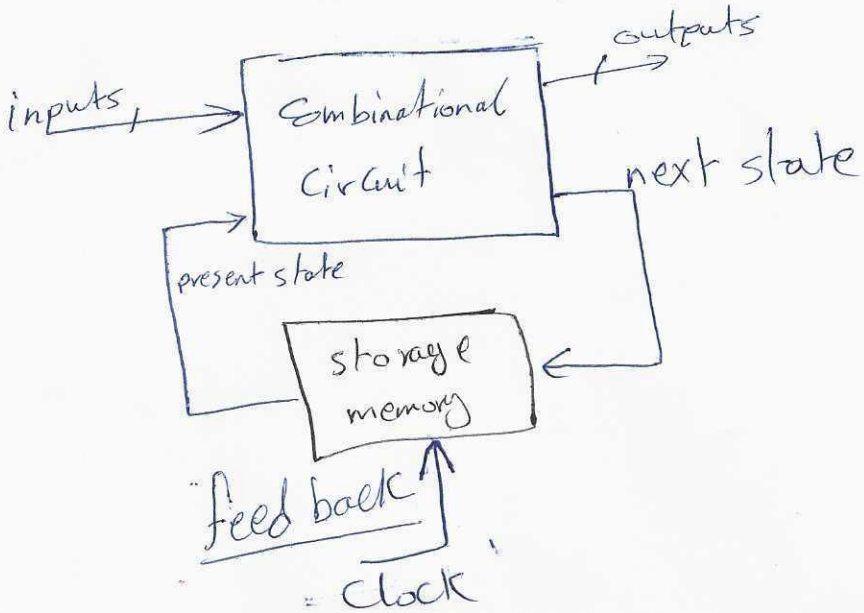
* Combinational Versus Sequential :-

1- Combinational Circuits :-

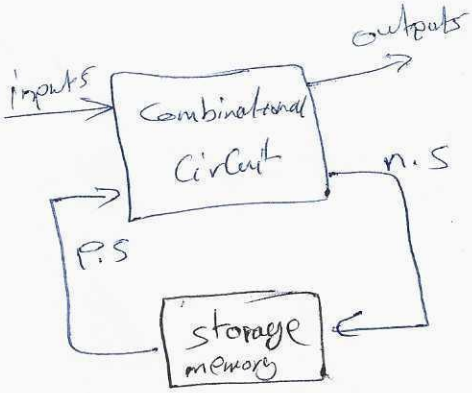


The outputs depend only on inputs

(2) Sequential Circuits :- The outputs depend on inputs and previous output (current or present state)

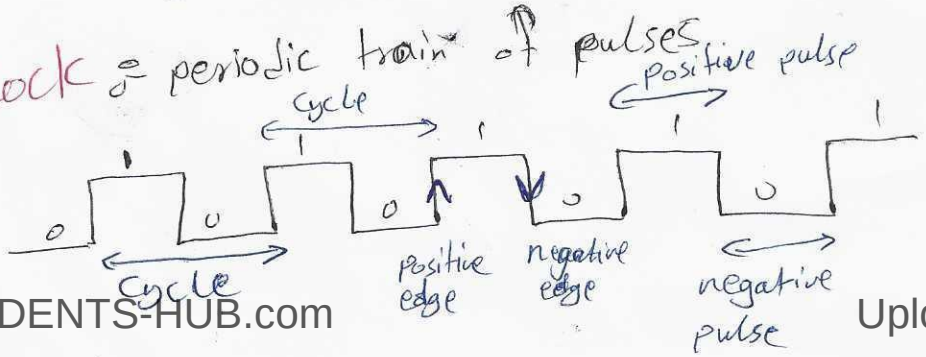


Synchronous



Asynchronous

* Clock :- periodic train of pulses



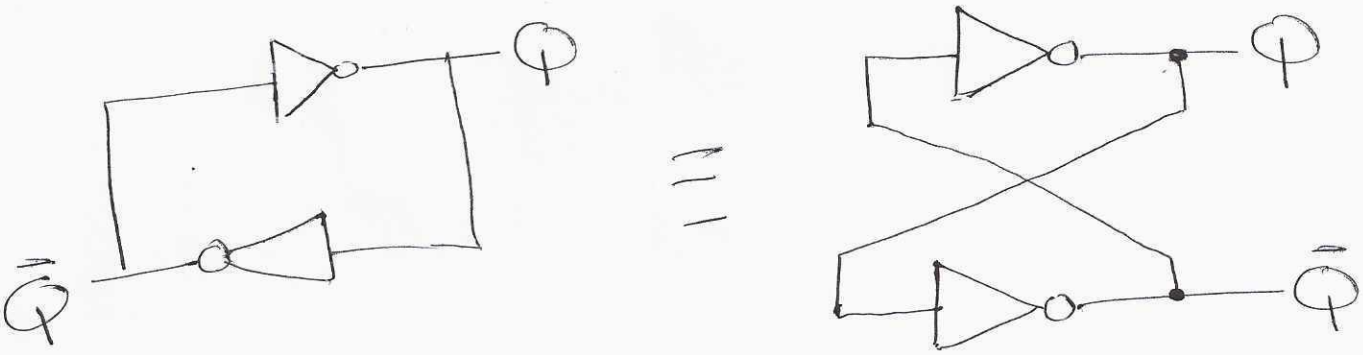
$$f = \frac{1}{T}$$

*Memory :- Can store and maintain binary state (0 or 1)

- Latches :- are level sensitive
- Flip-Flops :- are edge sensitive, built with Latches

* Latches :- store one bit of information

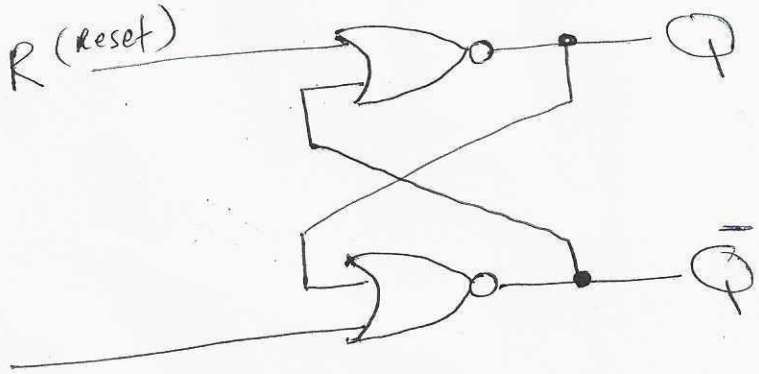
(1) Two inverters Latch



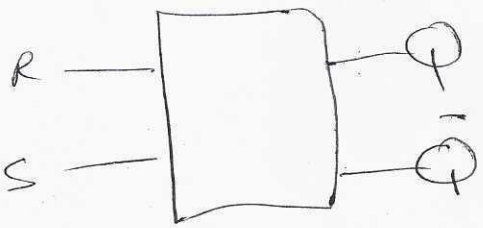
This circuit can't change the stored value

(2) SR Latch

SR Latch can be built using two NOR gates



Circuit diagram



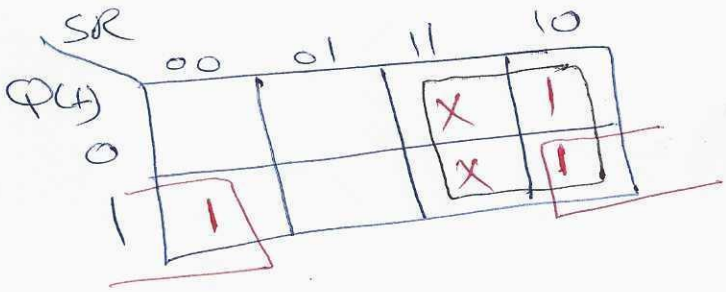
block diagram

Functional table

S	R	Q	$\bar{Q}$	
1	0	1	0	set state
0	0	1	0	
0	1	0	1	Reset state
0	0	0	1	
1	1	0	0	undefined

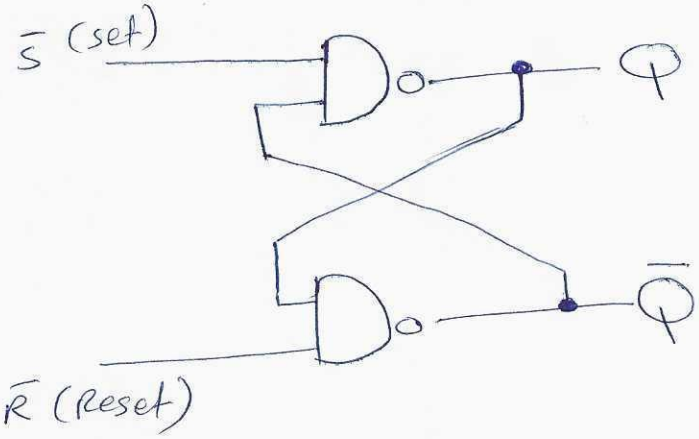
* Characteristic Equation of the SR latch

Q(t)	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Undefined
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	undefined

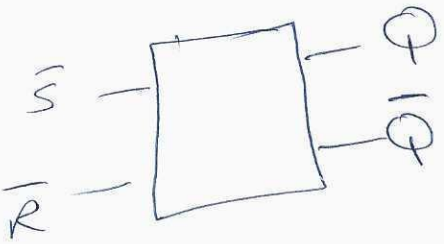


$$Q(t+1) = S + \bar{R}Q(t)$$

(3) $\bar{S}\,\bar{R}$ Latch with NAND gates



Circuit diagram

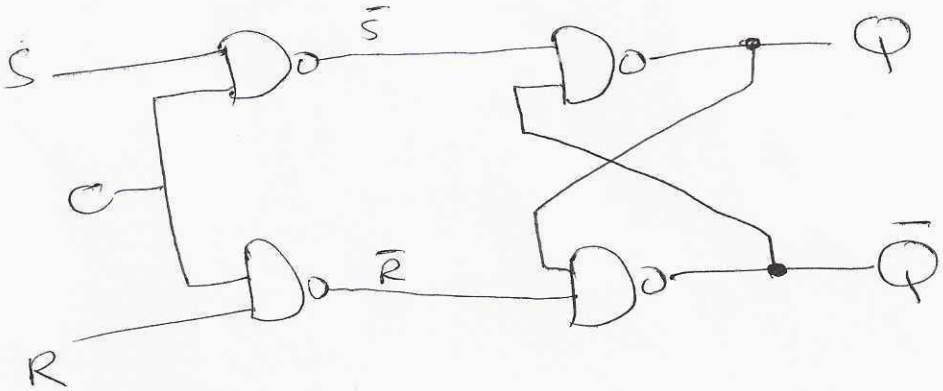


block diagram

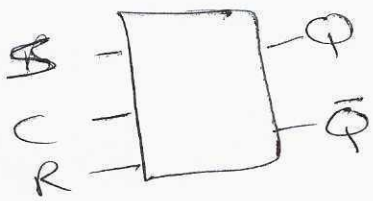
Functional table

$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	
0	1	1	0	set state
1	1	1	0	
1	0	0	1	Reset state
1	1	0	1	
0	0	1	1	undefined

(4) S R Latch with a clock input



Circuit diagram

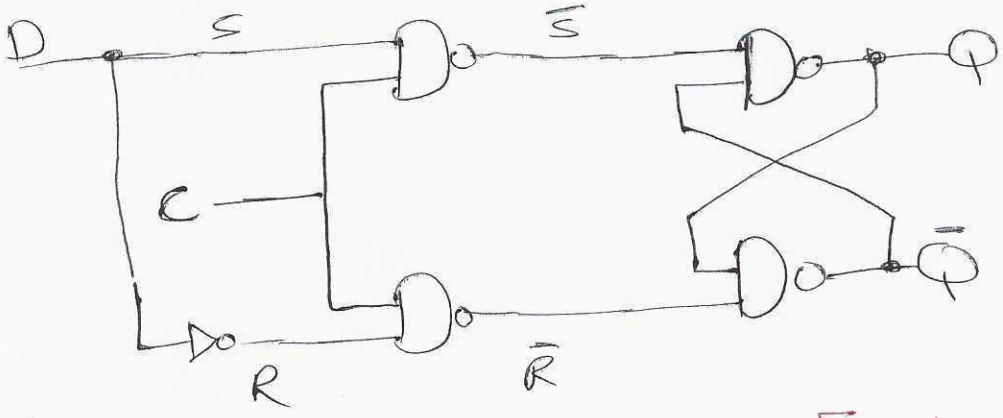


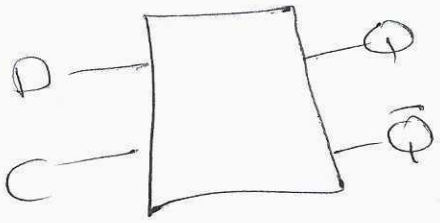
block diagram

Function Table

C	S	R	Q
0	X	X	No change
1	0	0	No change
1	0	1	0 Reset state
1	1	0	1 set state
1	1	1	undefined

(5) D latch with a clock input :-





Functional Table

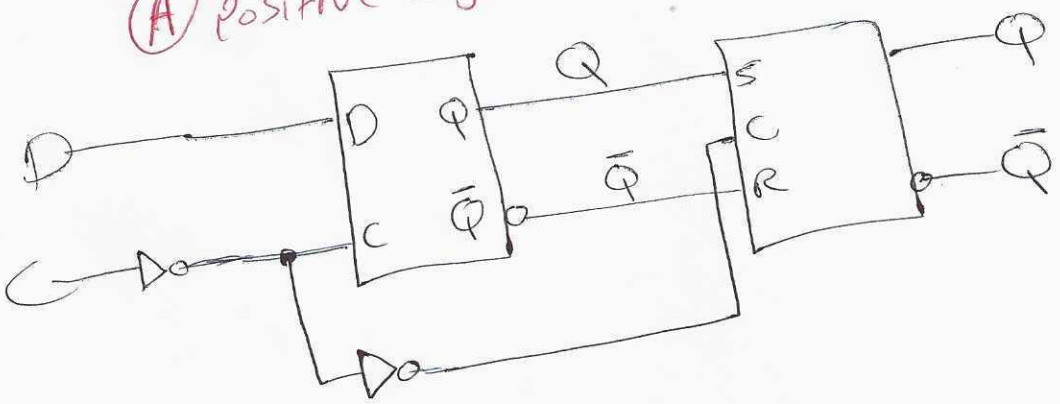
C	D	Q
0	X	No chang
1	0	0 Reset state
1	1	1 set state

* Flip-Flops :- sensitive to the edge of the clock
called edge-triggered memory element

① D Flip-Flop :- Built using two latches (master and slave)

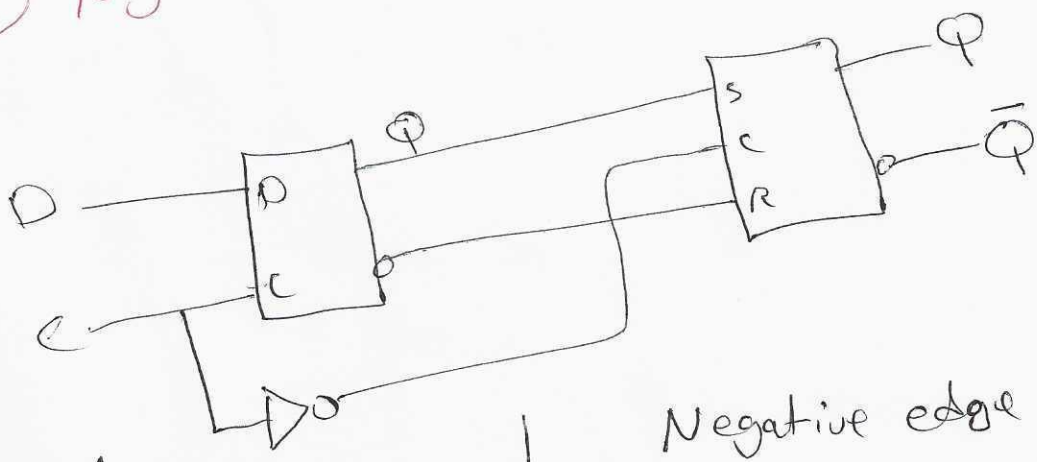
- master latch (D-type)
- slave latch (SR-type)

(A) positive edge



outputs changes when C changes from 0 to 1

(B) Negative edge



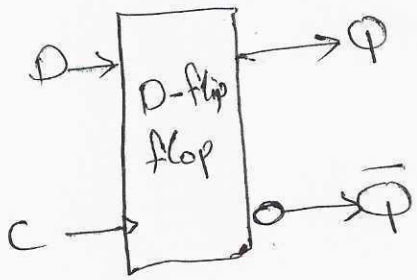
outputs Change when C changes form 1 to 0

Positive edge
Functional table

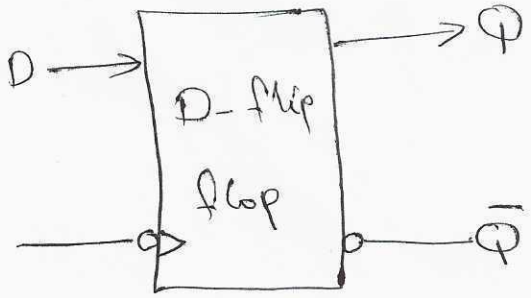
C	D	Q	$\bar{Q}$
↑	0	0	1
↑	1	1	0

Negative edge
Functional table

C	D	Q	$\bar{Q}$
↓	0	0	1
↓	1	1	0

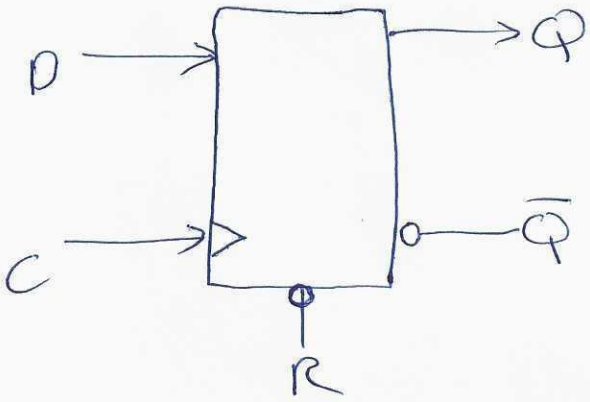


positive edge

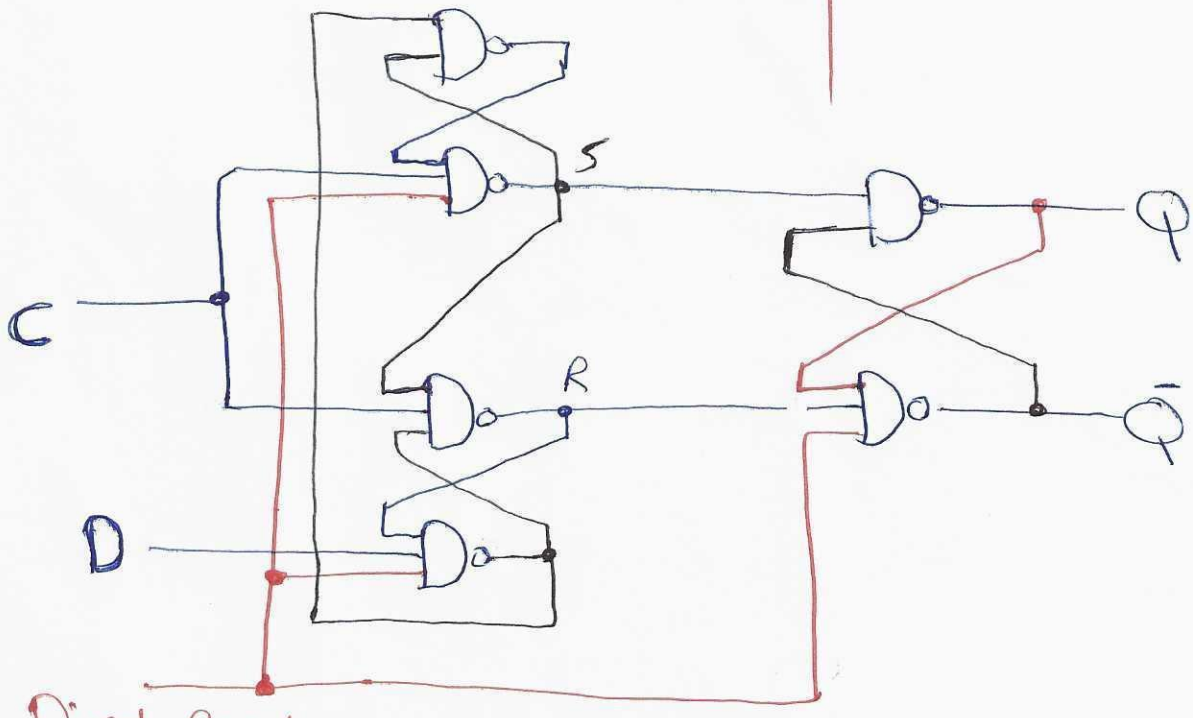


Negative edge

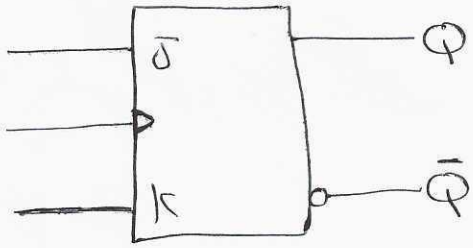
≠ D flip-flop with Asynchronous Reset



R	D	C	Q	$\bar{Q}$
0	X	X	0	1
1	0	↑	0	1
1	1	↑	1	0



* JK Flip flop



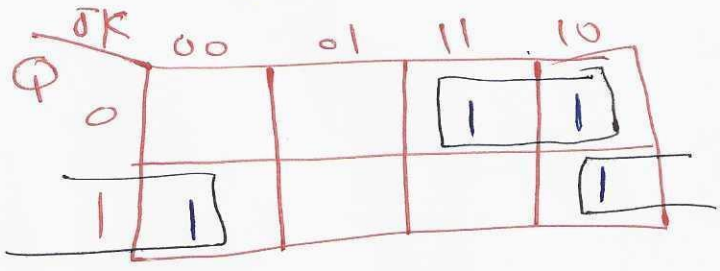
block diagram

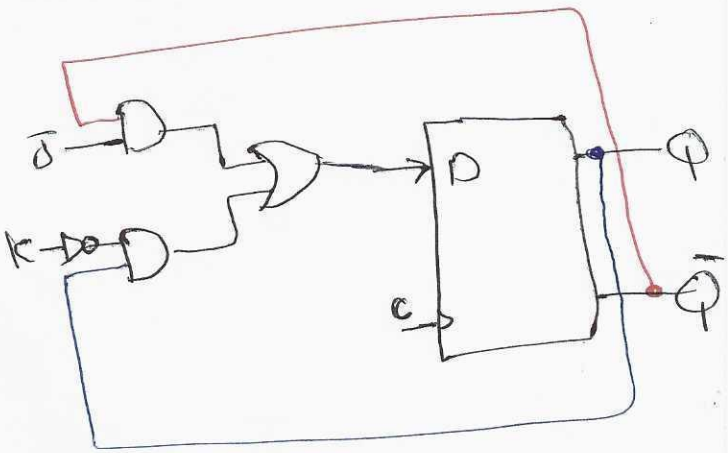
J	K	Q(t+1)	
0	0	Q(t)	no change
0	1	0	Reset
1	0	1	set
1	1	$\bar{Q}$(t)	inverse

Function table

Truth table

Q(t)	J	K	Q(t+1)	
0	0	0	0	no chang
0	0	1	0	Reset
0	1	0	1	set
0	1	1	1	complement
1	0	0	1	no change
1	0	1	0	Reset
1	1	0	1	set
1	1	1	0	complement



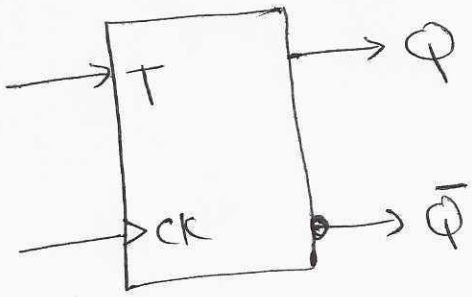


Circuit diagram

$$Q(t+1) = J\bar{Q} + \bar{K}Q$$

Characteristic equation of JK flip flop

* T Flip-flop



block diagram

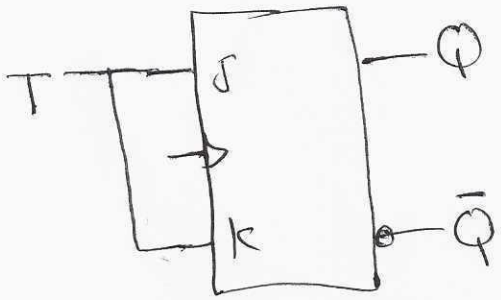
T	Q(t+1)
0	Q(t) no change
1	$\bar{Q}$(t) complement

we can design T flip flop from JK flip flop and from D Flip flop

① using JK flip-flop $Q(t+1)$

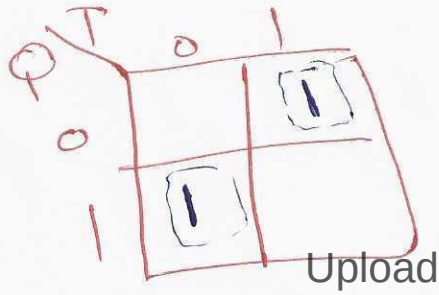
$J K = 0\ 0$, $T = Q(t)$

$J K = 1\ 1$ $\quad T^{Q(t+1)} = \bar{Q}(t)$



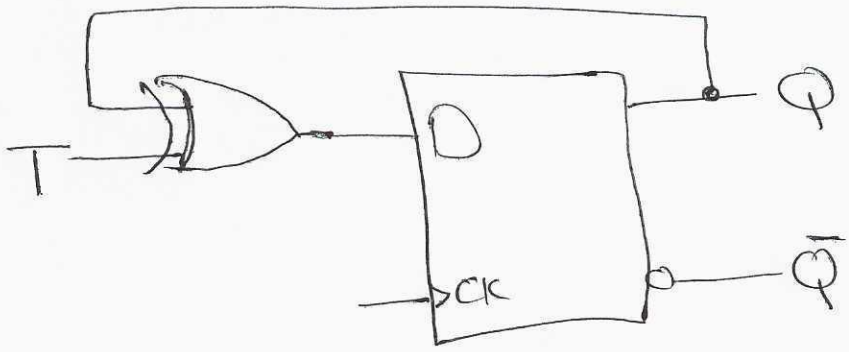
② using D flip flop

Q(t)	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0



$Q(t+1) = T\bar{Q} + \bar{T}Q$

$= T \oplus Q$



T flip flop from D flip flop

* Flip Flop Characteristics Equation

D Flip-flop

D	Q(t+1)
0	0 Reset
1	1 set

$Q(t+1) = D$

JK Flip-flop

J	K	Q(t+1)
0	0	Q(t) No Chang
0	1	0 reset
1	0	1 set
1	1	$\bar{Q}(t)$ Complement

$Q(t+1) = J\bar{Q}(t) + \bar{K}Q(t)$

T-flip-flop

T	Q(t+1)
0	Q(t) No change
1	$\bar{Q}(t)$ complem

$Q(t+1) = T \oplus Q(t)$

* Analysis of Clocked Sequential Circuits

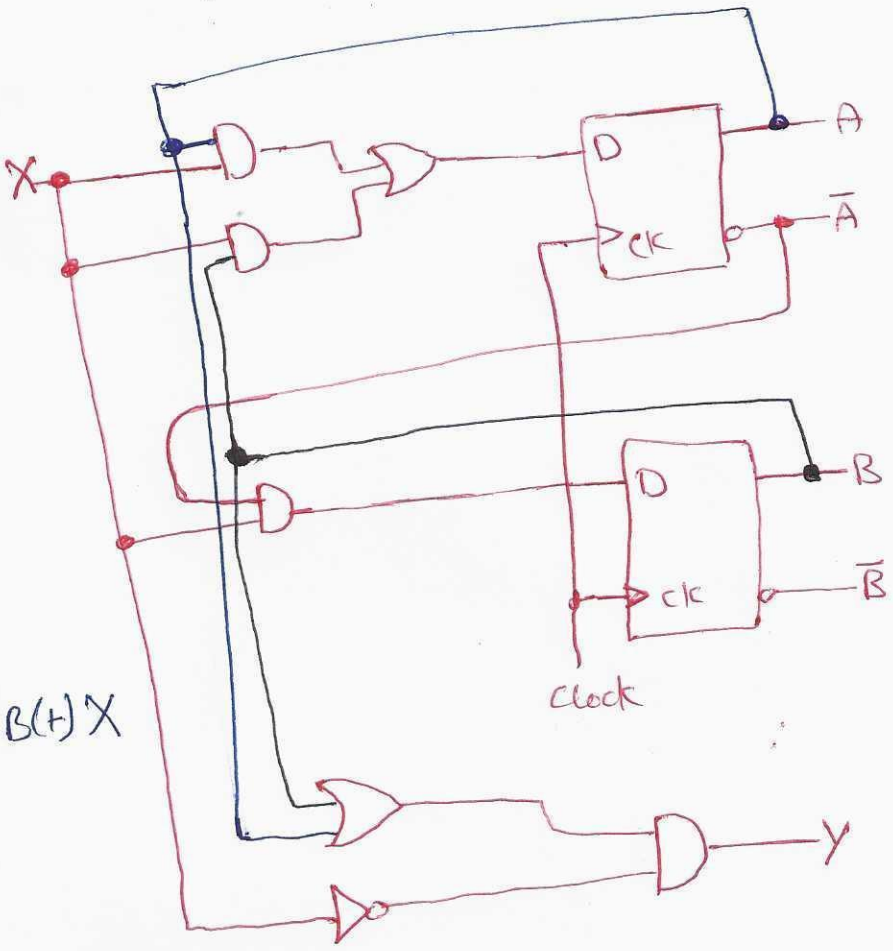
1- obtain the equations at the inputs of the flip-flop

2- obtain the ouput equation.

3- Fill the state table for all possible inputs and state values

4- Draw the state diagram.

Example:-



(1) Equation at the input of the flip flop

$D_A = AX + BX$

$D_B = \bar{A}X$

D-flip flop

$A(t+1) = D_A = A(t)X + B(t)X$

$B(t+1) = D_B = \bar{A}(t)X$

(2) Equation of the output (Y)

$Y = (A + B) \cdot \bar{X}$

(3) State Tables:-

Present state A	Present state B	input X	Next state A	Next state B	output Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

$A(t+1) = A(t)X + B(t)X$

$B(t+1) = \bar{A}X$

$Y = (A+B)\bar{X}$

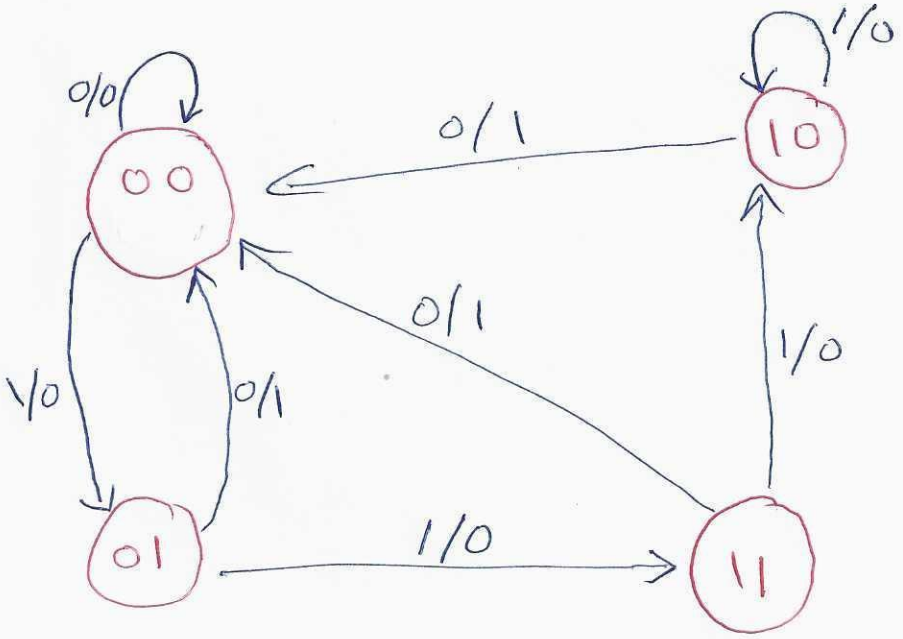
Present state A	Present state B	Next state X=0 A	Next state X=0 B	Next state X=1 A	Next state X=1 B	output X=0 Y	output X=1 Y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

④ state diagram: graphical representation of the state table

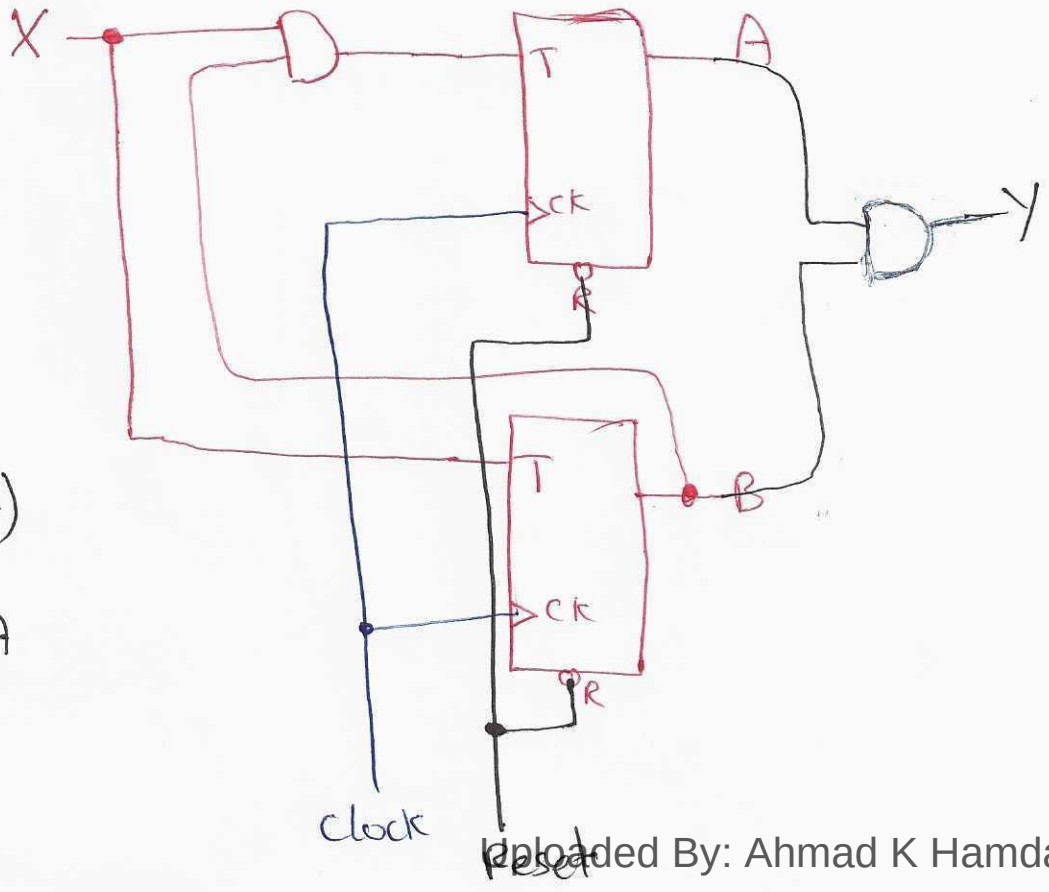
# of flip flops

① The circles are the states 2

② Arcs are the state transitions labeled with input x / output y



Example:



① input equations

$T_A = X \cdot B(t)$

$T_B = X$

$A(t+1) = T \oplus A(t)$

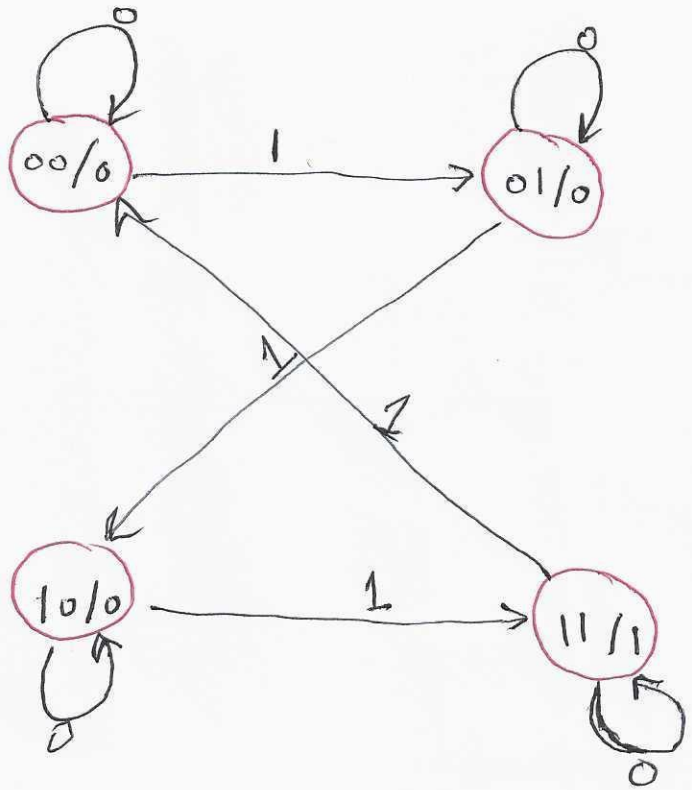
$= B \cdot X \oplus A$

$B(t+1) = T \oplus B$

$= X \oplus B$

(3) state table

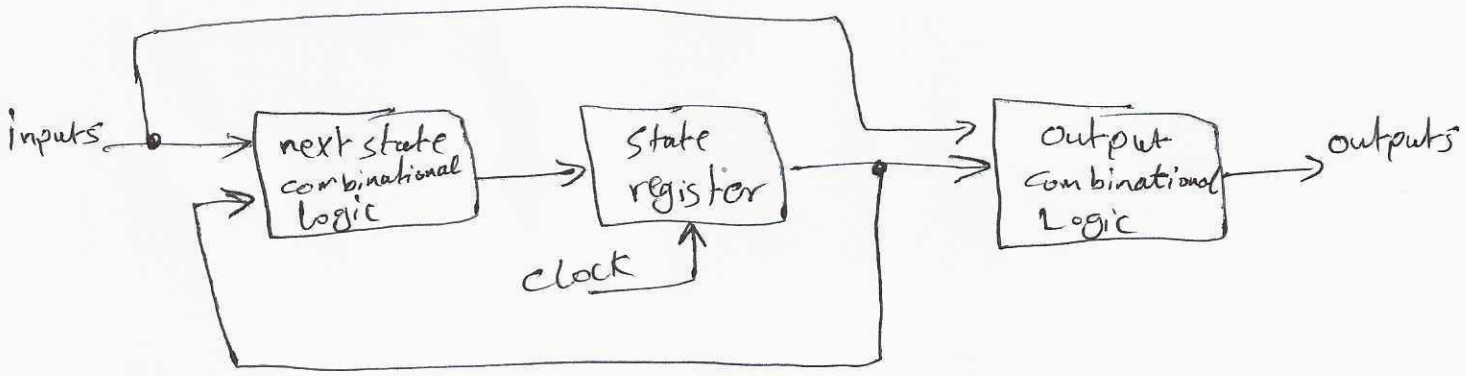
present state A	present state B	input X	Next state A	Next state B	output Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1



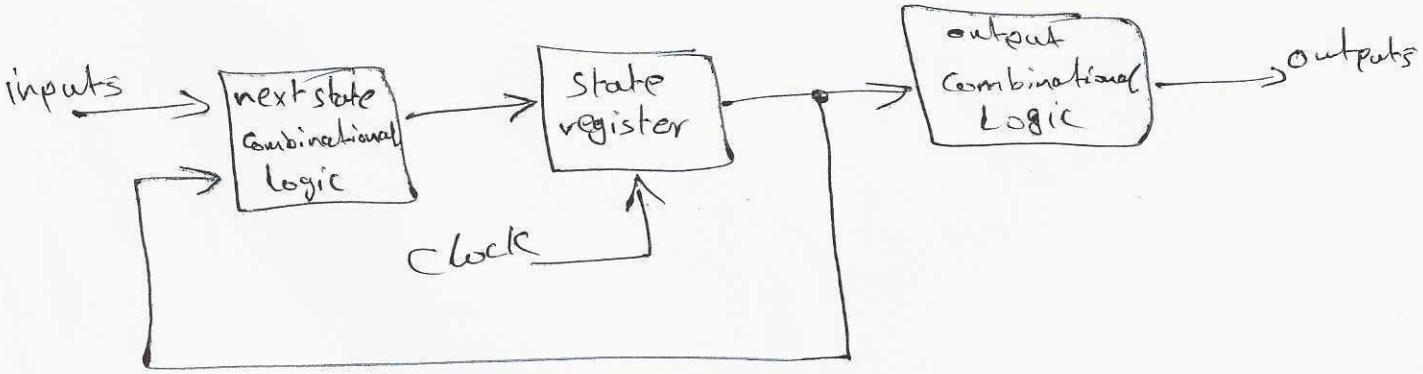
* Types of synchronouse sequential Circuits

There are two ways to design a synchronous sequential Circuits :-

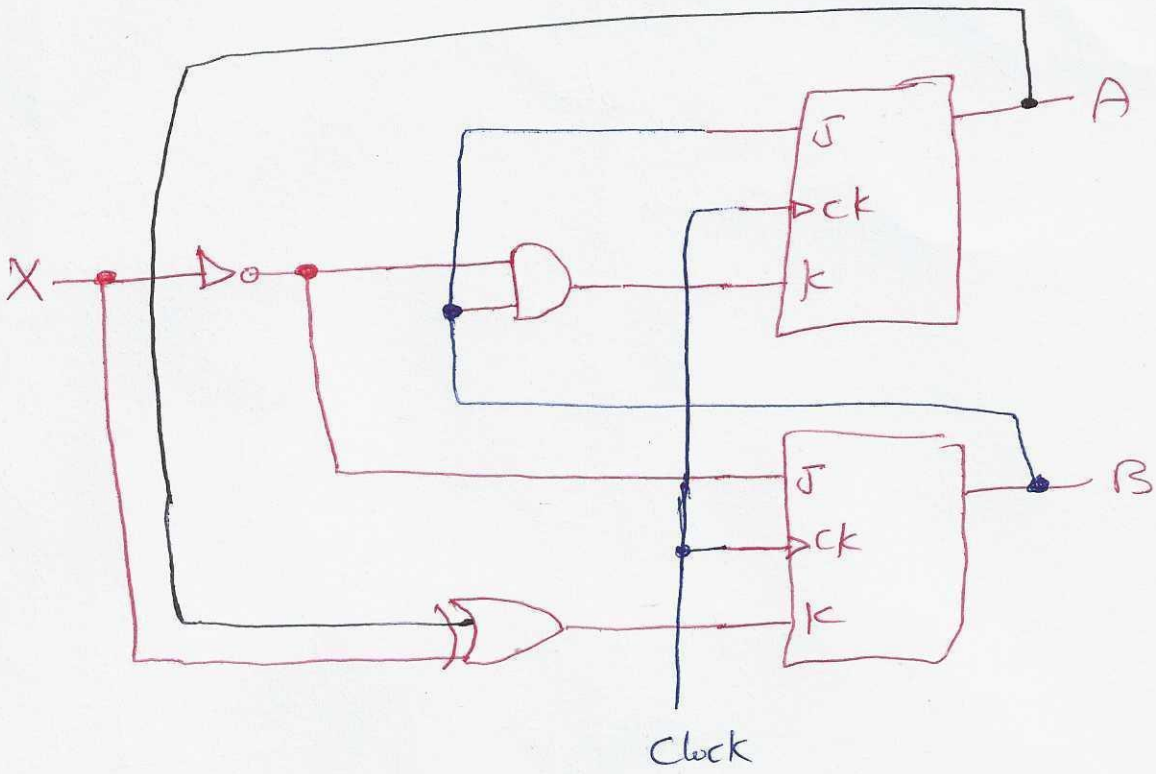
① Mealy machine



② Moore machine



Example:-



(1) input equations

$$J_A = B$$

$$K_A = \bar{X}B$$

$$A(t+1) = J_A \bar{A}(t) + \bar{K}_A A(t)$$

$$= B\bar{A} + (\overline{\bar{X}B})A = \bar{A}B + A\bar{B} + AX$$

$$J_B = \bar{X}$$

$$K_B = X \oplus A$$

$$B(t+1) = J_B \bar{B} + \bar{K}_B B$$

$$= \bar{X}\bar{B} + (\overline{X \oplus A})B$$

$$= \bar{X}\bar{B} + [\bar{A}\bar{X} + AX] \cdot B$$

(3) state tables:

present state A	present state B	input X	Next state A	Next state B
0	0	0	0	1
0	0	1	0	0
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1