DEPARTMENT OF COMPUTER SYSTEM ENGINEERING

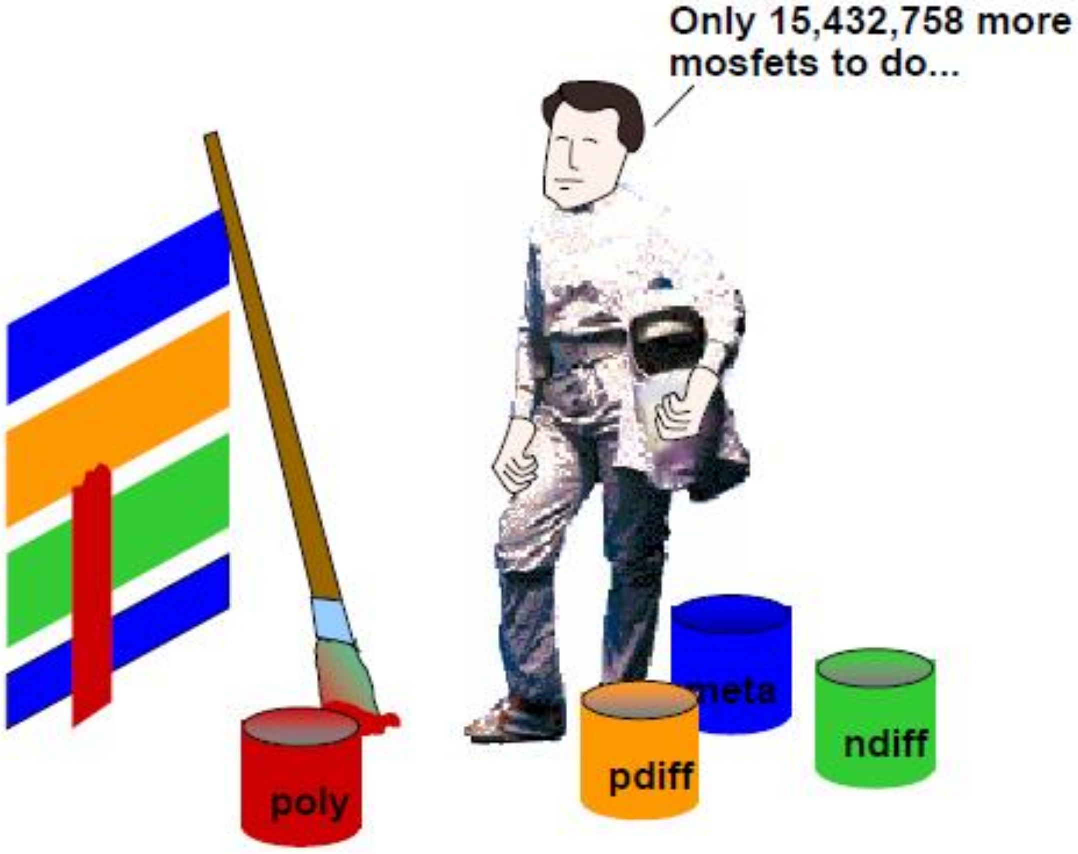
Digital Integrated Circuits - ENCS333

Dr. Khader Mohammad

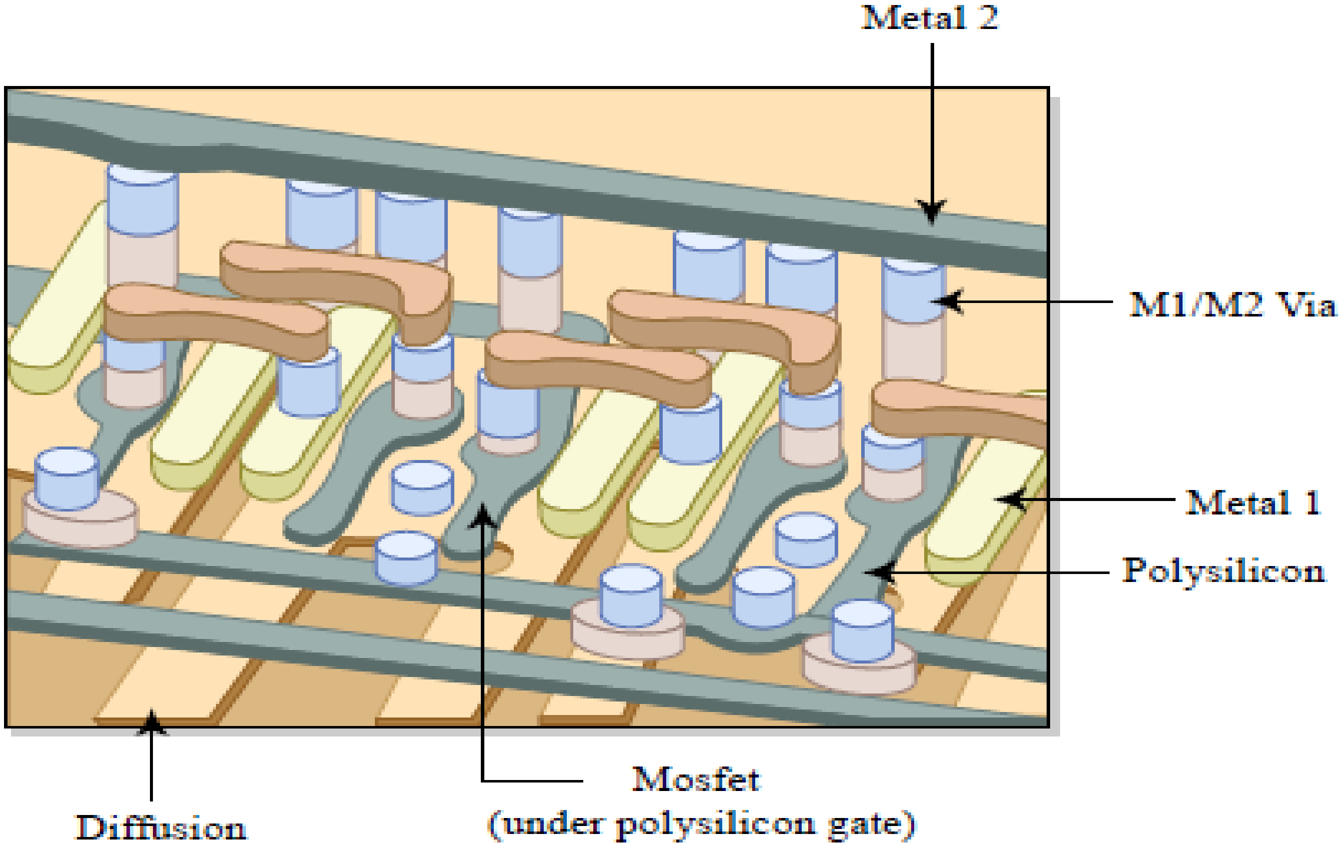
Lecture #7 – Layout

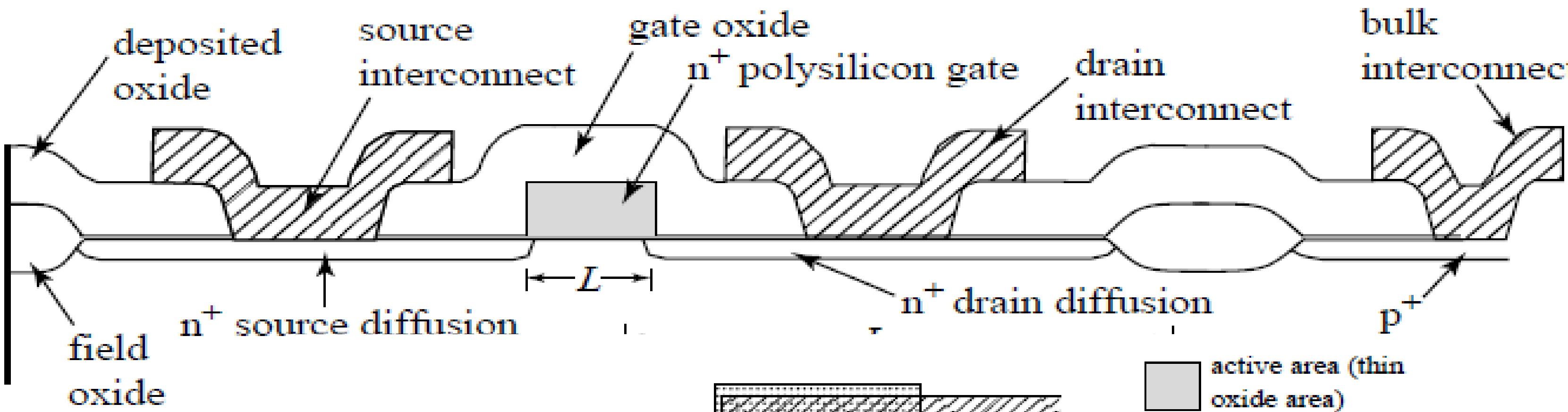
Integrated-Circuit Devices and Modeling

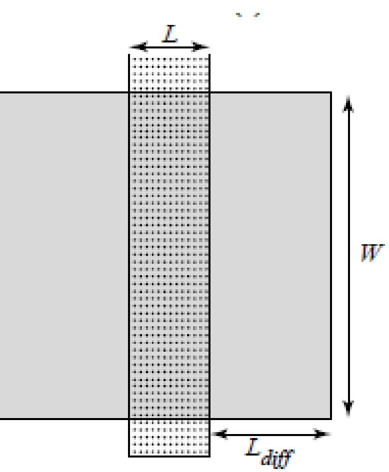
Layout

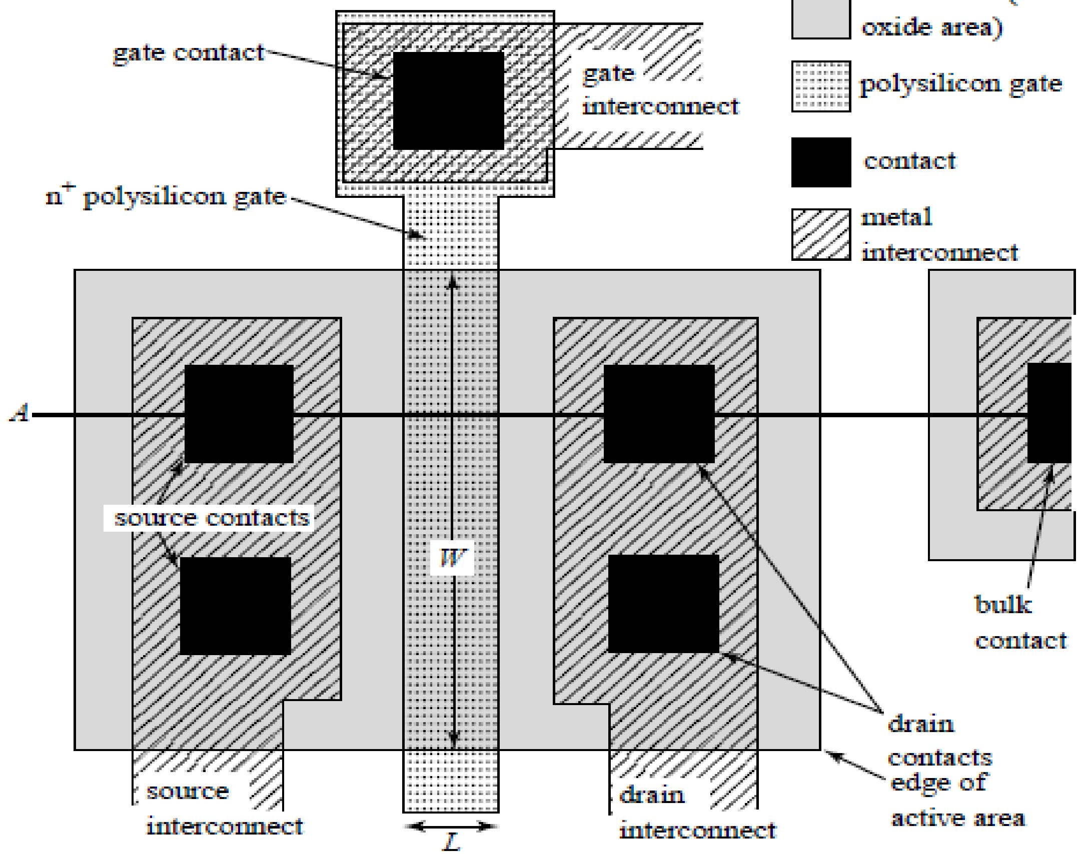


Real silicon



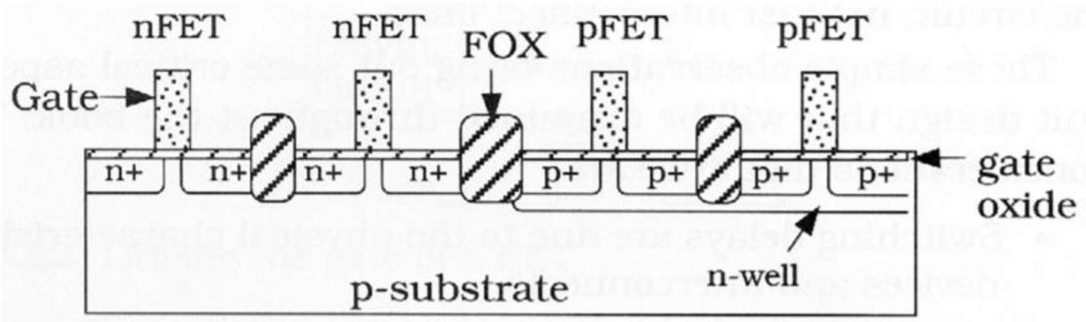

deposited oxide
source interconnect
gate oxide
n^+ polysilicon gate
drain interconnect
bulk interconnect
L
field oxide
n^+ source diffusion
n^+ drain diffusion
p^+


L
W
L_{diff}


gate contact
gate interconnect
n^+ polysilicon gate
active area (thin oxide area)
polysilicon gate
contact
metal interconnect
A
source contacts
W
bulk contact
drain contacts
edge of active area
source interconnect
drain interconnect
L

CMOS Fabrication Process

- What is a “process”
  – sequence of steps used to form circuits on a wafer
  – use additive (deposition) and subtractive (etching) steps
- n-well process – starts with p-type wafer (doped with acceptors)
- can form nMOS directly on p-substrate
  – add an n-well to provide a place for pMOS
- Isolation between devices
  - thick insulator called Field Oxide, FOX

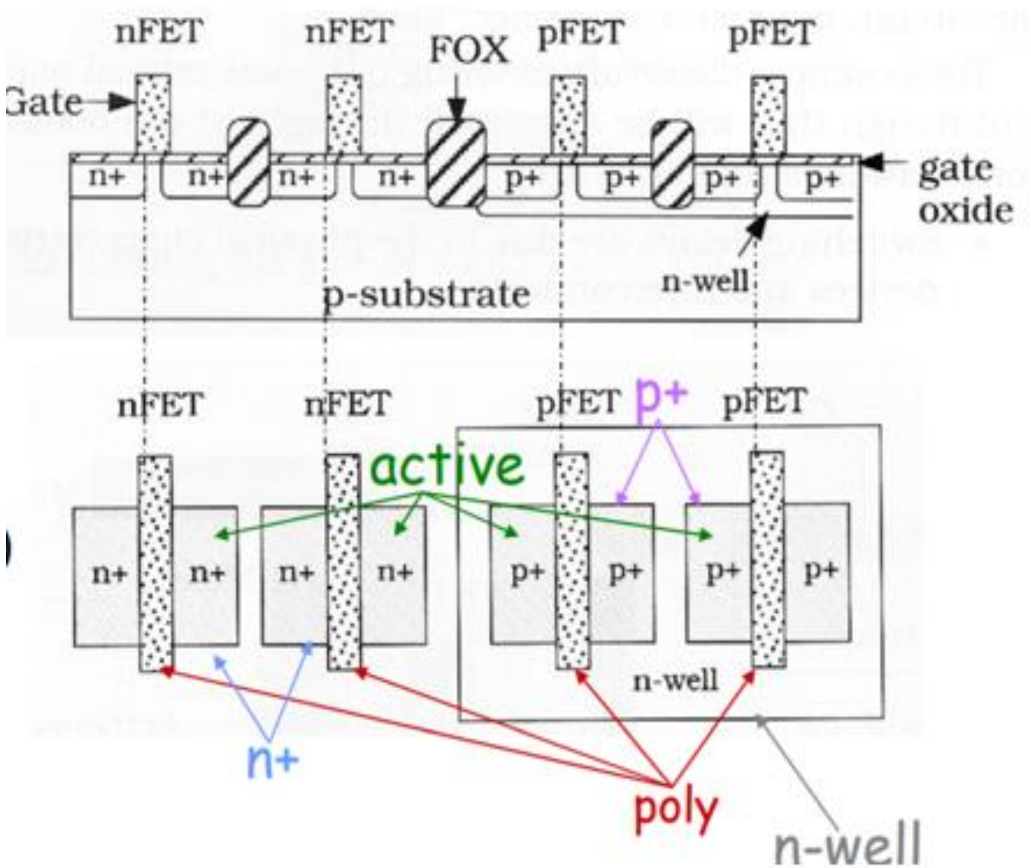


Lower CMOS Layers

- Visible Features
  - – p-substrate
  - – n-well
  - – n+ S/D regions
  - – p+ S/D regions
  - – gate oxide
  - – polysilicon gate
- Mask Layers
  - - n-well
  - – active (S/D regions)

    active = not FOX
  - - n+ doping
  - – p+ doping
  - – poly patterning

    gate oxide aligned to gate poly, no oxide mask



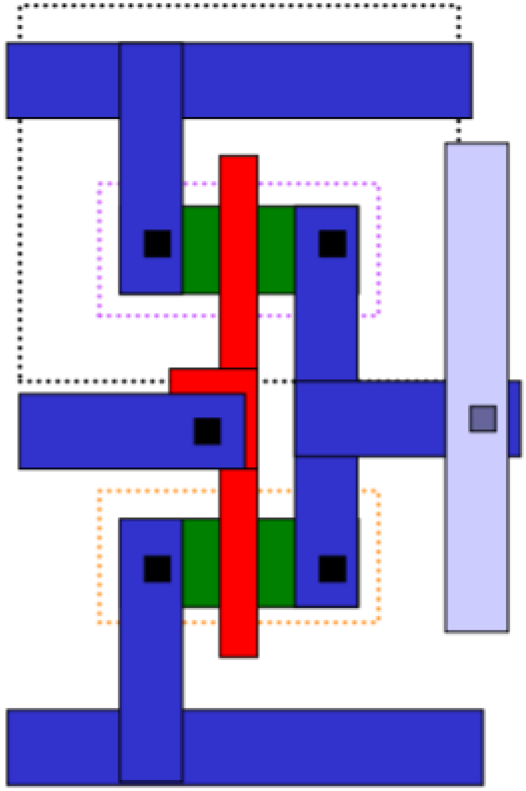
Process (μ)		0.25	0.18	0.13	0.10	0.07	0.05
V_{DD} (V)		2	1.8	1.5	1.2	0.9	0.7
L_{eff} (nm)		160	100	70	50	35	25
t_{ox} (A)		50	45	30	25	20	15
Levels		6	6	7	8	9	9
Poly	H (μ)	0.2	0.15	0.13	0.1	0.07	0.07
	W (μ)	0.25	0.18	0.13	0.1	0.07	0.05
	space (μ)	0.25	0.18	0.13	0.1	0.07	0.05
	sheet ρ (Ω/□)	4	5.3	6.2	8	11.4	11.4
M1–2	H (μ)	0.5	0.46	0.34	0.26	0.2	0.14
	W (μ)	0.30	0.23	0.17	0.13	0.1	0.07
	space (μ)	0.30	0.23	0.17	0.13	0.1	0.07
	sheet ρ (Ω/□)	0.044	0.048	0.065	0.085	0.11	0.16
	t_{ins} (nm)	650	500	360	320	270	210
M3–4	H (μ)	0.9	0.8	0.7	0.55	0.4	0.28
	W (μ)	0.6	0.5	0.4	0.3	0.2	0.14
	space (μ)	0.6	0.5	0.4	0.3	0.2	0.14
	sheet ρ (Ω/□)	0.024	0.028	0.031	0.04	0.055	0.079
	t_{ins} (nm)	900	800	700	600	500	400
M5–6	H (μ)	2.5	2.5	1.5	1.2	1.0	0.8
	W (μ)	2.0	2.0	1.0	1.0	0.6	0.5
	space (μ)	2.0	2.0	1.0	1.0	0.6	0.5
	sheet ρ (Ω/□)	0.009	0.009	0.015	0.018	0.022	0.028
	t_{ins} (nm)	1400	1400	900	800	700	600
M7–8	H (μ)	–	–	2.5	2.5	1.5	1.4
	W (μ)	–	–	2.0	2.0	1.0	0.9
	space (μ)	–	–	2.0	2.0	1.0	0.9
	sheet ρ (Ω/□)	–	–	0.009	0.009	0.015	0.016
	t_{ins} (nm)	–	–	1400	1400	900	800
M9	H (μ)	–	–	–	–	2.5	2.5
	W (μ)	–	–	–	–	2.0	2.0
	space (μ)	–	–	–	–	2.0	2.0
	sheet ρ (Ω/□)	–	–	–	–	0.009	0.009
	t_{ins} (nm)	–	–	–	–	1400	1400
Via (M1–M2)	size (μ)	0.55	0.26	0.2	0.16	0.12	0.09
	R (Ω)	0.95	1.32	1.61	2.23	3.35	4.63
κ		3.3	2.7	2.3	2	1.8	1.5

Layout CAD Tools

- Layout Editor
  - draw multi-vertices polygons which represent physical design layers
  - Manhattan geometries, only 90º angles
- Manhattan routing: run each interconnect layer perpendicular to each other
- Design Rules Check (DRC)
  - checks rules for each layer (size, separation, overlap)
  - must pass DRC or will fail in fabrication
- Parameter Extraction
  - create netlist of devices (tx, R, C) and connections
  - extract parasitic Rs and Cs, lump values at each line (R) / node (C)
- Layout Vs. Schematic (LVS)
  - compare layout to schematic
  - check devices, connections, power routing
- can verify device sizes also
  - ensures layout matches schematic exactly
  - passing LVS is final step in layout

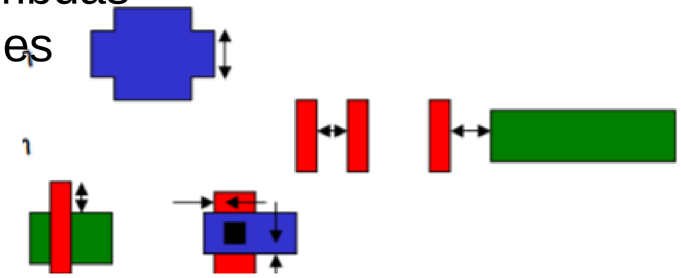
CMOS Layout Layers

- Mask layers for 1 poly, 2 metal, n-well CMOS process
– Background: p-substrate
– nWell
– Active
– Poly
– pSelect
– nSelect
– Active Contact
– Poly Contact
– Metal1
– Via
– Metal2
– Overglass



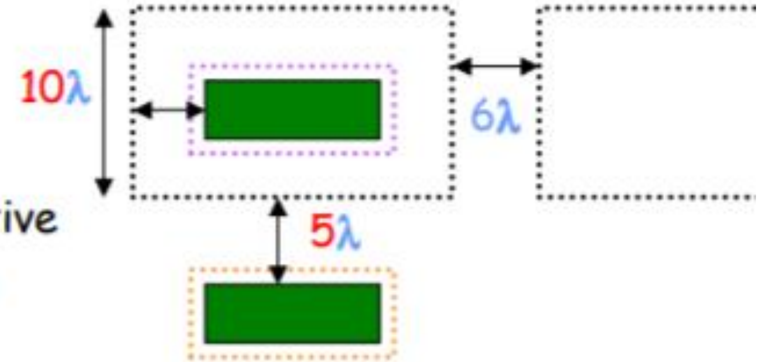
Design Rules: Intro

- Why have Design Rules
  - – fabrication process has minimum/maximum feature sizes that can be
produced for each layer
  - – alignment between layers requires adequate separation (if layers
unconnected) or overlap (if layers connected)
  - – proper device operation requires adequate separation
- "Lambda" Design Rules
  - – lambda, λ, = 1/2 minimum feature size, e.g., 0. 6μm process -> λ =0.3μm
  - – can define design rules in terms of lambdas
- allows for "scalable" design using same rules
- Basic Rules
  - – minimum layer size/width
  - – minimum layer separation
  - – minimum layer overlap

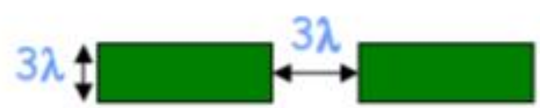


Design Rules: 1

- n-well MOSIS **SCMOS rules;** λ **=0.3μm** for AMI C5N
  - required everywhere pMOS is needed
  - rules
    - minimum width
    - minimum separation to self
    - minimum separation to nMOS Active
    - minimum overlap of pMOS Active

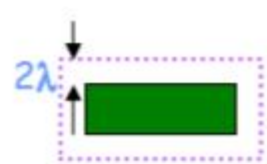


- Active
  - required everywhere a transistor is needed
  - any non-Active region is FOX
  - rules
    - minimum width
    - minimum separation to other Active

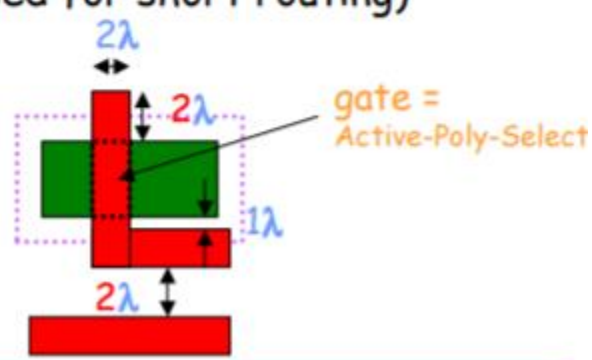


Design Rules: 2

- n/p Select
  - defines regions to be doped n+ and p+
  - tx S/D = Active AND Select NOT Poly
  - tx gate = Active AND Select AND Poly
  - rules
    - minimum overlap of Active
      - same for pMOS and nMOS
    - several more complex rules available



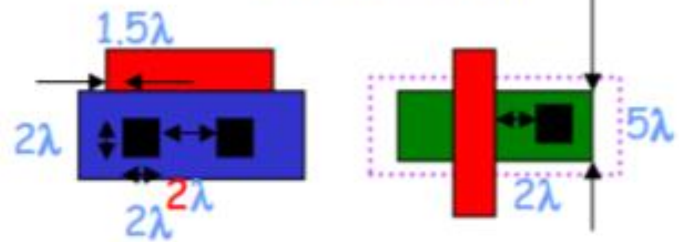
- Poly
  - high resistance conductor (can be used for short routing)
  - primarily used for tx gates
  - rules
    - minimum size
    - minimum space to self
    - minimum overlap of gate
    - minimum space to Active



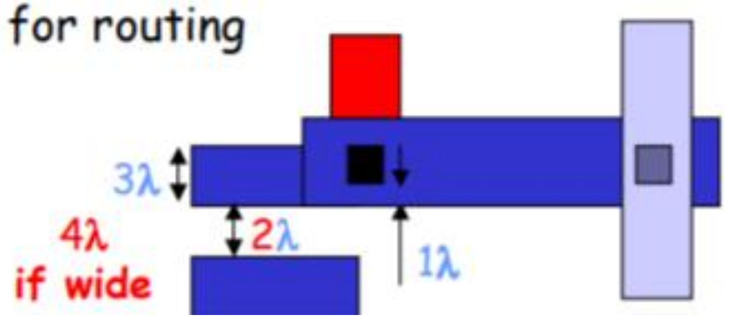
Design Rules: 3

- Contacts
  - Contacts to Metal1, from Active or Poly
    - use same layer and rules for both
  - must be SQUARE and MINIMUM SIZED
  - rules
    - exact size
    - minimum overlap by Active/Poly
    - minimum space to Contact
    - minimum space to gate

note: due to contact size and overlap rules, min. active size at contact will be 2+1.5+1.5=5λ



- Metal1
  - low resistance conductor used for routing
  - rules
    - minimum size
    - minimum space to self
    - minimum overlap of Contact



Design Rules: 4

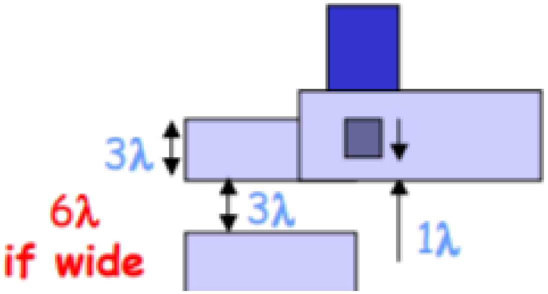
Vias

- Connects Metal1 to Metal2
- must be SQUARE and MINIMUM SIZED
- rules
  - exact size 2λ
  - space to self 3λ
  - minimum overlap by Metal1/Metal2 1λ
  - minimum space to Contact 2λ
  - minimum space to Poly/Active edge 2λ

see MOSIS site for illustrations

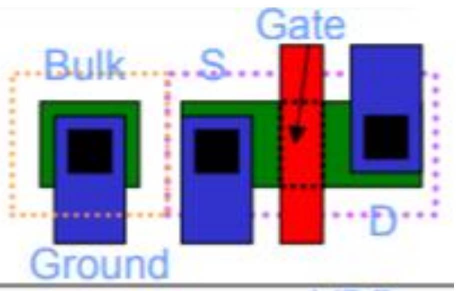
Metal2

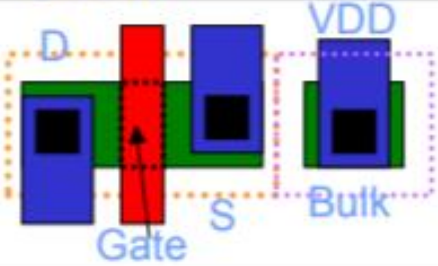
- low resistance conductor used for routing
- rules
  - minimum size
  - minimum space to self
  - minimum overlap of Via

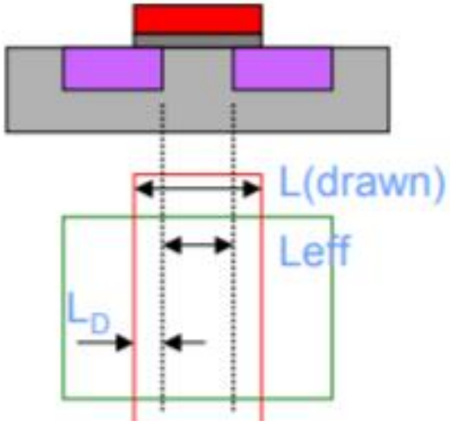


Physical Realization of a MOSFET

- nMOS Layout
  - gate is intersection of Active, Poly, and nSelect
  - S/D formed by Active with Contact to Metal1
  - bulk connection formed by p+ tap to substrate
- pMOS Layout
  - gate is intersection of Active, Poly, and pSelect
  - S/D formed by Active with Contact to Metal1
  - bulk connection formed by n+ tap to nWell
- Effective Gate Size
  - S/D will diffuse under the gate
    - effective channel length is less than drawn
    - Leff = L(drawn) - $2L_D$
  - FOX will undercut active region
    - effective channel width is less than drawn
    - Weff = W(drawn) - ΔW
  - L_D and Δ W defined by fab. process
  - generally taken care of by SPICE



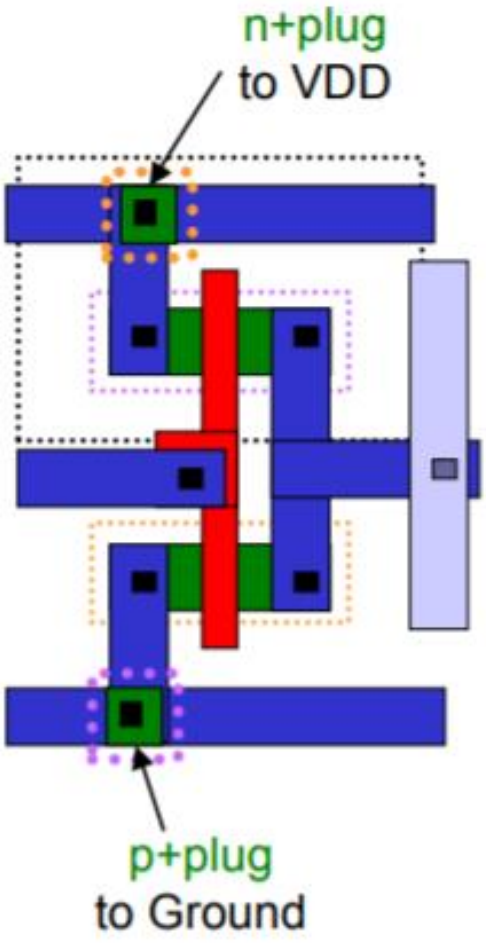




Substrate/well Contacts

Substrate and nWells must be connected to the power supply within each cell

- use many connections to reduce resistance
- generally place
  - ~ 1 substrate contact per nMOS tx
  - ~ 1 nWell contact per pMOS tx
- this connection is called a tap, or plug
- often done on top of VDD/Ground rails
- need p+ plug to Ground at substrate
- need n+ plug to VDD in nWell



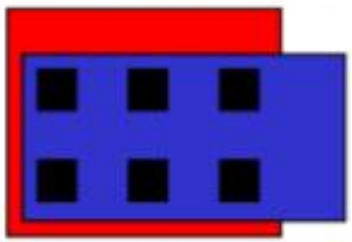
Multiple Contacts

Each contact has a characteristic resistance, Rc

Contact resistances are much higher than the resistance of most interconnect layers

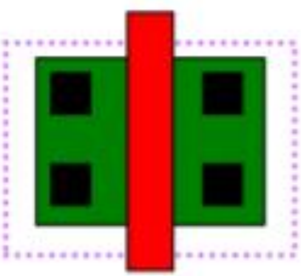
Multiple contacts can be used to reduce resistance

- $R_{c,eff} = R_c / N$, N=number of contacts

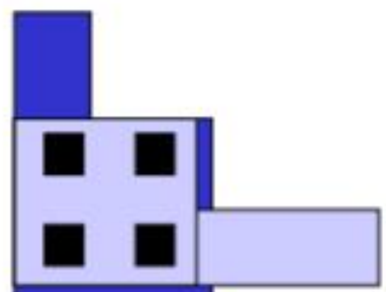


N=6

Generally use as many contacts as space allows



use several Contacts in wide txs

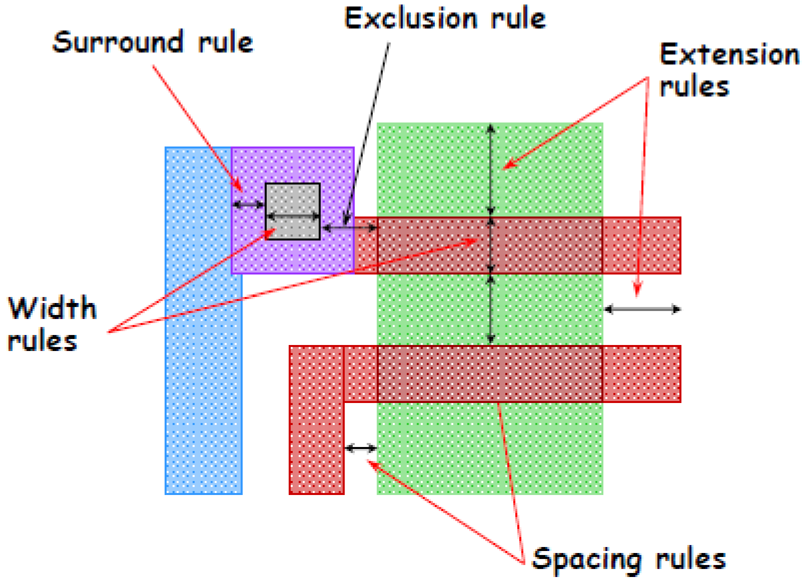


add Vias if room allows

Design Rules

- Design rules are an abstraction of the fabrication process that specify various geometric constraints on how different masks can be drawn.

- Design rules can be absolute measurements (e.g. in nm) or scaled to an abstract unit, the lambda. Lambda-based designs are scaled to the appropriate absolute units depending on the manufacturing process finally used.



Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

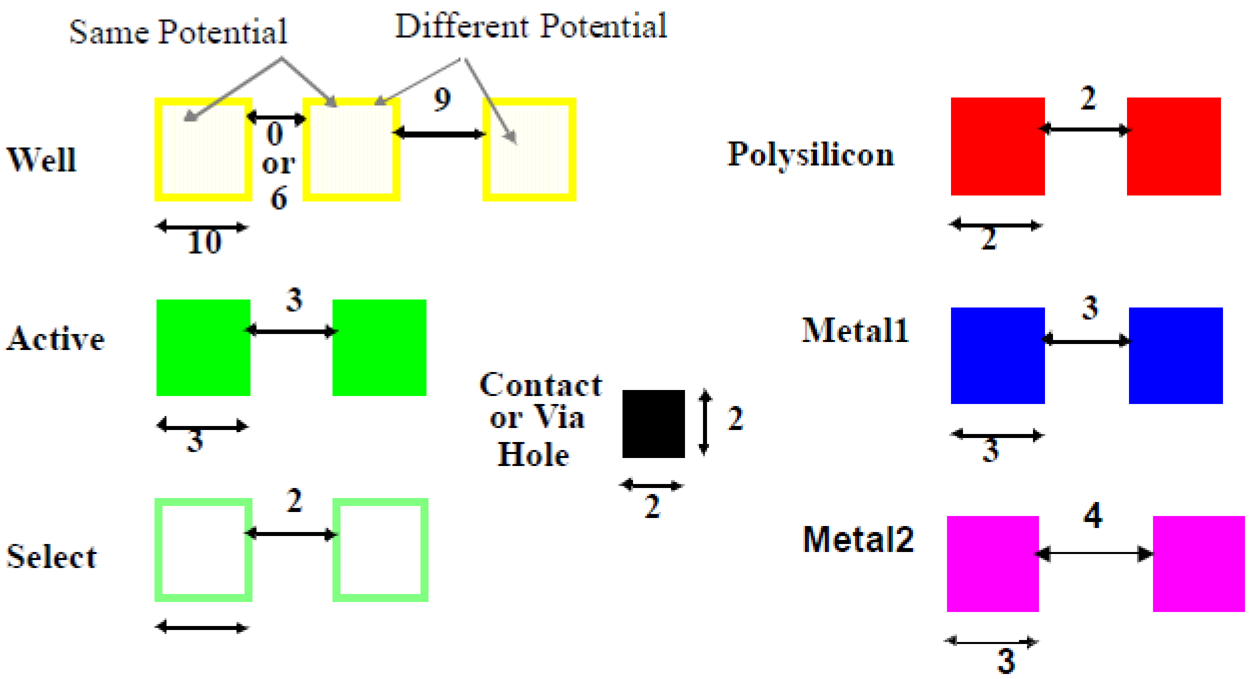
CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

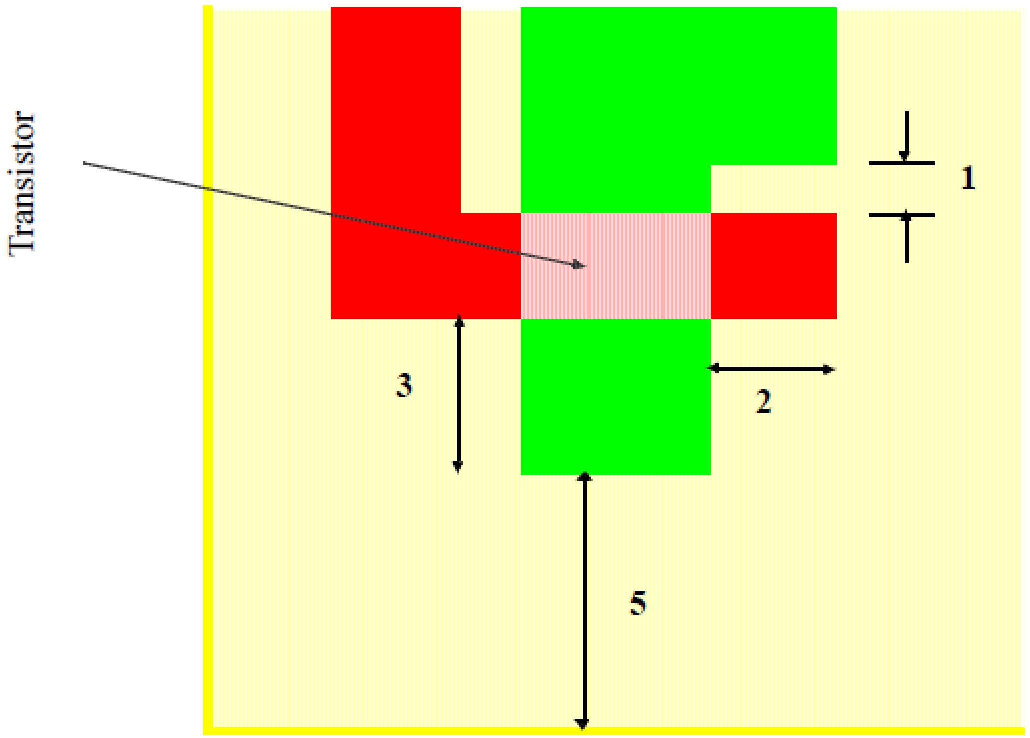
Layers in 0.25 μm CMOS process

Layer Description	Representation				
metal	m1	m2	m3	m4	m5
well	nw				
polysilicon	poly				
contacts & vias	ct	v12,v23,v34,v45	nwc	pwc	
active area and FETs	ndif	pdif	nfet	pfet	
select	nplus	pplus	prb		

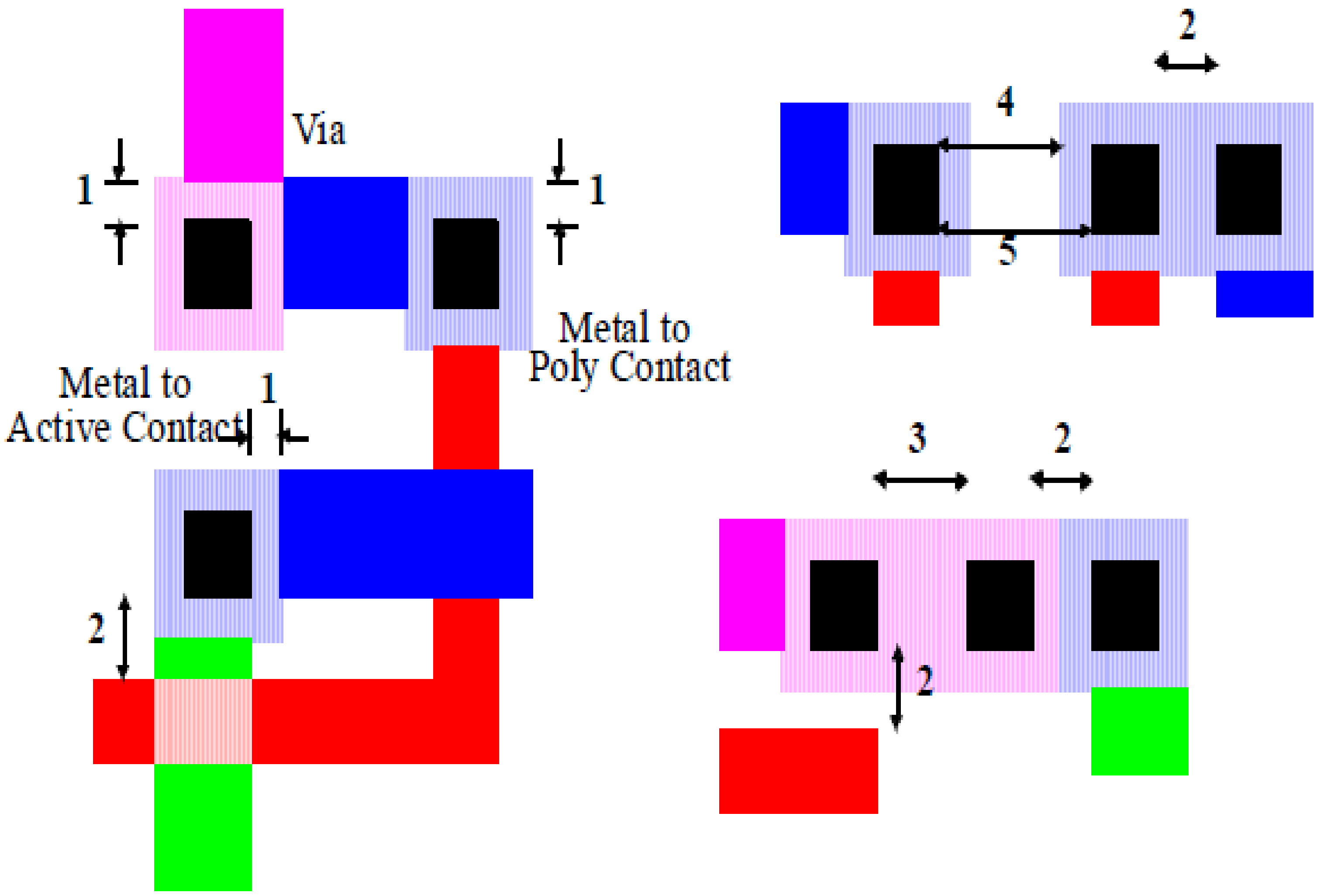
Intra-Layer Design Rules



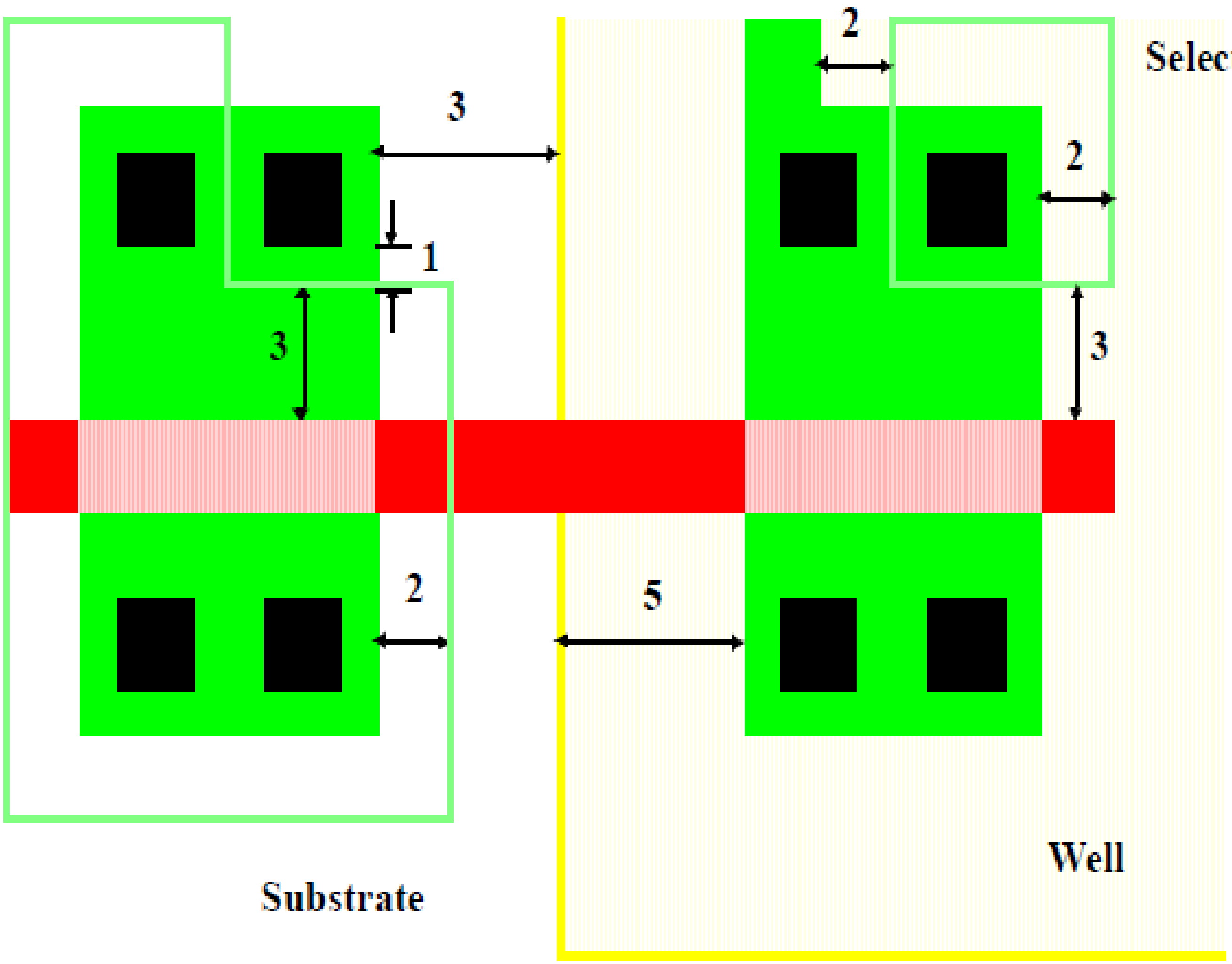
Transistor Layout



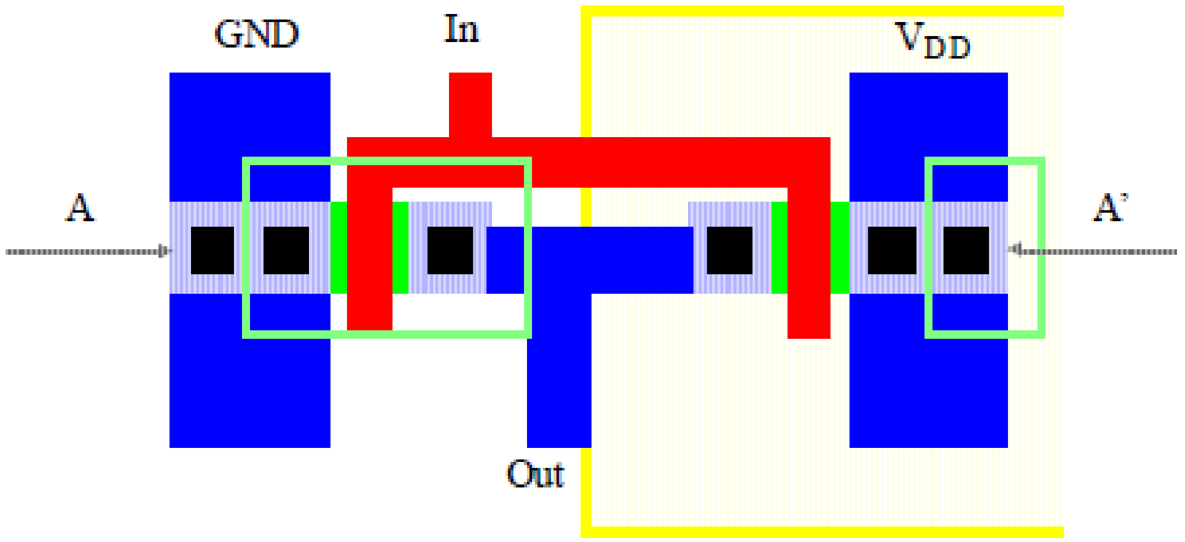
Vias and Contacts



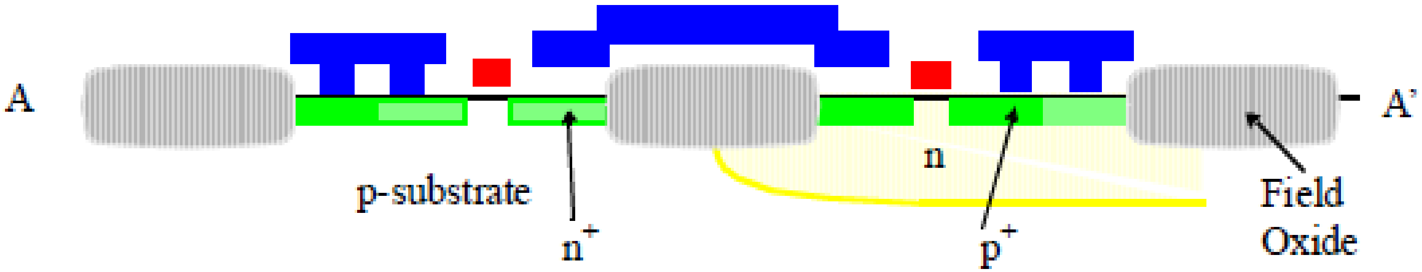
Select Layer



CMOS Inverter Layout



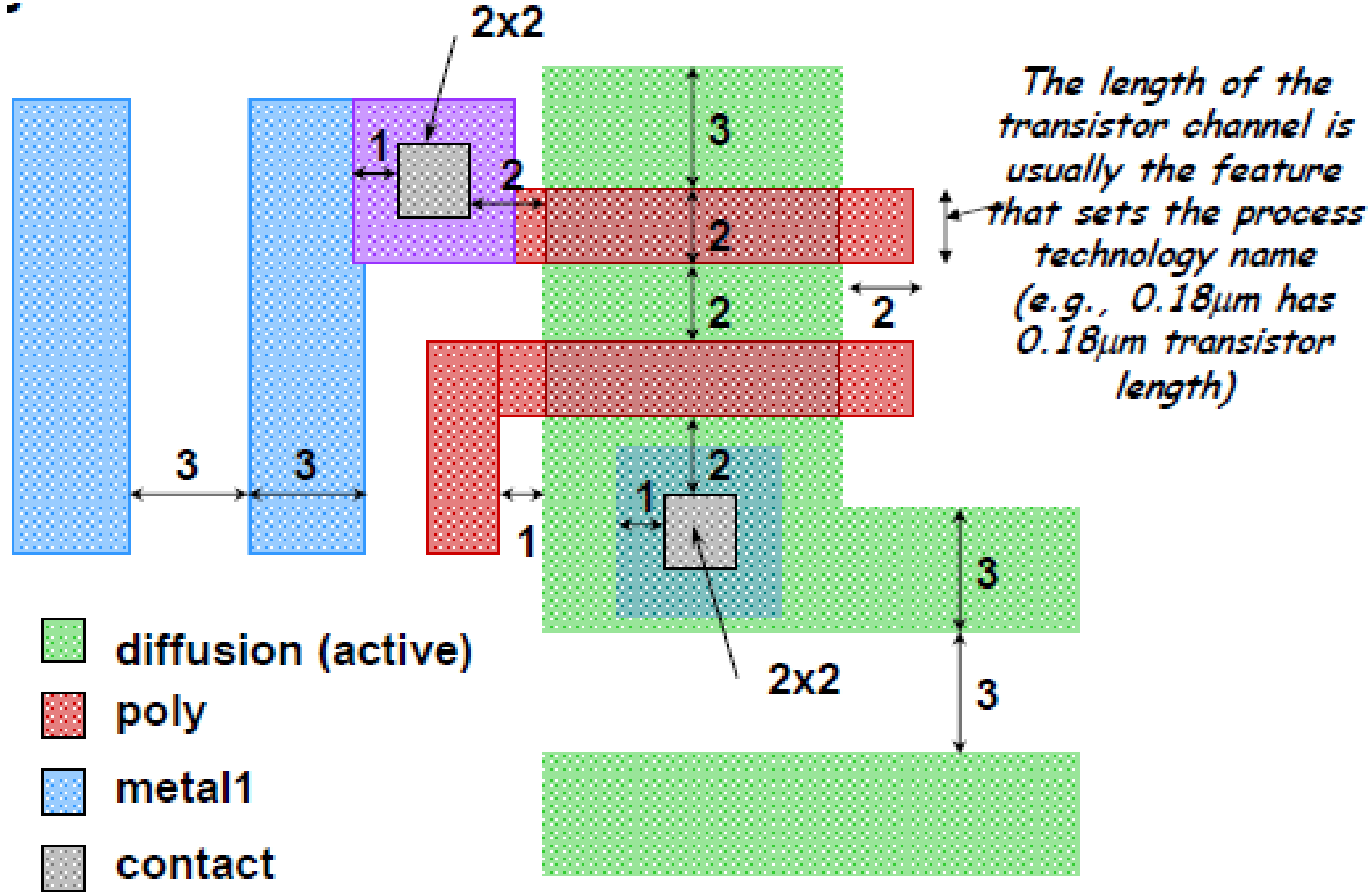
(a) Layout



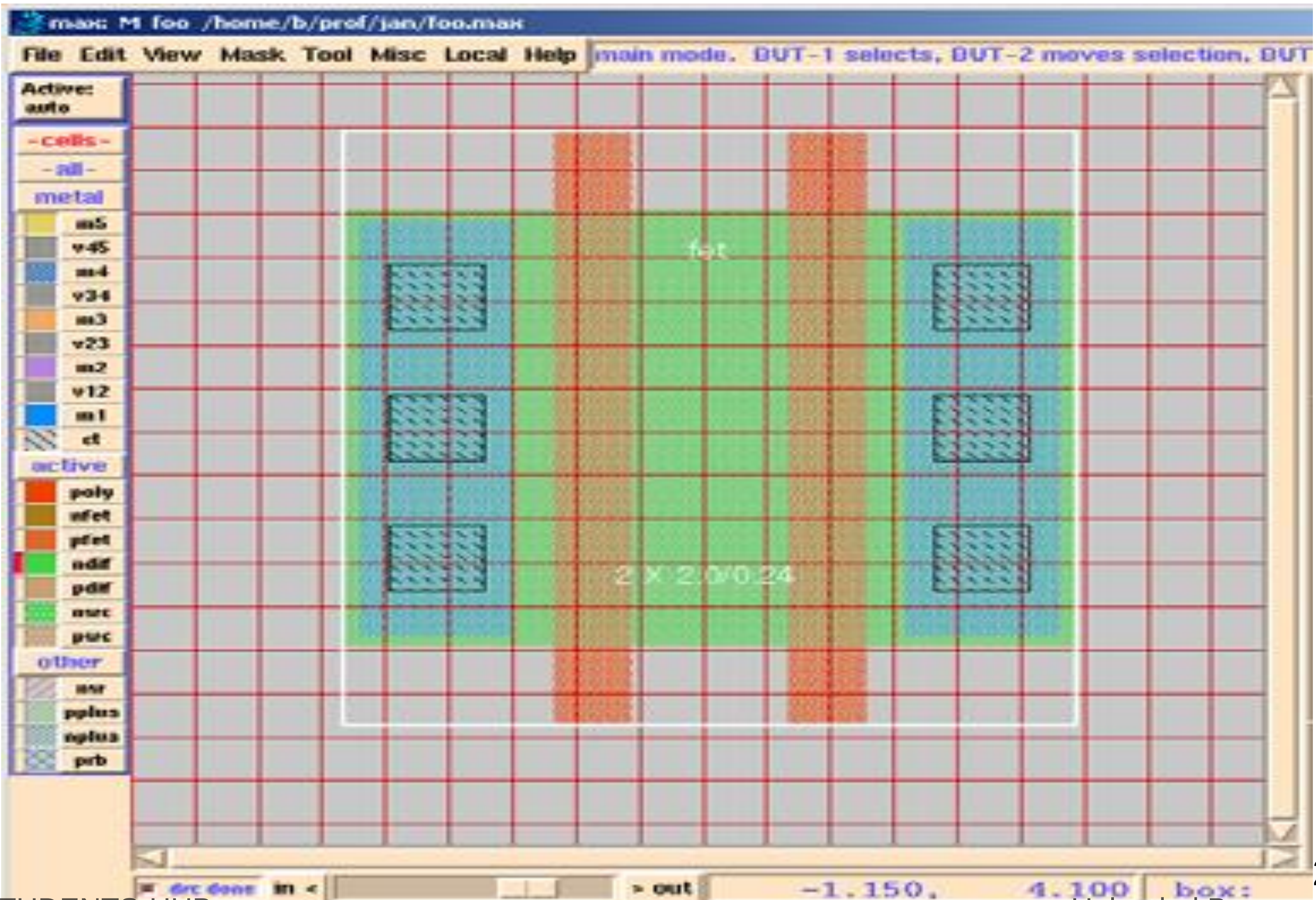
(b) Cross-Section along A-A'

Lambda-based Design Rules

- **One lambda (λ)= one half of the "minimum" mask dimension.**
- **Typically the length of a transistor channel is 2λ.**
- **Usually all edges must be "on grid", e.g., in the MOSIS scalable rules, all edges must be on a lambda grid.**



Layout Editor

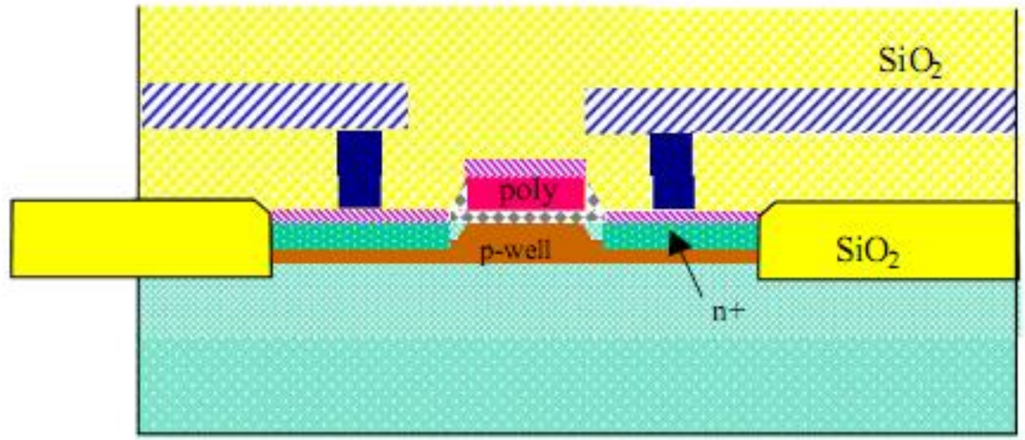


Design Rules

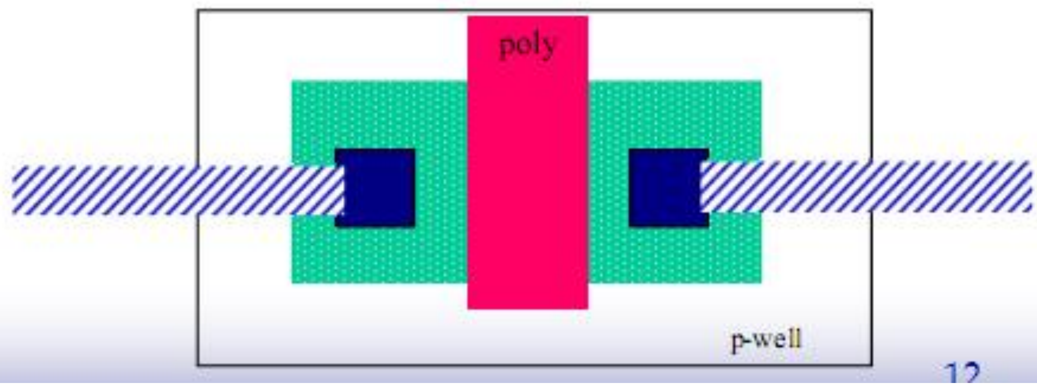
- Intra-layer
  - Widths, spacing, area
- Inter-layer
  - Enclosures, distances, extensions, overlaps
- Special rules (sub-0.25μm)
  - Antenna rules, density rules, (area)

Transistor Layout

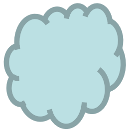
Cross-Sectional View



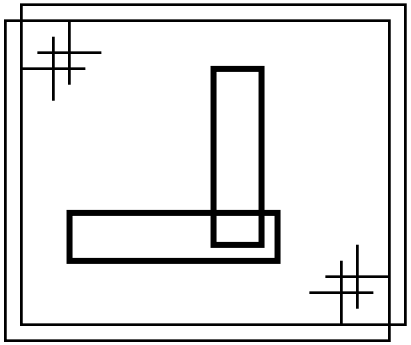
Layout View



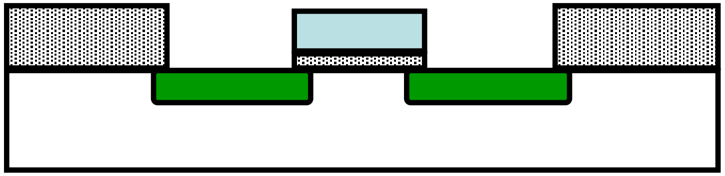
Why Have Design Rules?



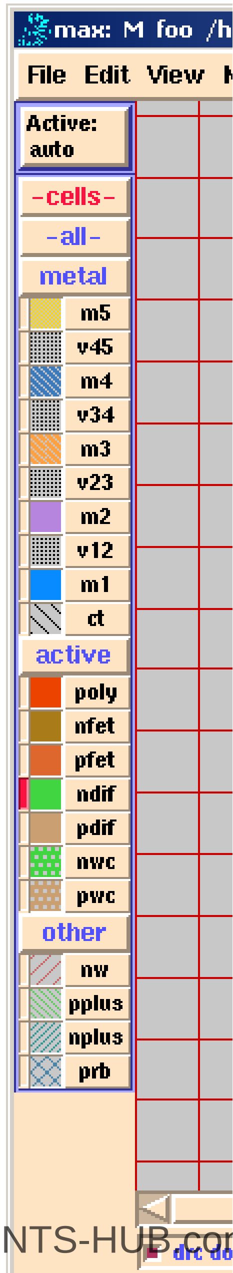
- To be able to tolerate some level of fabrication errors such as



1. Mask misalignment
2. Dust
3. Process parameters (e.g., lateral diffusion)
4. Rough surfaces



max Layer Representation

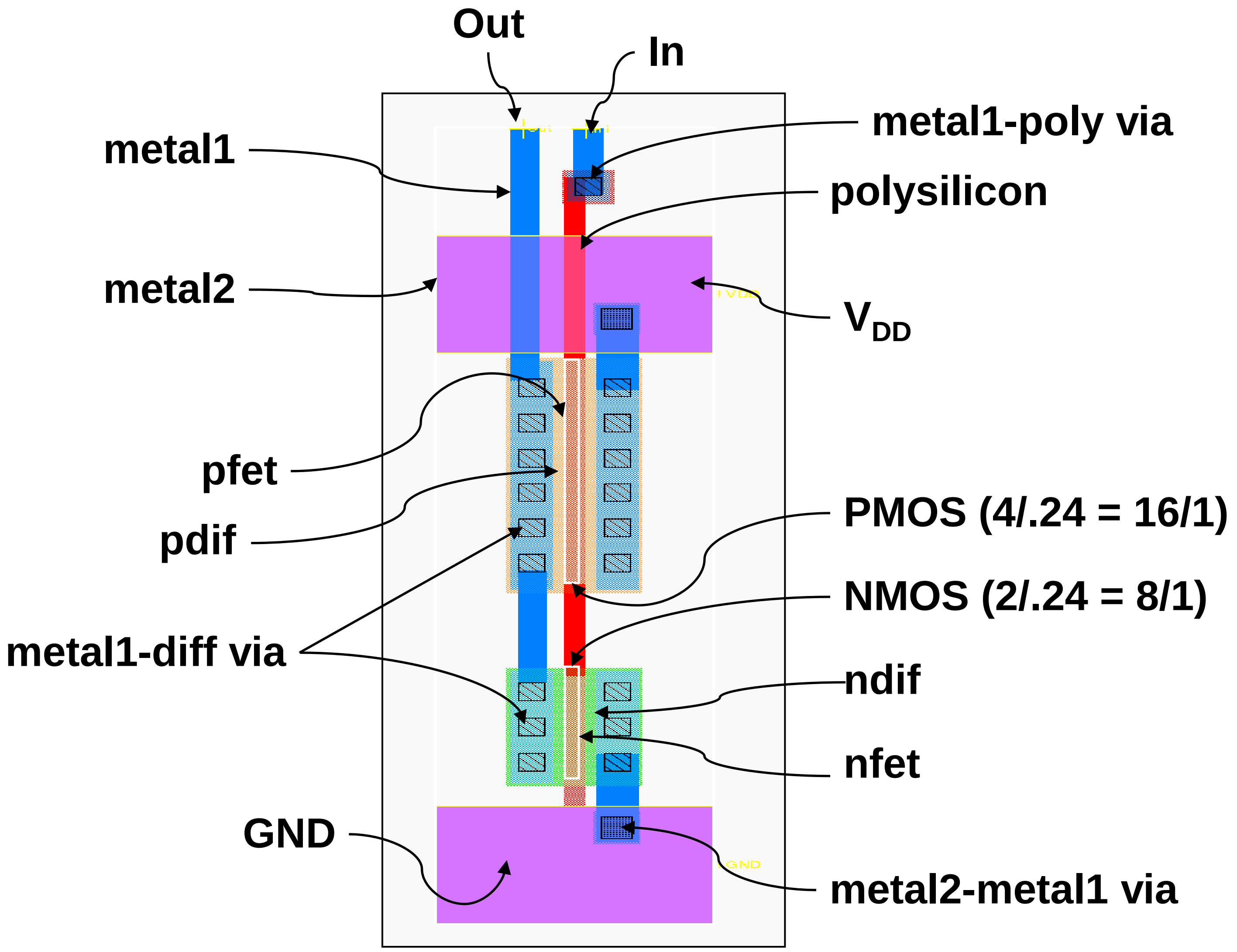


- Metals (five) and vias/contacts between the interconnect levels
  - Note that m5 connects only to m4, m4 only to m3, etc., and m1 only to poly, ndif, and pdif
  - Some technologies support "stacked vias"

- Active – active areas on/in substrate (poly gates, transistor channels (nfet, pfet), source and drain diffusions (ndif, pdif), and well contacts (nwc, pwc))

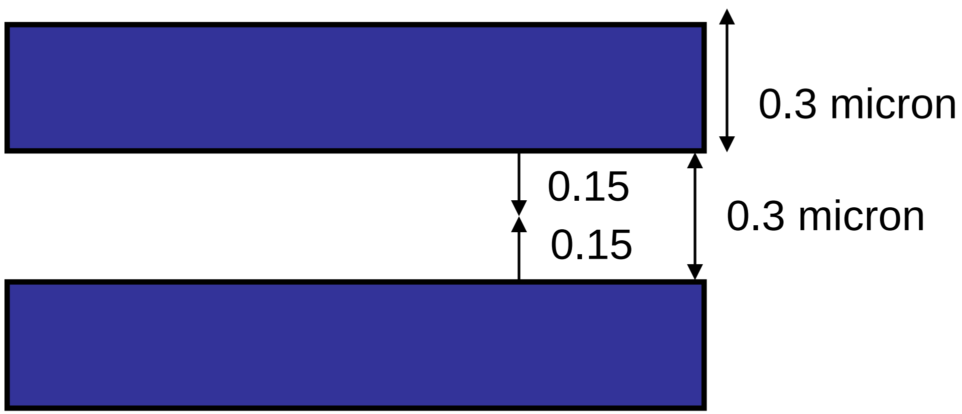
- Wells (nw) and other select areas (pplus, nplus, prb)

CMOS Inverter *max* Layout



Intra-Layer Design Rule Origins

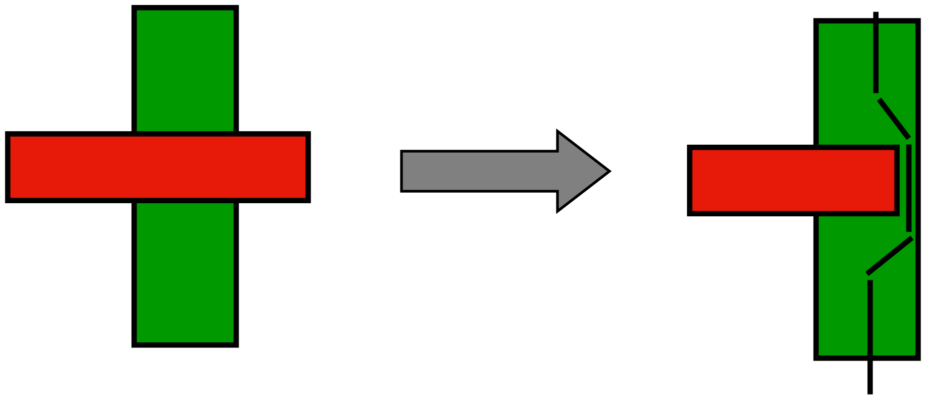
- Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
  - minimum line width is set by the resolution of the patterning process (photolithography)
- Minimum spaces between objects (that are *not* related) on the same layer to ensure they will not short after fab



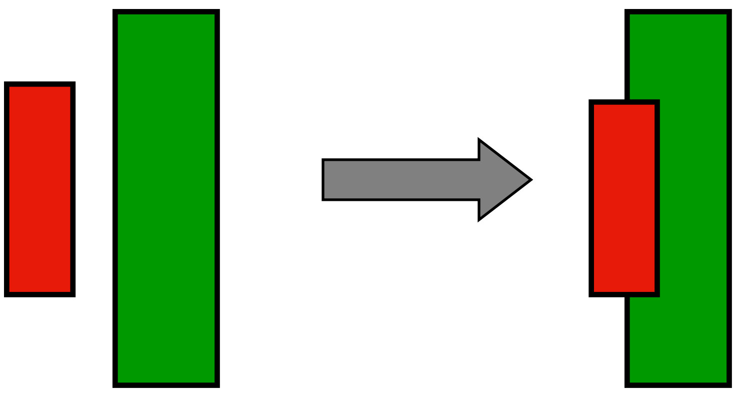
Inter-Layer Design Rule Origins

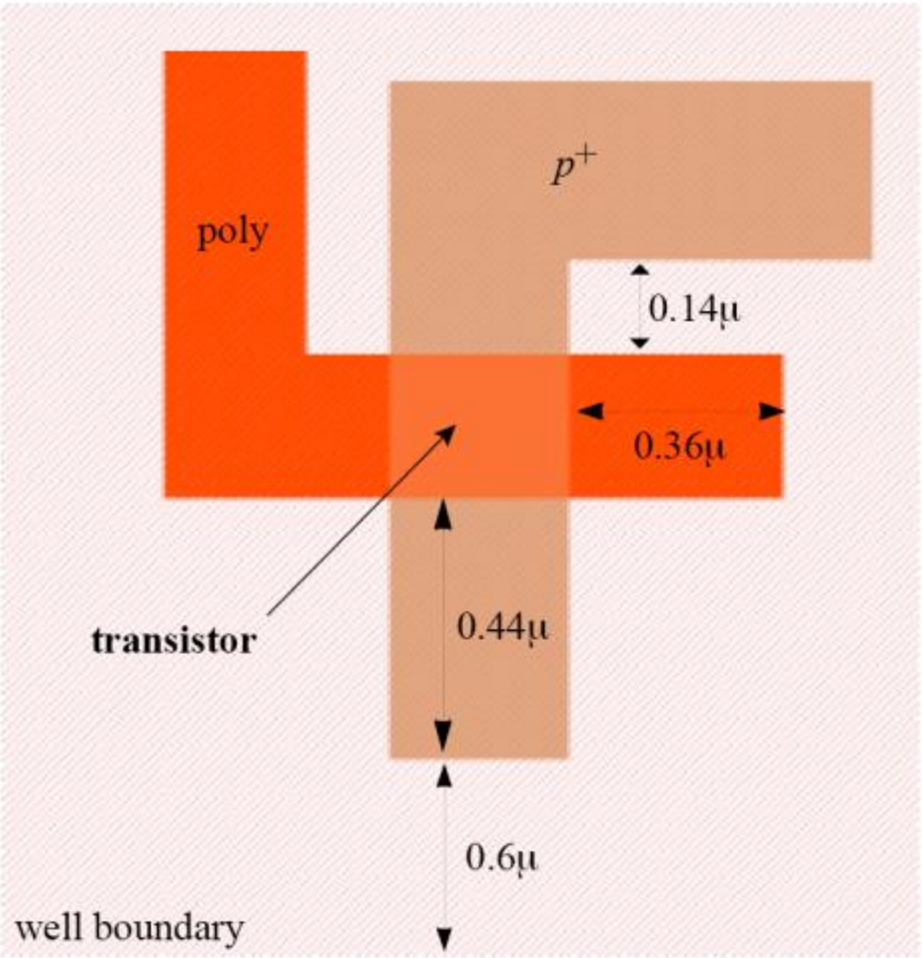
1. Transistor rules – transistor formed by overlap of active and poly layers

Transistors

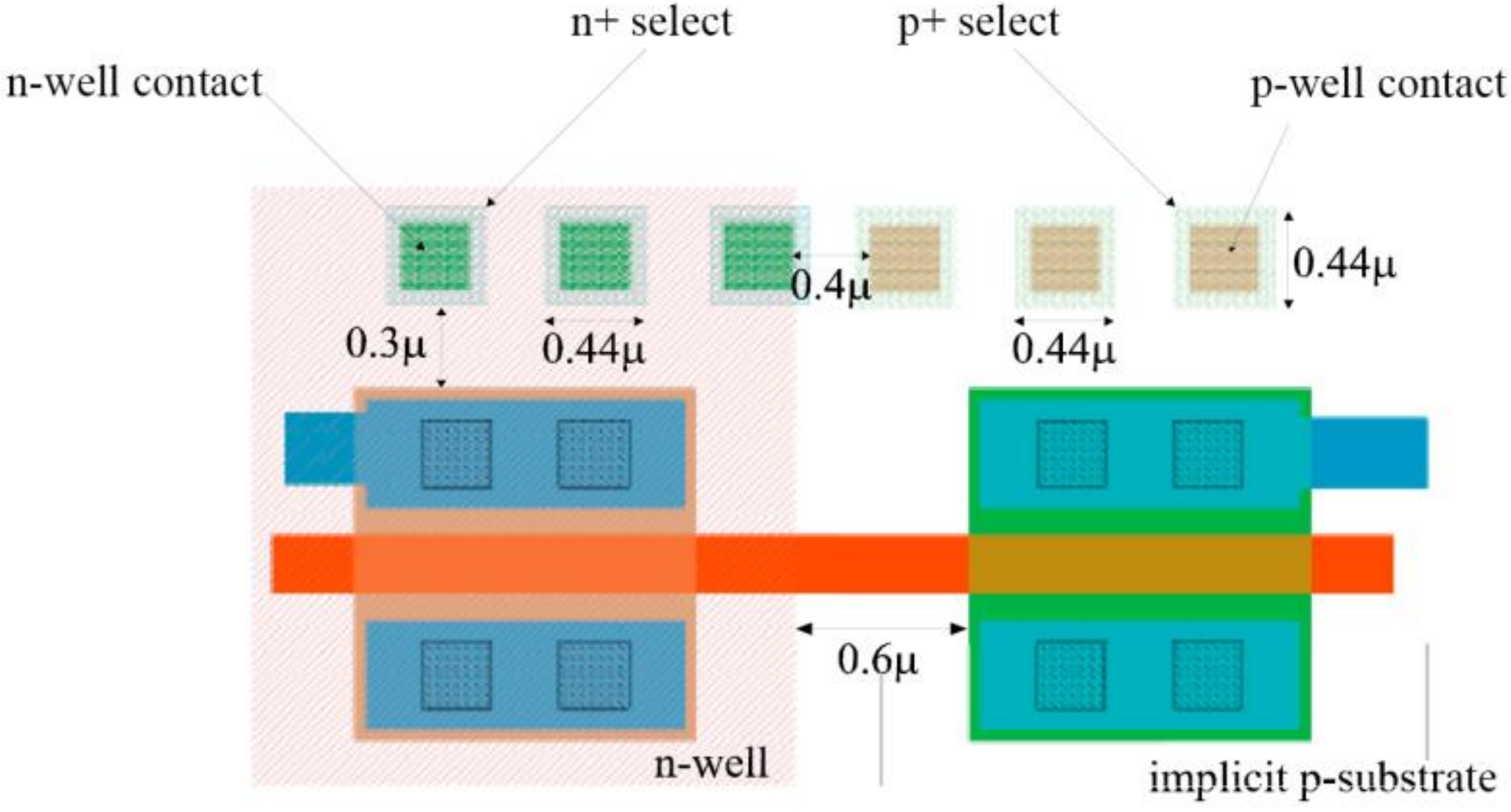


Unrelated Poly & Diffusion

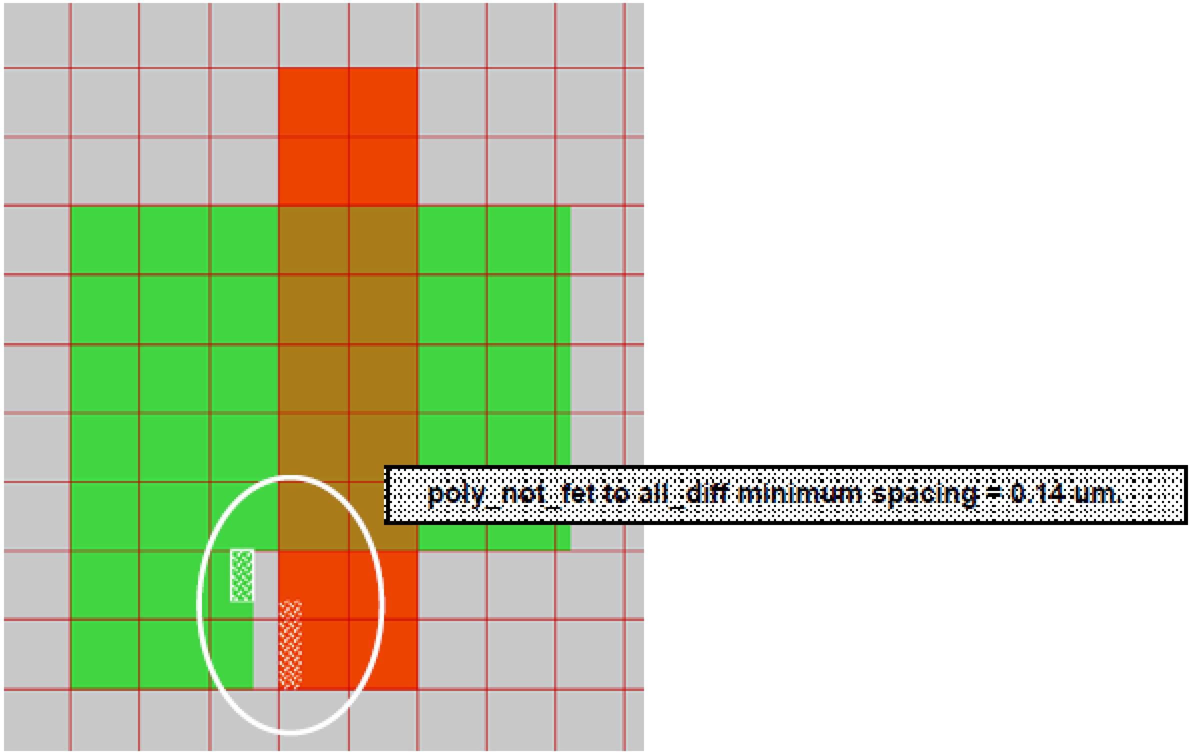



poly
p+
0.14μ
0.36μ
transistor
0.44μ
0.6μ
well boundary

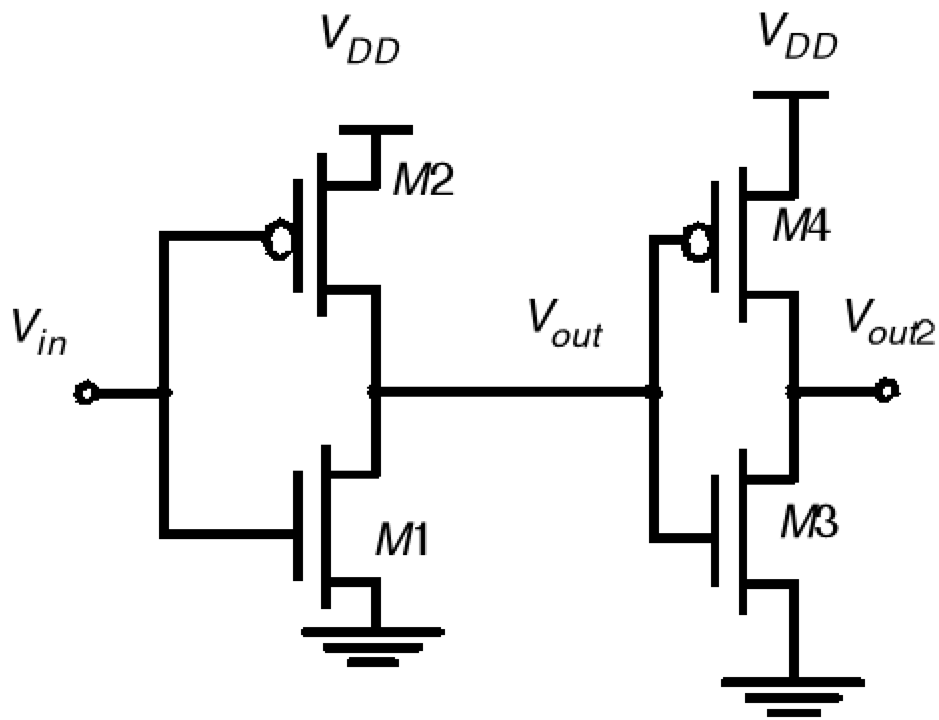
Inter-Layer: Well and Substrate



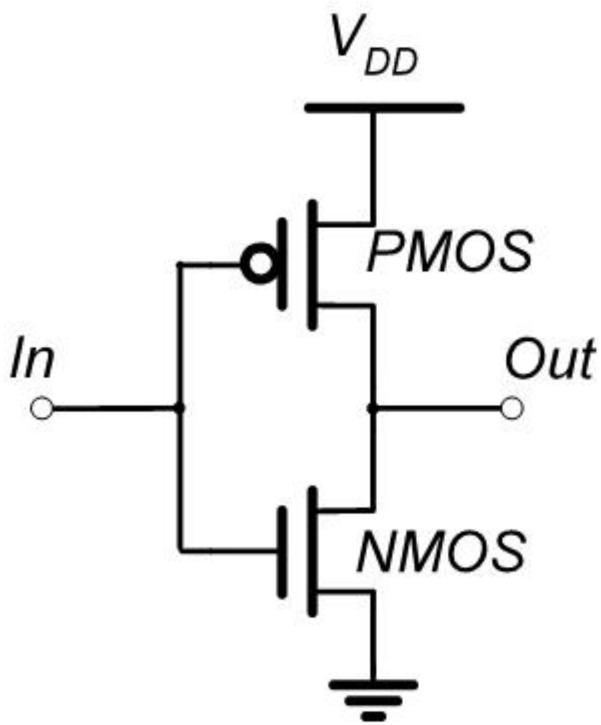
Design Rule Checker

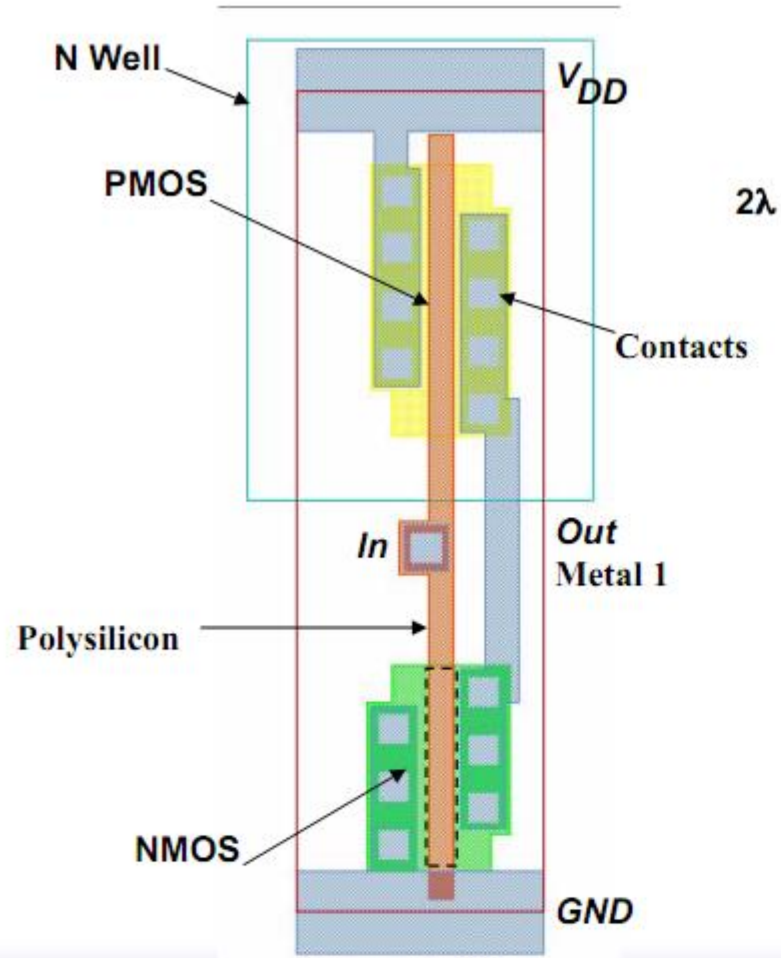


Circuit Under Design



CMOS Inverter

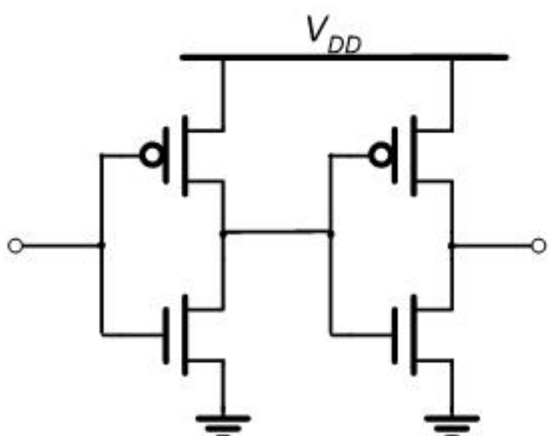


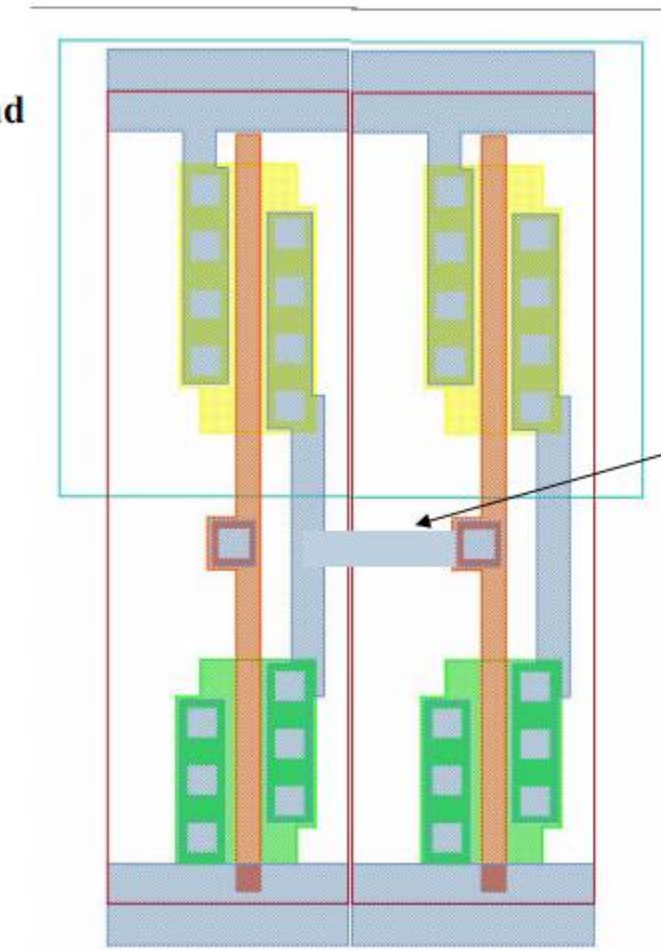


Two Inverters

Share power and ground

Abut cells



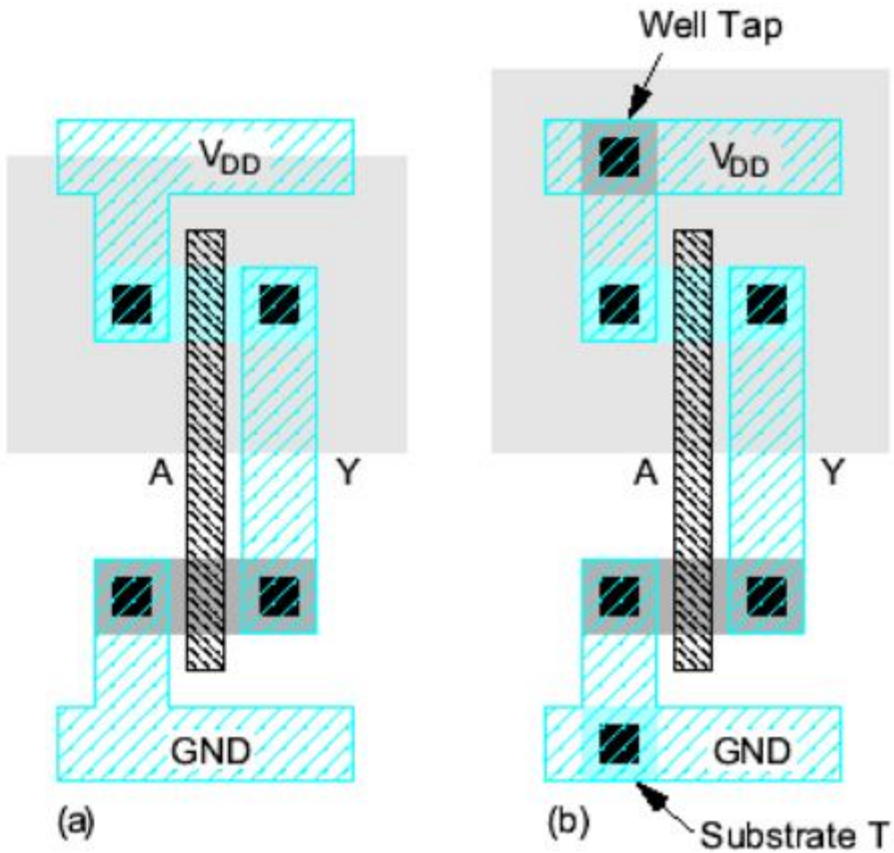


Connect in Metal

Gate Layout

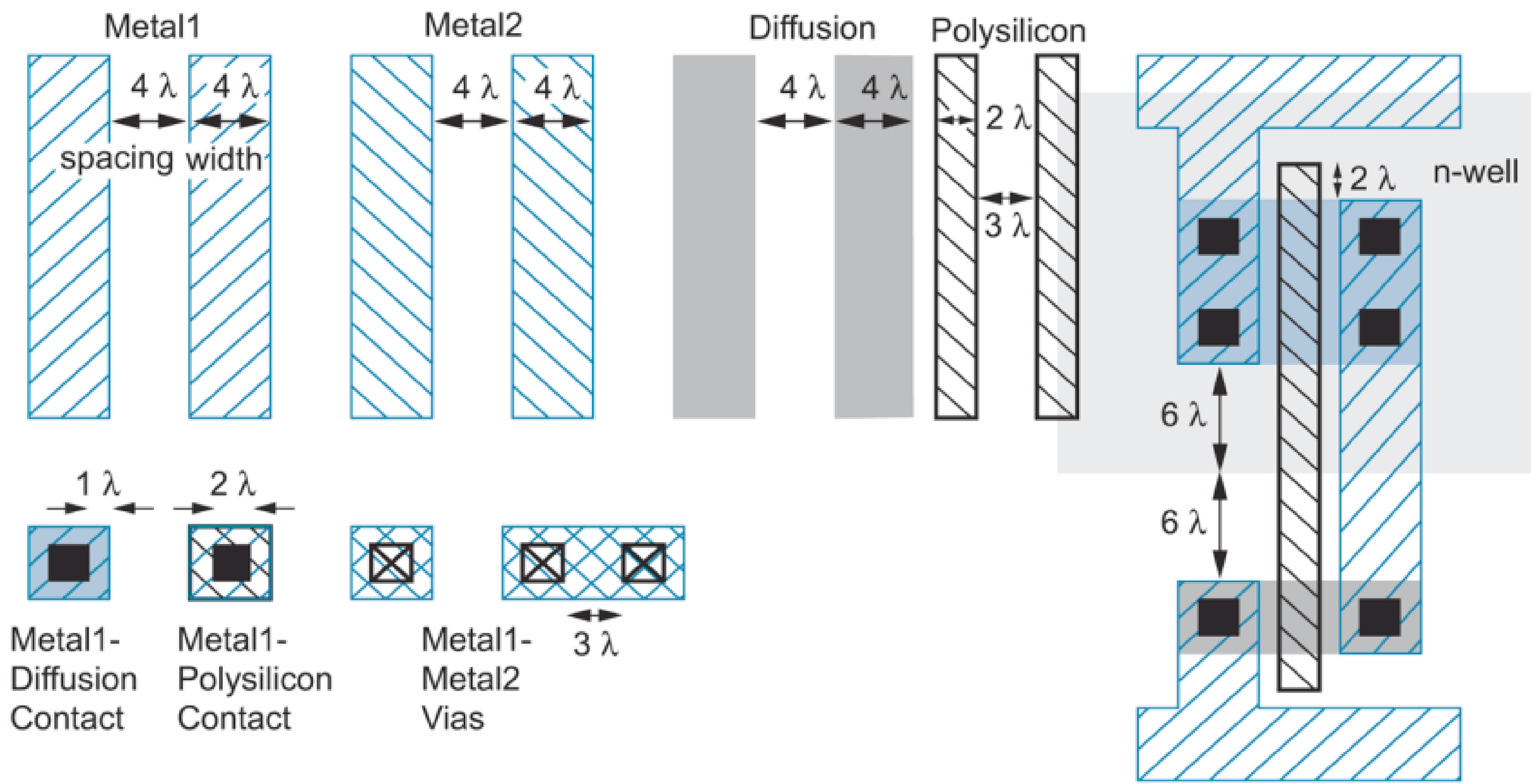
- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - V_{DD} and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts

Example: Inverter



Layout Design Rules

Conservative rules to get started !



Design Rules Summary

- Metal and diffusion have minimum width and spacing of 4λ
- Contacts are 2λ x 2λ and must be surrounded by 1λ on the layers above and below
- Polysilicon uses a width of 2λ
- Polysilicon overlaps diffusions by 2λ where a transistor is desired and has spacing or 1λ away where no transistor is desired
- Polysilicon and contacts have a spacing of 3λ from other polysilicon or contacts
- N-well surrounds pMOS transistors by 6λ and avoid nMOS transistors by 6λ

The power and ground lines are called supply rails

Inverter Layout

- Transistor dimensions specified as W / L ratio
- Minimum size is 4λ / 2λ, sometimes called 1 unit

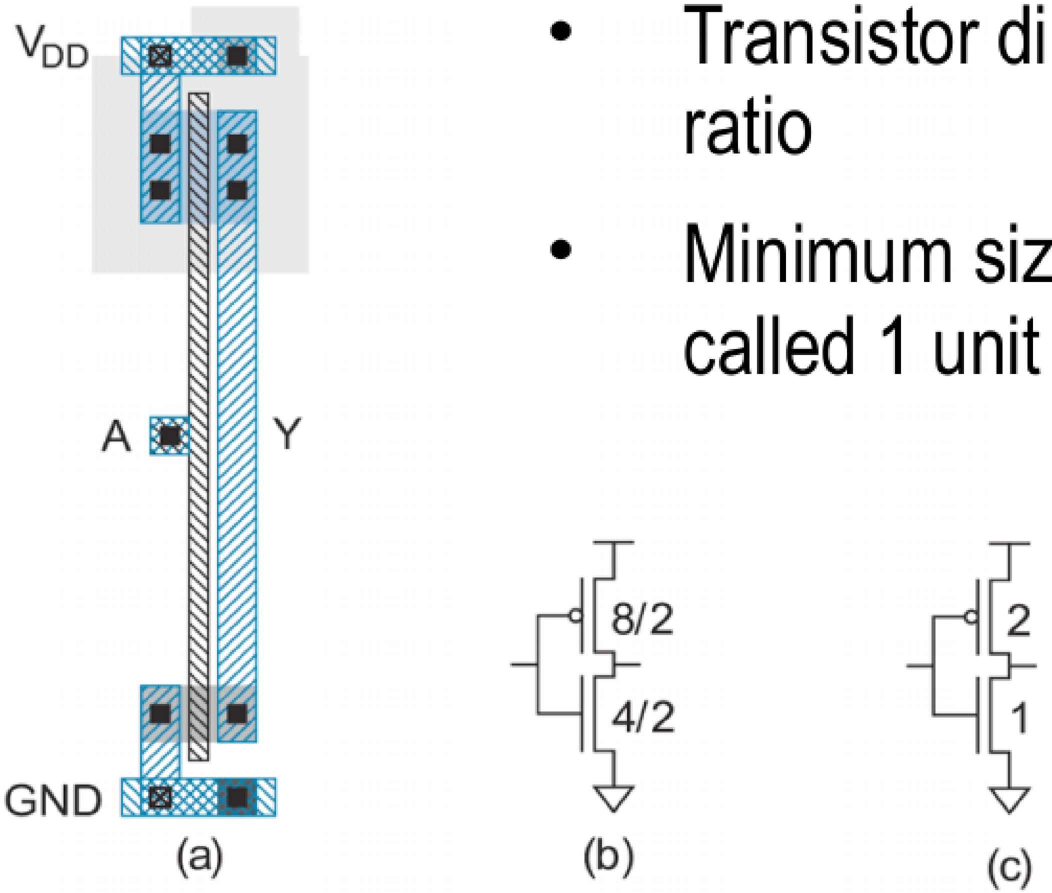
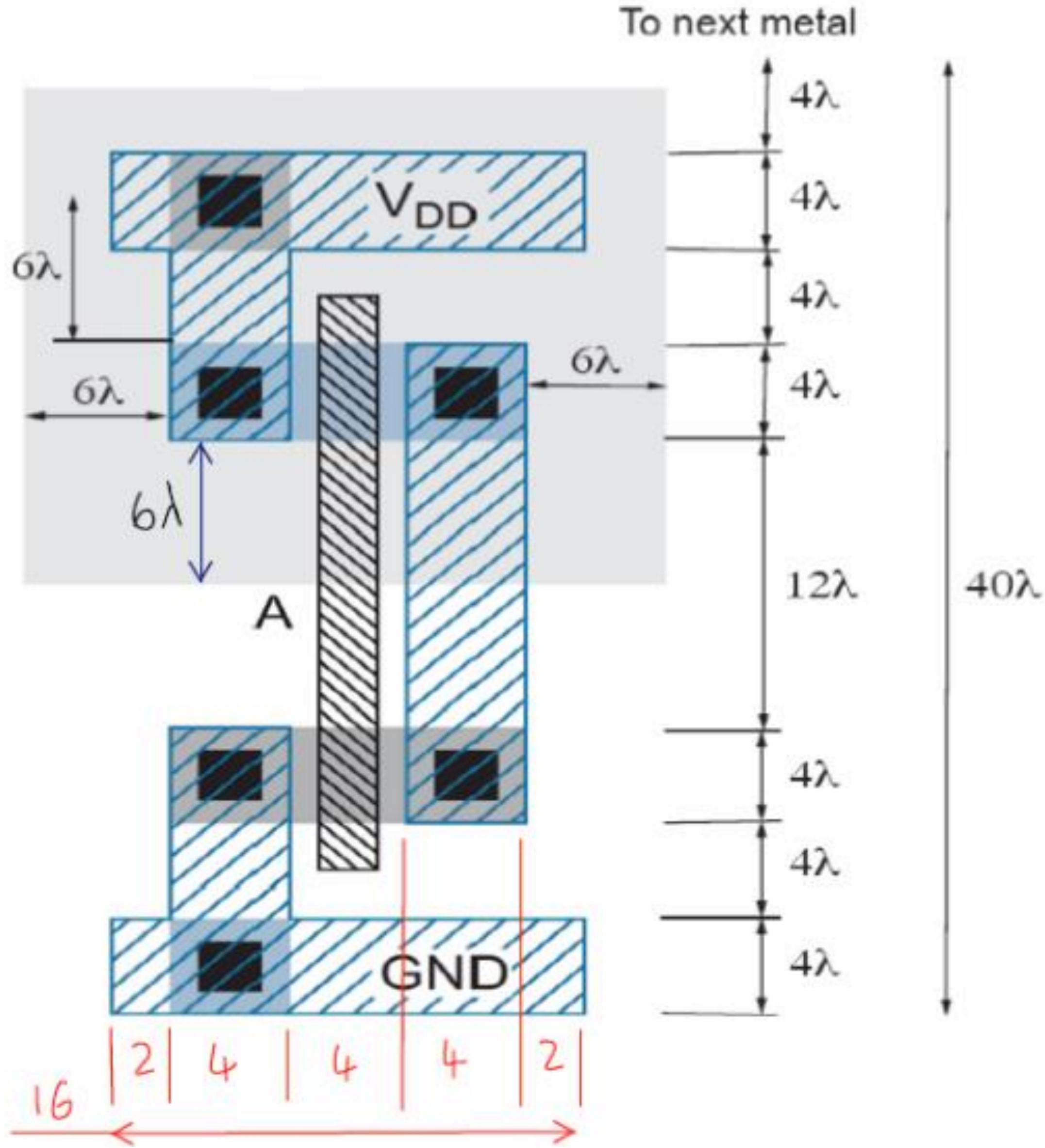
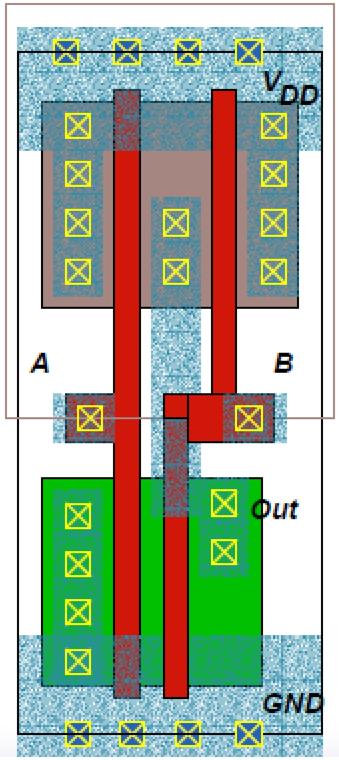


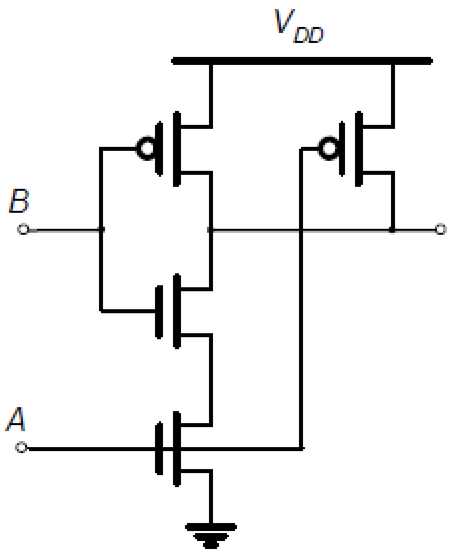
FIG 1.40 Inverter with dimensions labeled

Inverter Standard Cell Area (1/2

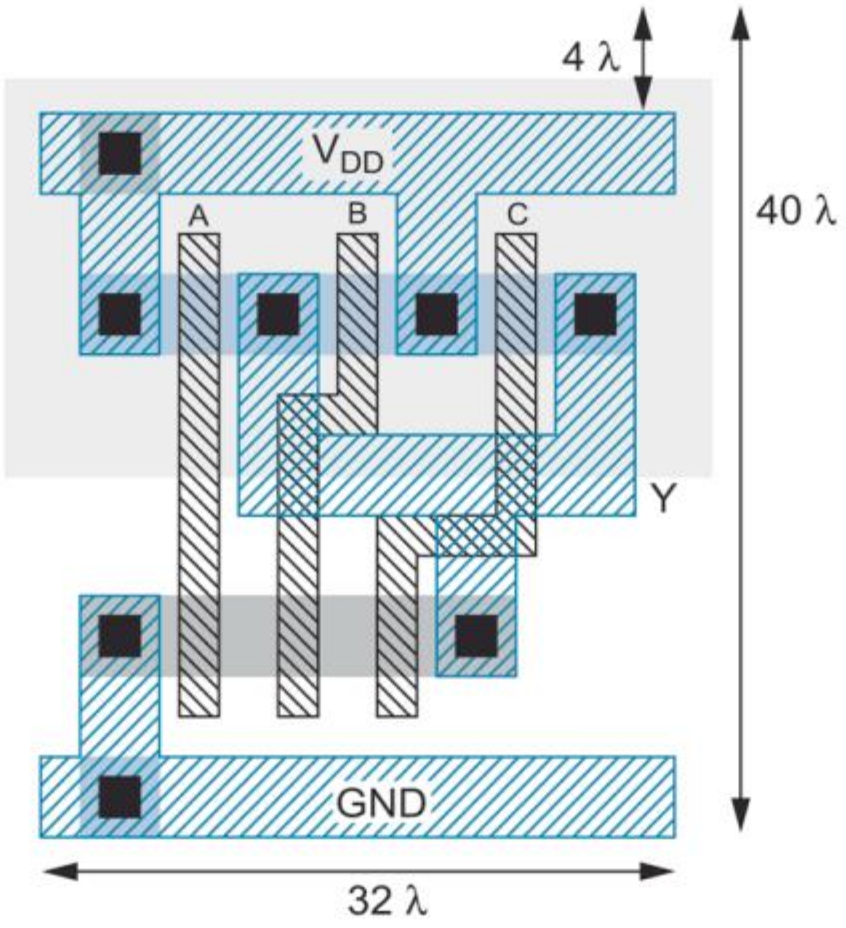




2-input NAND gate

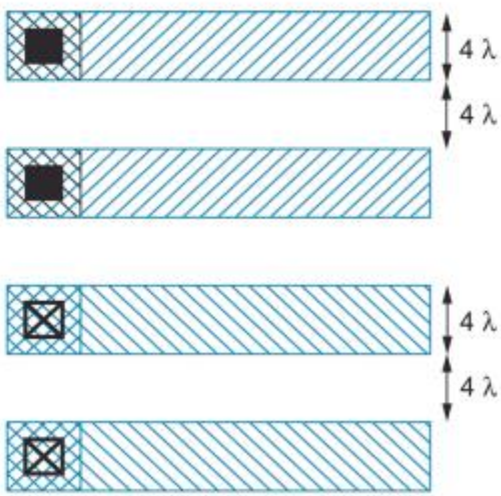


3-input Standard Cell NAND

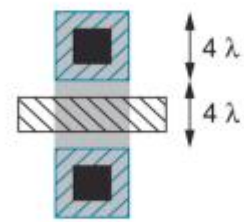


Wiring Tracks

- A **wiring track** is the space required for a wire
  - 4λ width, 4λ spacing from neighbor = 8λ pitch
  - Transistors also consume one wiring track



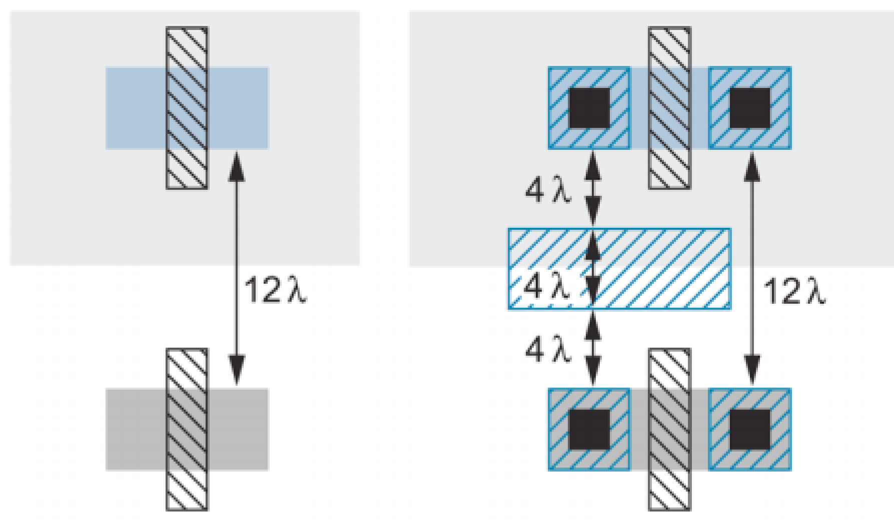
(a)



(b)

Well Spacing

- Wells must surround transistors by 6λ
  - Implies 12λ between opposite transistor flavors
  - Leaves room for one wire track



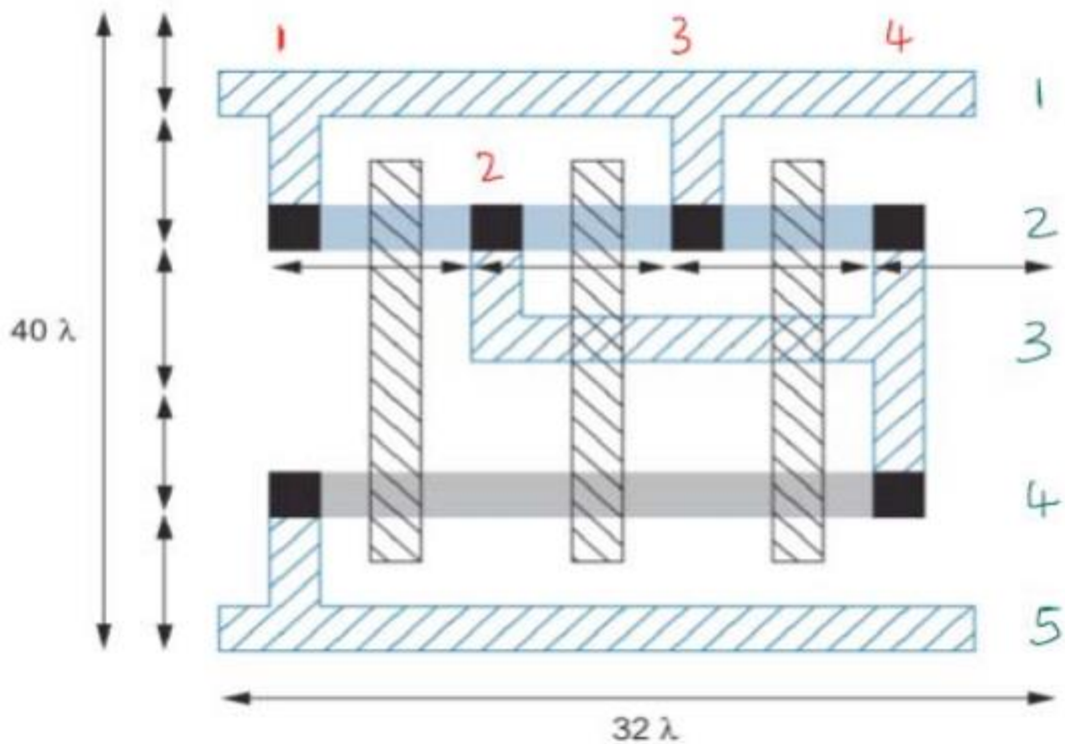
(a) (b)

Area Estimation

Horizontal
$4 \times 8 = 32$

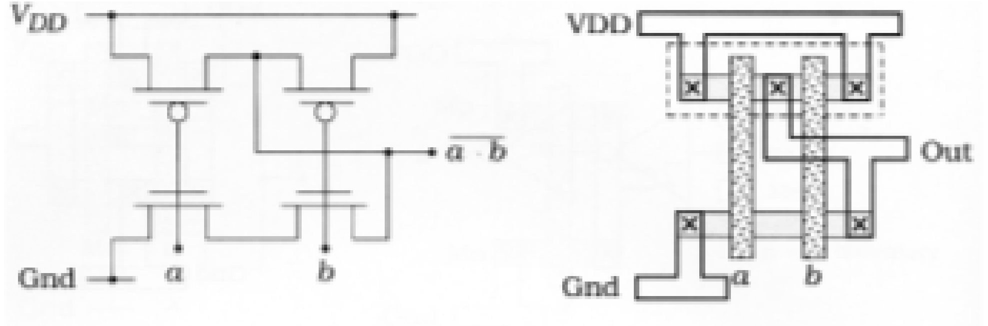
Vertical
$5 \times 8 = 40$

- Estimate area by counting wiring tracks
  - Multiply by 8 to express in λ



Stick Diagram NAND

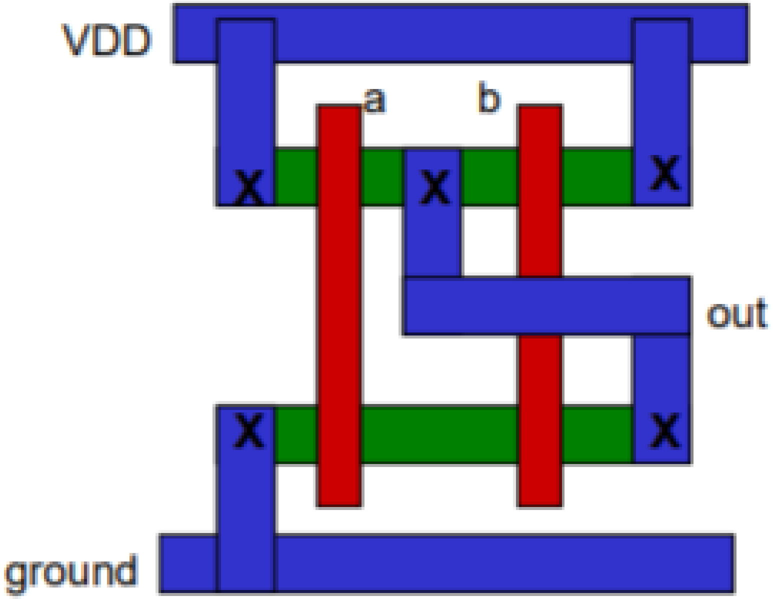
- Simplified NAND Layout
  - several layers not shown



(a) Circuit (b) Layer design

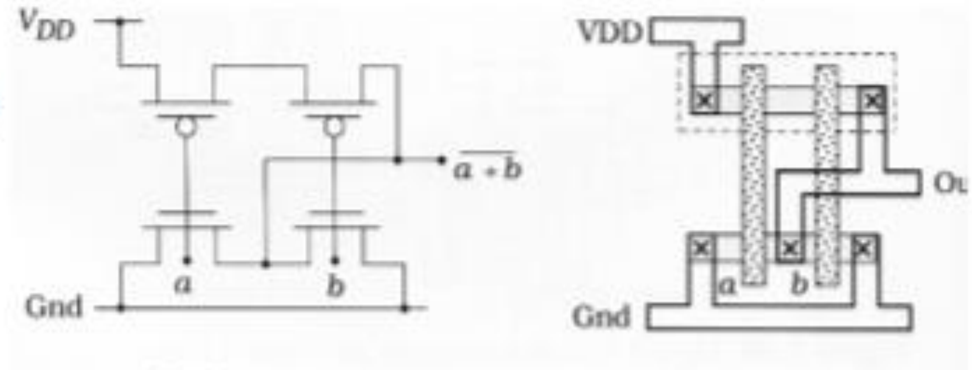
Stick Diagram

- Metal supply rails
  - blue
- n and p Active
  - green
- Poly gates
  - red
- Metal connections
  - supply, outputs
- Contacts
  - black X



Stick Diagram NOR

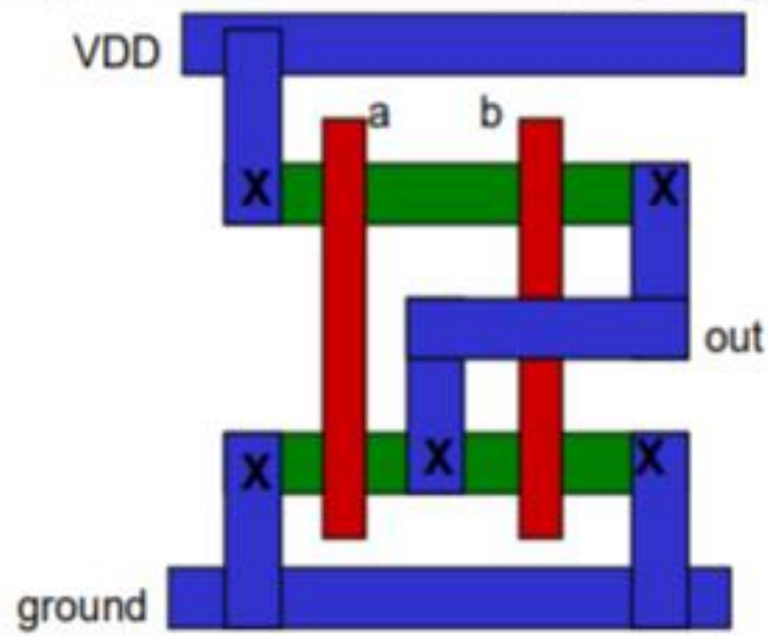
- Simplified NOR Layout
  - several layers not shown



(a) Circuit (b) Layer design

Stick Diagram

- Metal supply rails
  - blue
- n and p Active
  - green
- Poly gates
  - red
- Metal connections
  - supply, outputs
- Contacts
  - black X



Stick Diagrams

- Stick Diagram Rules
  – apply to full layout also

•Poly over Active = tx
nMOS unless in n-well
(or near top/VDD--mostly)

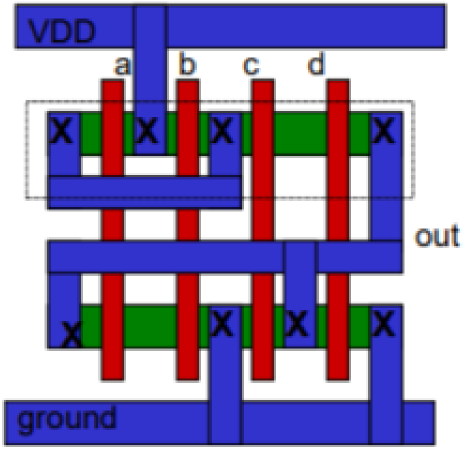
•Poly can cross Metal1 and Metal2

•Metal1 can cross Poly, Active, Metal2

•Metal2 can cross Poly, Active, Metal1

•tx S/D Contact must be on Active-Metal1

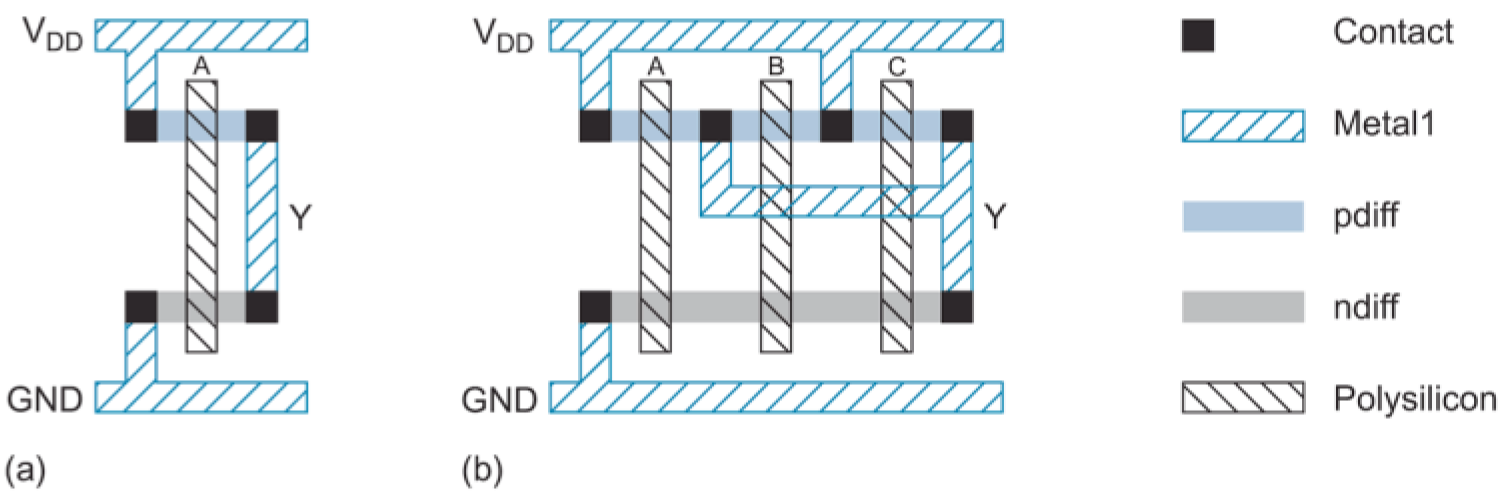
•(poly) Contact must be on Poly-Metal1 •Via connects Metal1 and Metal2



What is this logic function?

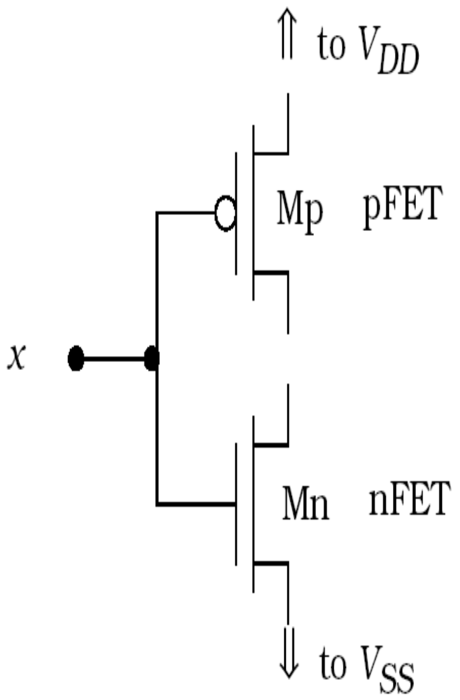
Stick Diagrams

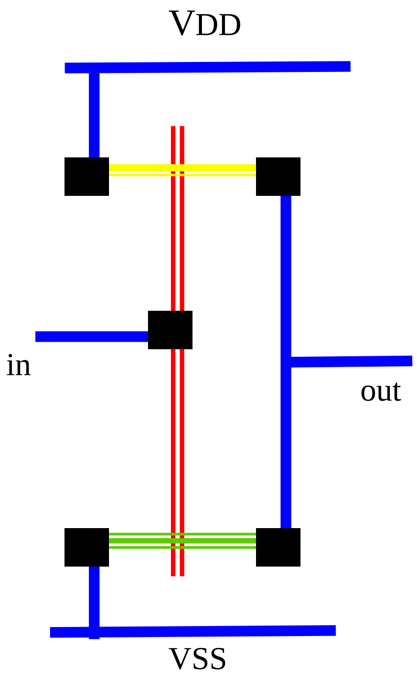
- **Stick diagrams** help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or dry-erase markers

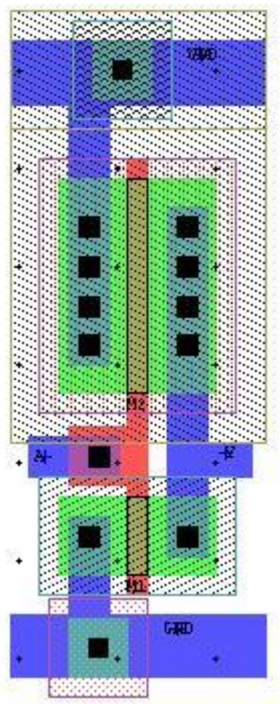


CMOS Inverter Stick Diagrams

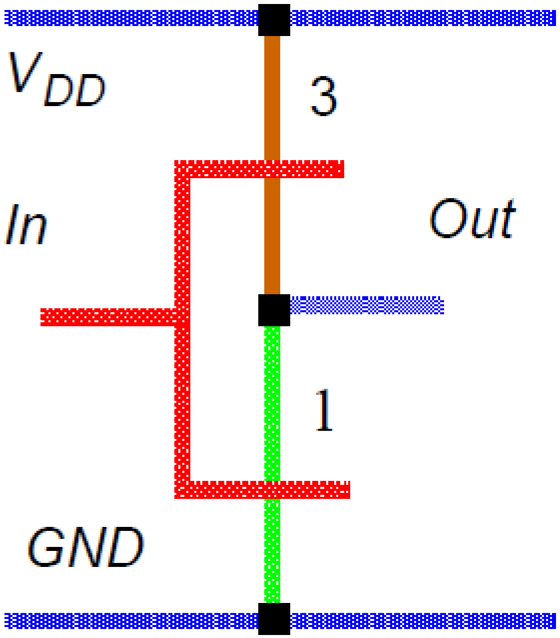
- **CMOS inverter described in other way.**







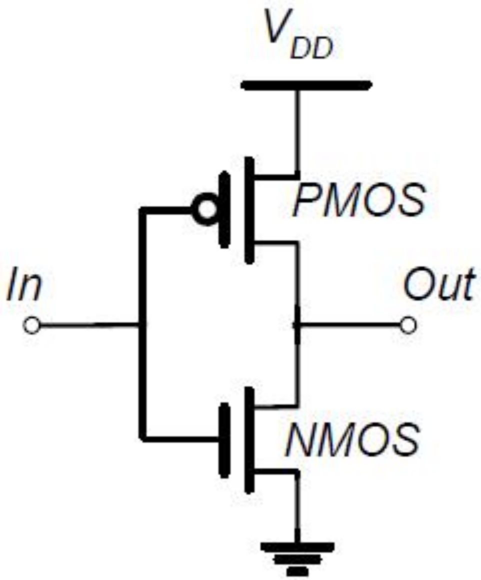
Sticks Diagram

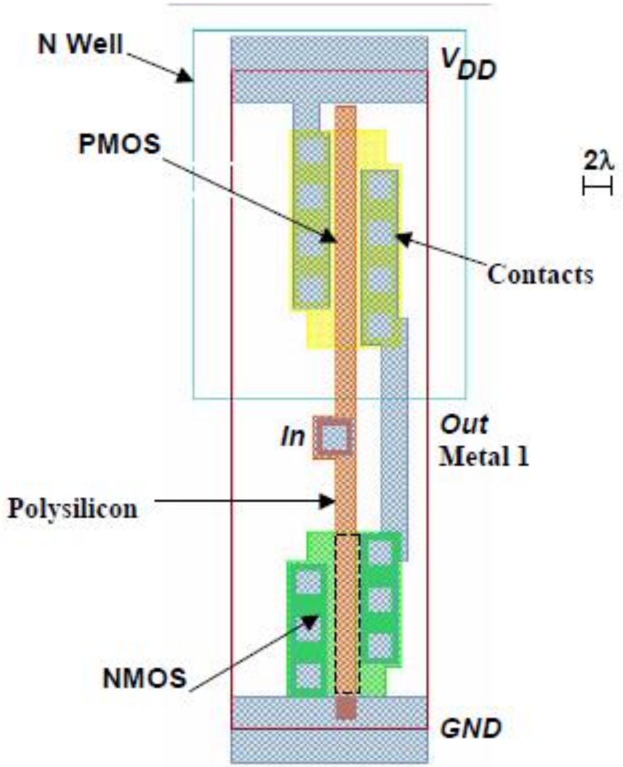


Stick diagram of inverter

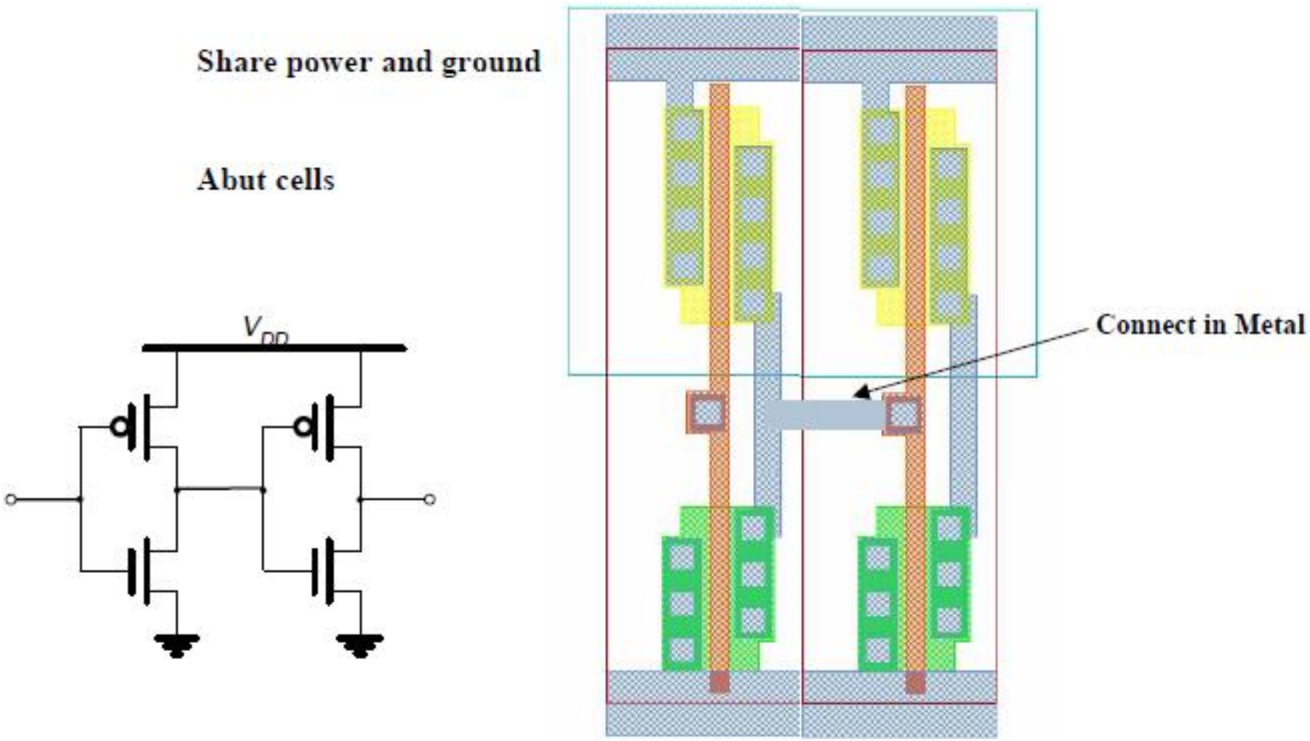
- Dimensionless layout entities
- Only topology is important
- Final layout generated by "compaction" program

CMOS Inverter



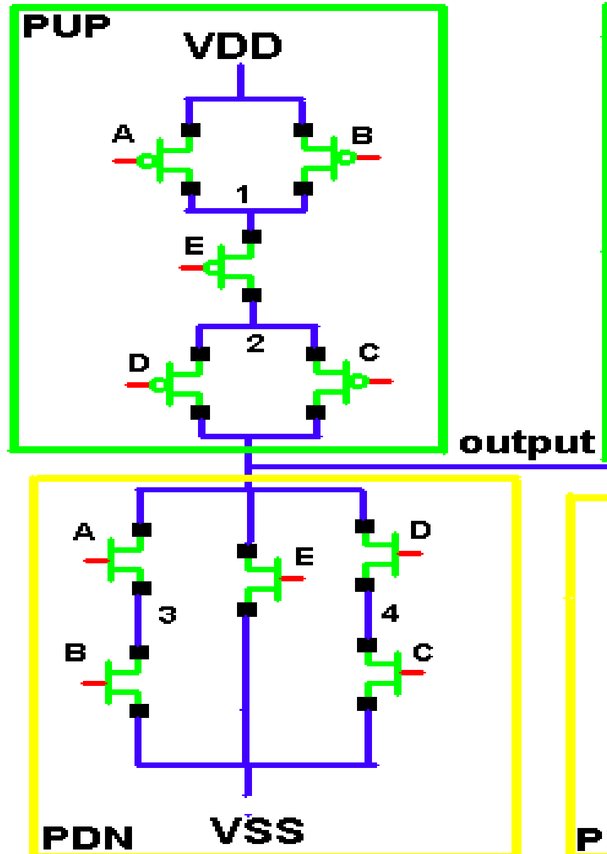


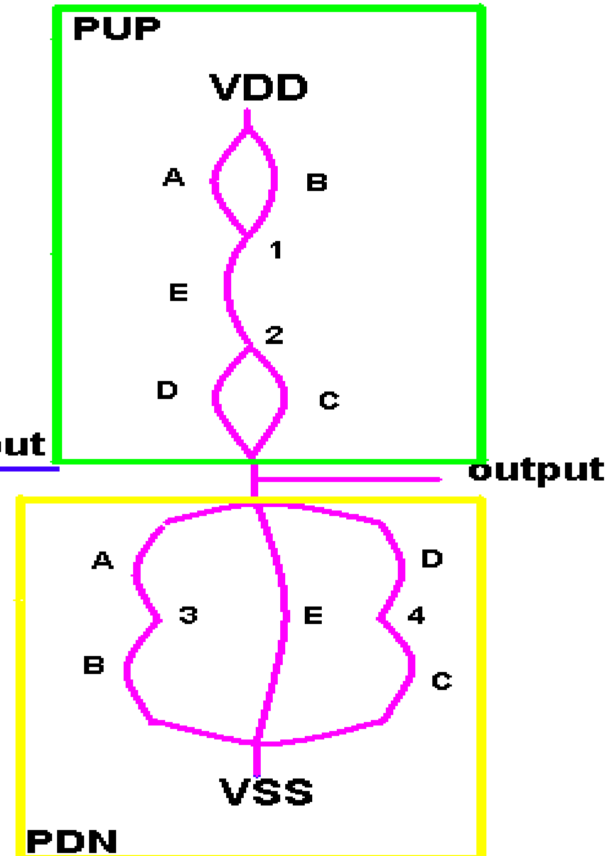
Two Inverters



Stick Diagram

$F = (AB)+E+(CD)$



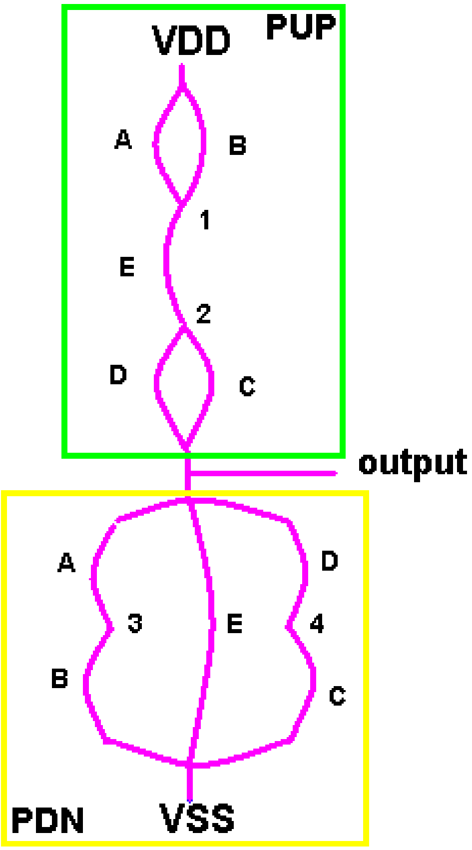


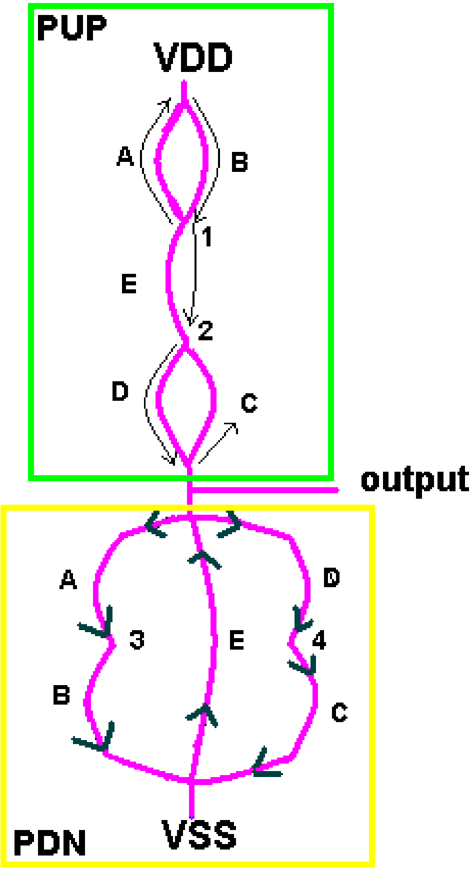
Identify each transistor and connection to the transistor by a unique name

construct a logic graph

F = (AB)+E+(CD)

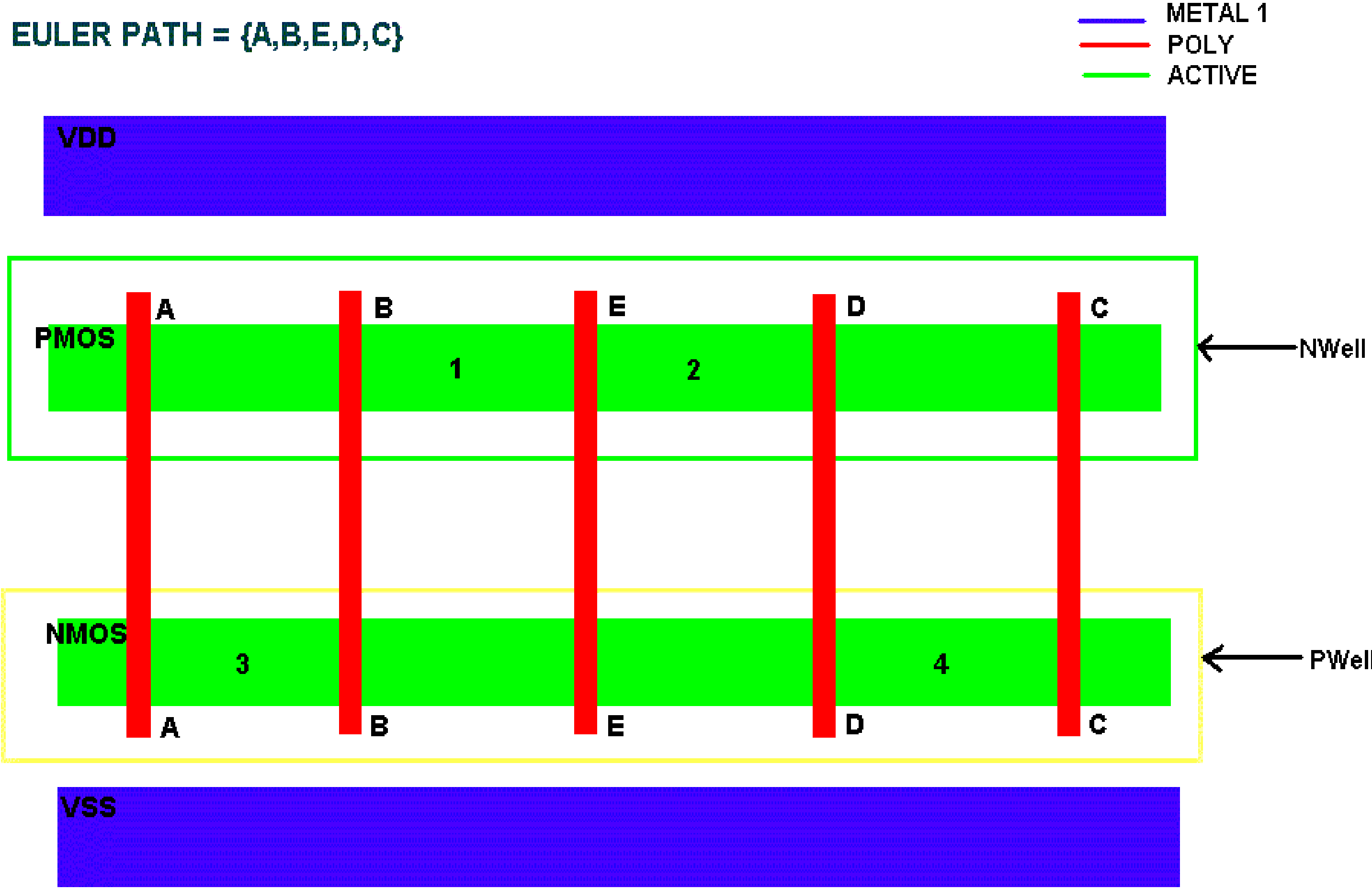
See the tutorial for further details.





EULER PATH = {A,B,E,D,C}

- construct one Euler path for both the Pull up and Pull down network

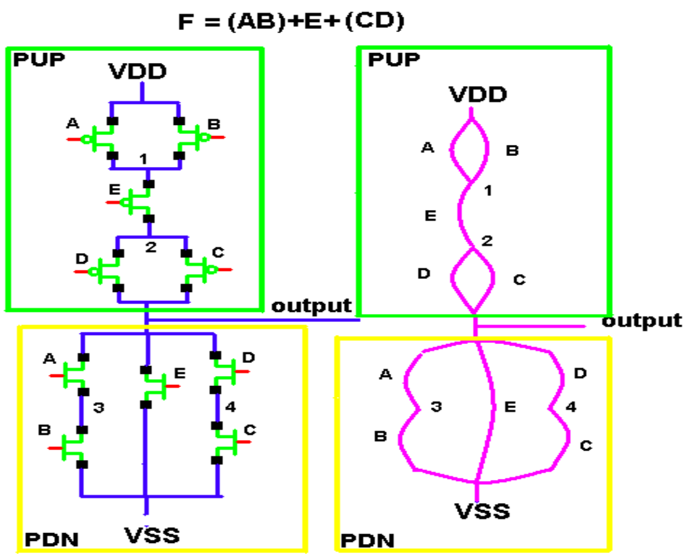


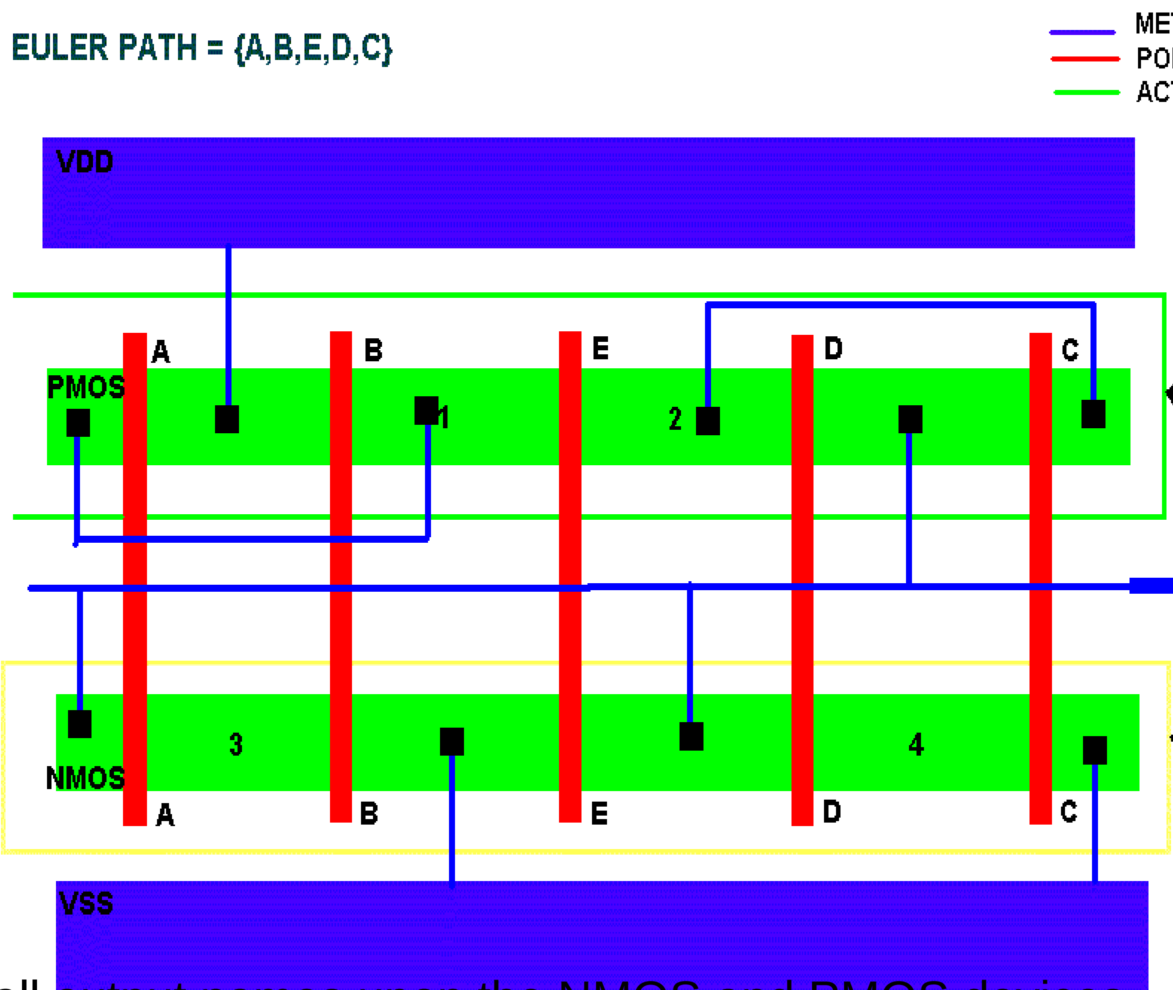
-Trace two green lines horizontally to represent the NMOS and PMOS devices and surround them by n and p-wells

-Trace the number of inputs (5 in this example) vertically across each green strip and label them in order.

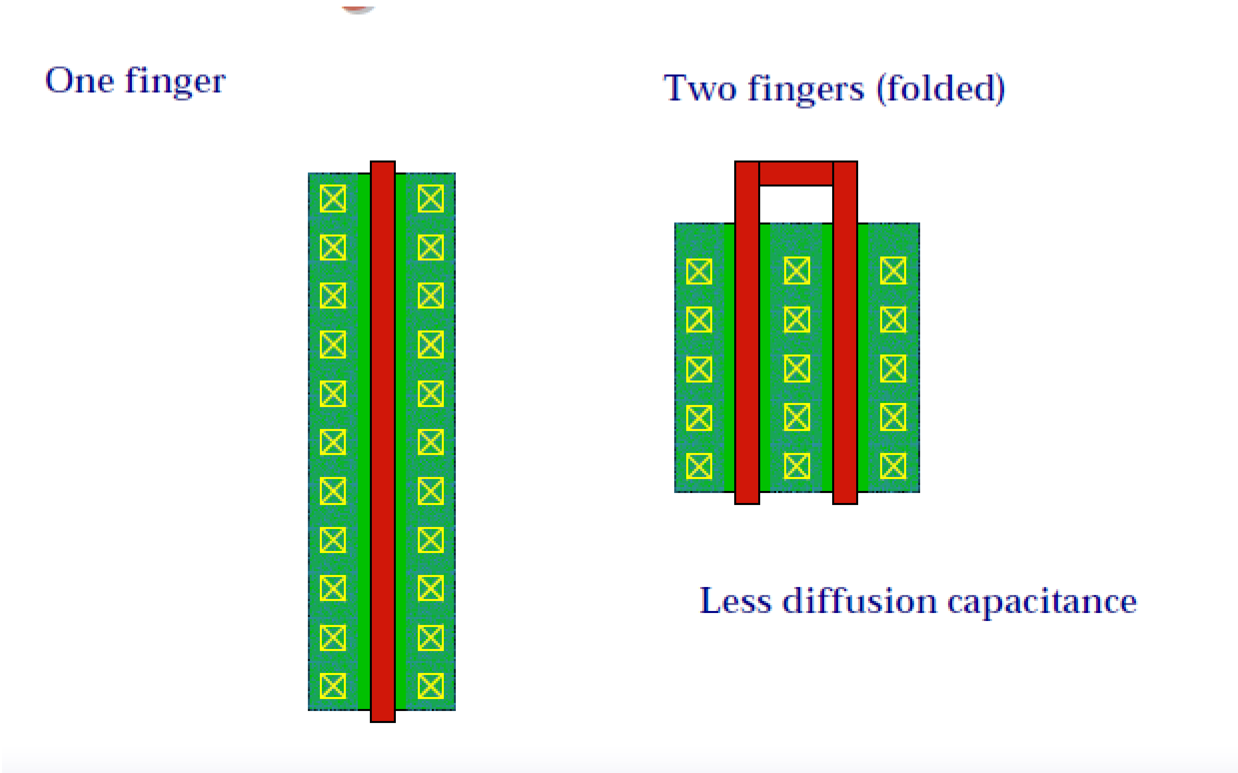
-Trace blue lines to represent VDD and VSS

-Place the connection labels upon the NMOS and PMOS devices

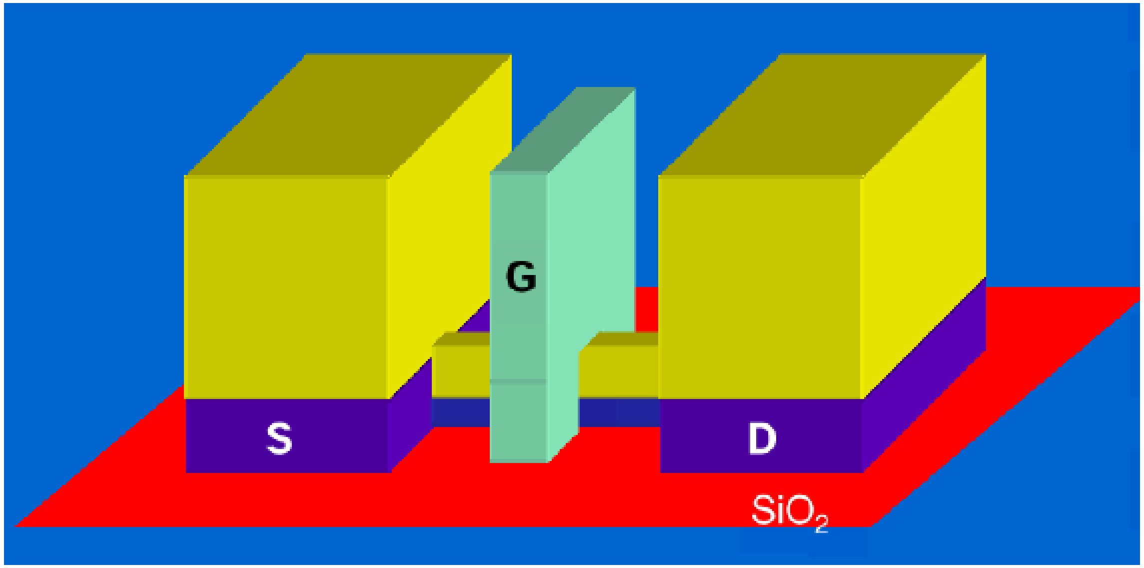




-Place the VDD, VSS and all output names upon the NMOS and PMOS devices
-interconnect the devices based on Euler path.

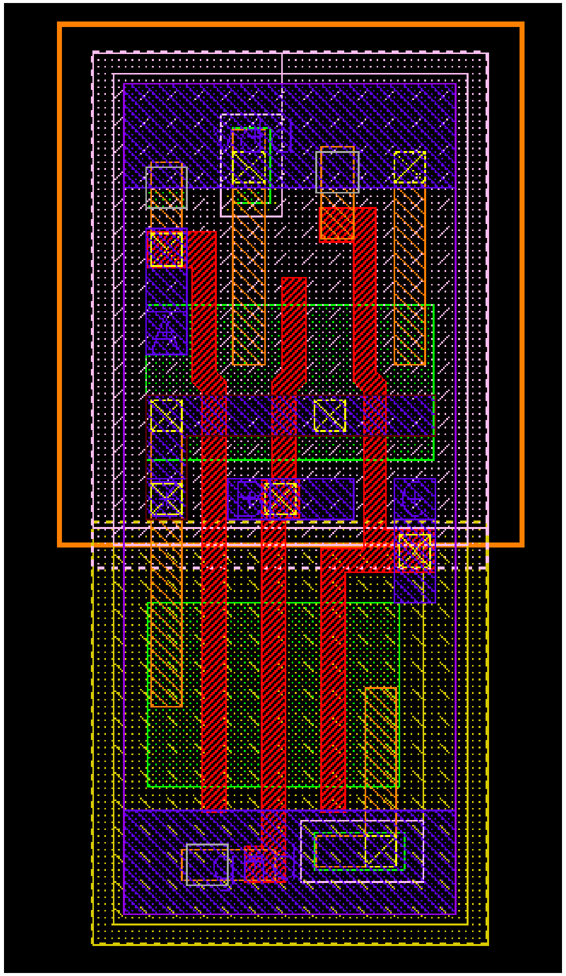

One finger
Two fingers (folded)
Less diffusion capacitance

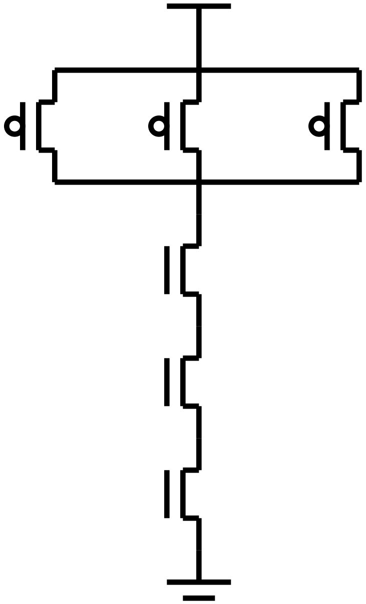
Future device



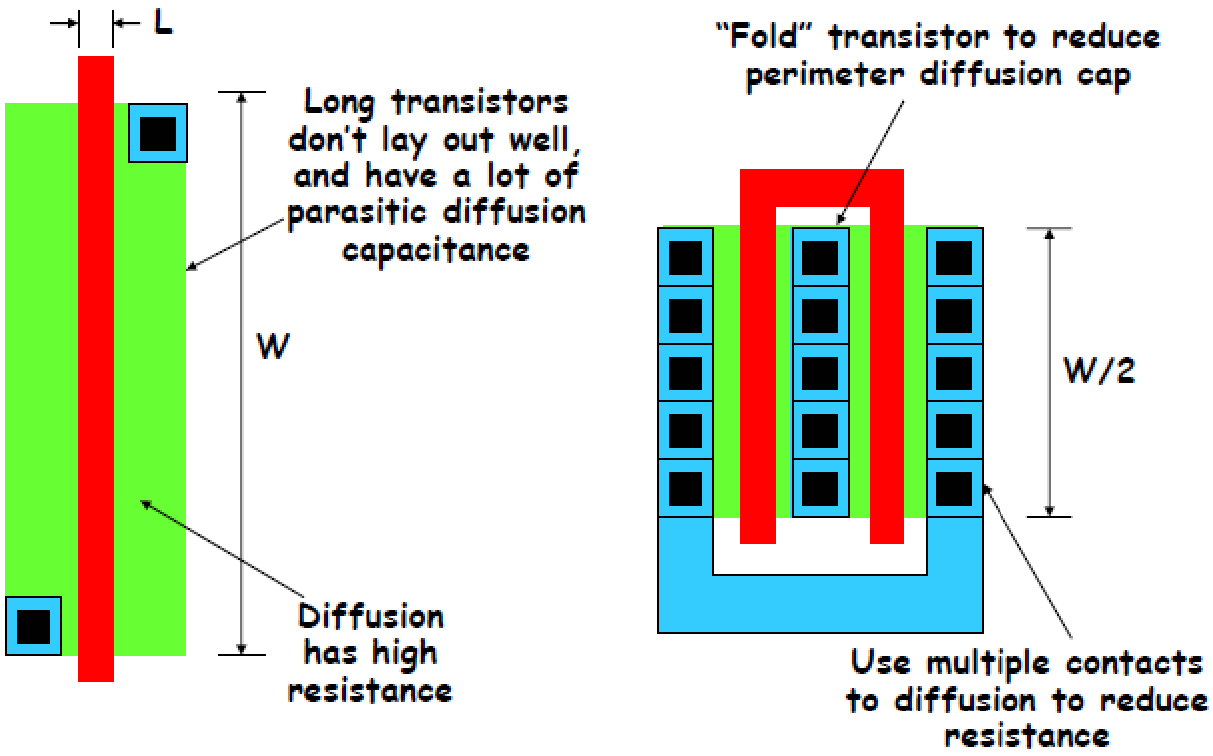
25 nm MOS transistor (Folded Channel)

Layout vs. Schematic

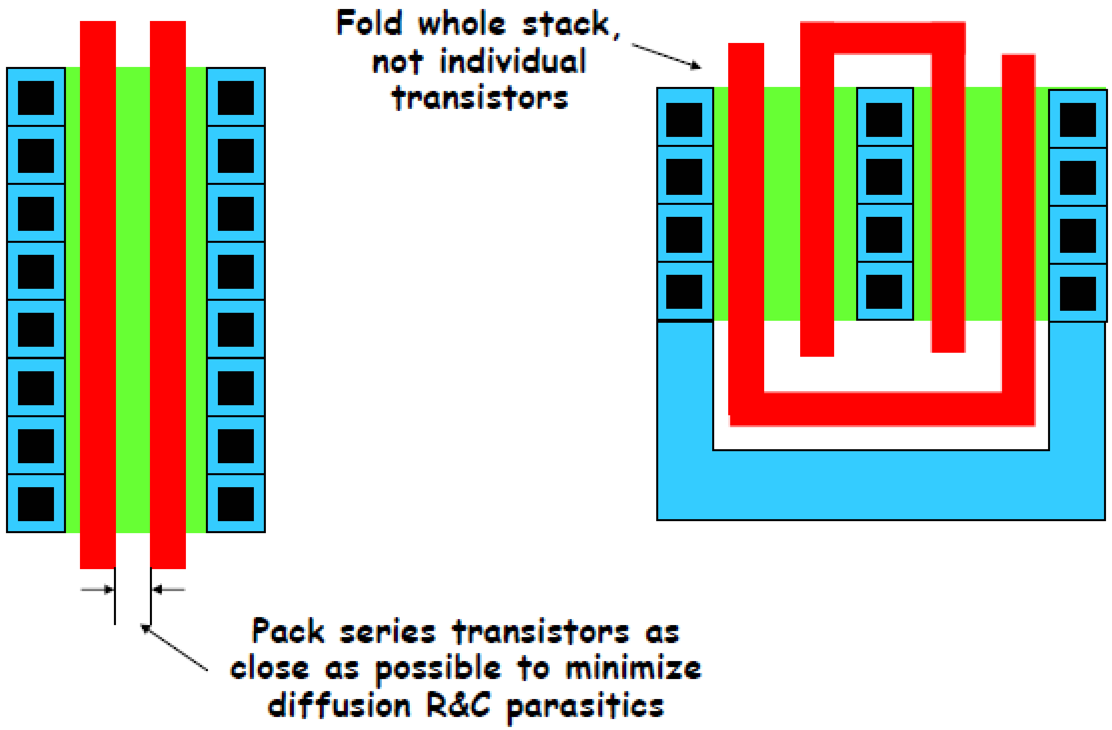




Gate Layout Tricks

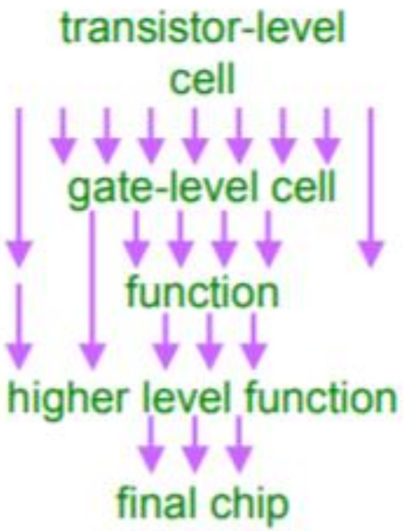


Gate Layout Tricks



Cell Hierarchy and Instancing

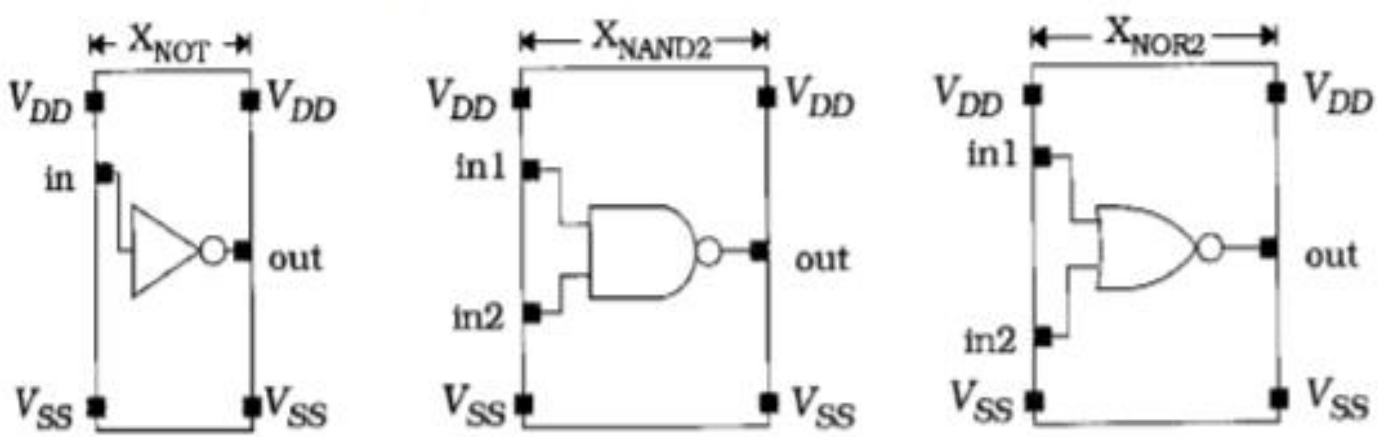
- Hierarchical Design
  - transistors used to build gates
  - gates used to build logic functions
  - logic functions used in larger blocks
  - build up in this manner to final chip level



- Each physical design file is called a "cell"
  - basic cells can be used to create a "cell library"
    - elements of the cell library used to create all higher level cells
  - lower level cell is called an "instance"
  - construct functions by "instancing" cells into higher level cells
    - details of the cell is left inside the lower level cell file
    - information is not copied, but referenced

Cell Concept

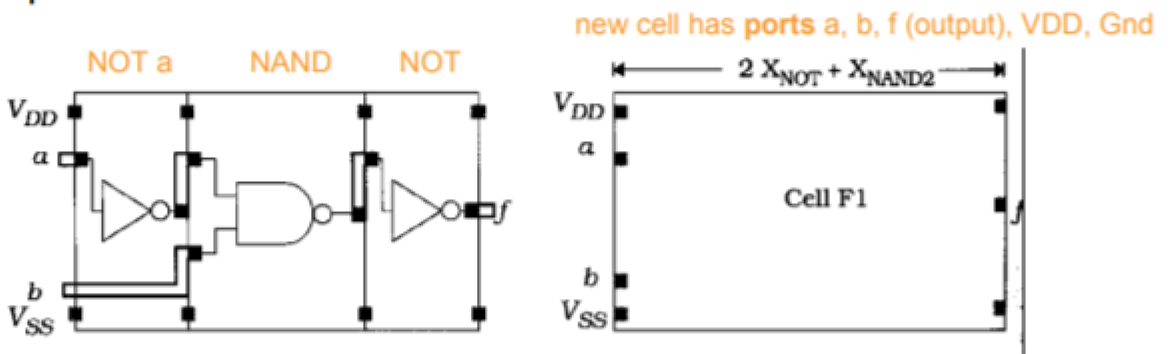
- Instancing
  - construct all blocks using instances of lower level cells
    - tx-level cells are called "primitives" (lowest level cells)
  - allow layout optimization within each cell
  - eases layout effort at higher level
    - higher level layout deal with interconnects rather than tx layout
- Cell View
  - see only I/O ports (including power), typically in Metal1
  - can't see internal layer polygons of the primitive



Instancing

- Ports
  - – all signals that connect to higher level cells
  - – physical locations of the layout cell, typically in Metal1 or Metal2
- Metal1 vs Metal2 ports
  - – best to keep ports in Metal1 for primitives
  - – always try to use only the lowest level metals you can
- Building Functions from Primitives
  - – instantiate one or more lower-level cells to from higher-level function

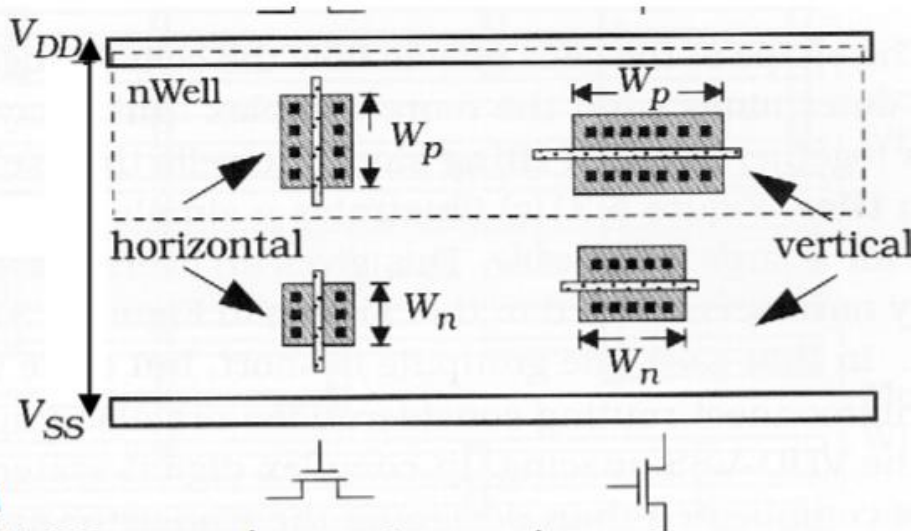
- Example: $f = \overline{a}\, b$



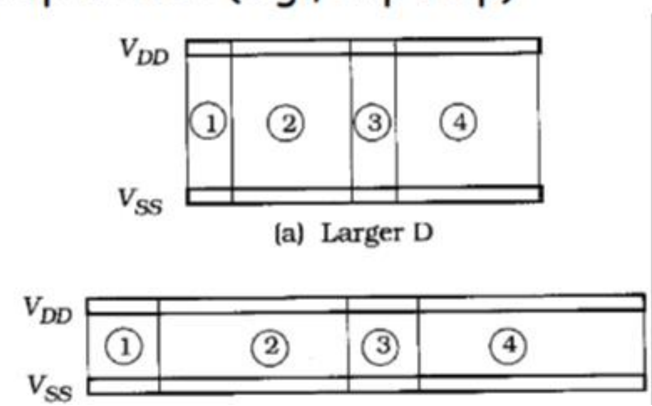
(a) Primitive cells (b) New complex cell

Cell Pitch

- Pitch = cell height
  - Official Definition
    - from middle of VDD rail to middle of Gnd rail
  - Our Definition
    - from top of VDD to bottom of Gnd

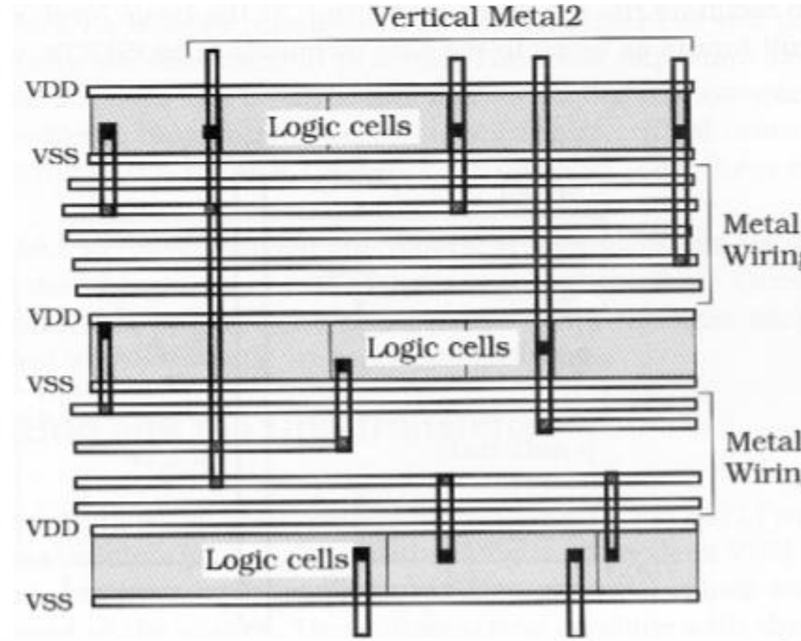


  - Considerations to set pitch
    - fix height for pMOS tx, nMOS tx, and some internal routing
    - fix height to match height of more complex cell (e.g., flip flop)
- Transistor Orientation
  - Horizontal (tx W run vertically)
    - pitch sets max tx W
    - cells taller & narrow
  - Vertical (tx W runs horizontally)
    - can increase tx W with fixed pitch
    - cells short & wide

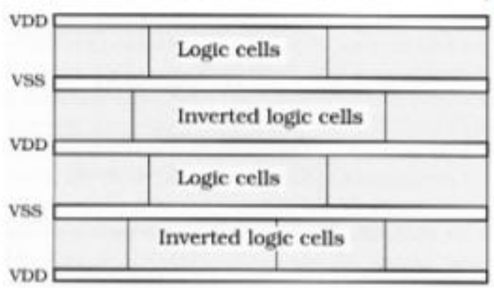


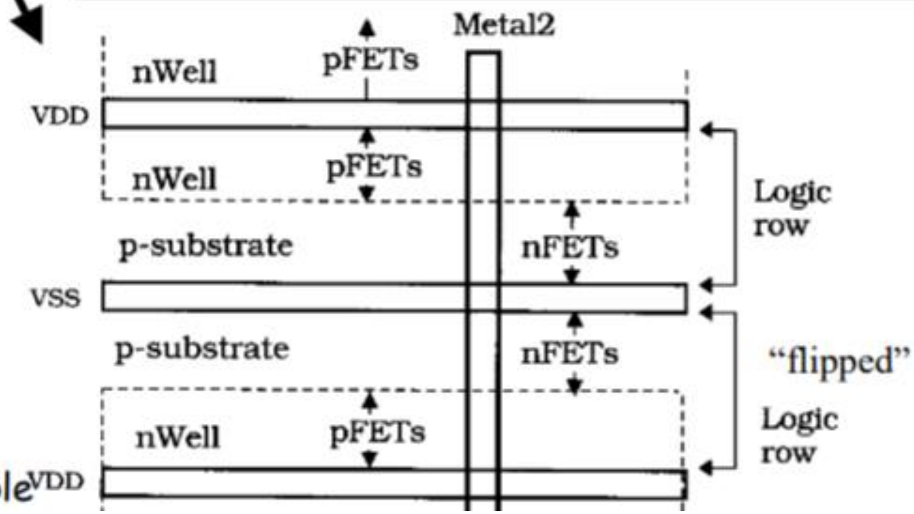
Cell Routing

- Metal1 routing strategy
  - ☻ – very flexible
  - ☻ – requires fewer metal layers
  - ☹ – demands much chip area for routing



- High-level metal routing strategy
  - ☻ – allows high density tx packing
  - ☻ – minimum chip area for routing
  - ☹ – demands several metal layers



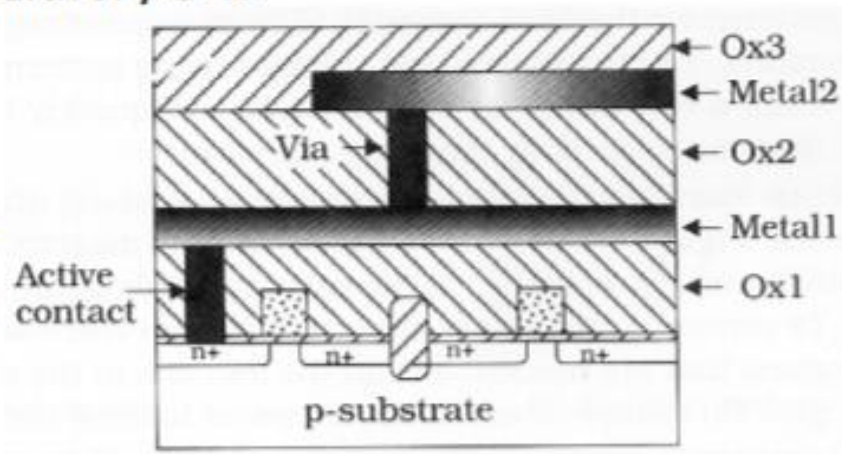


- Inter-cell routing
  - – always use lowest level interconnect possible

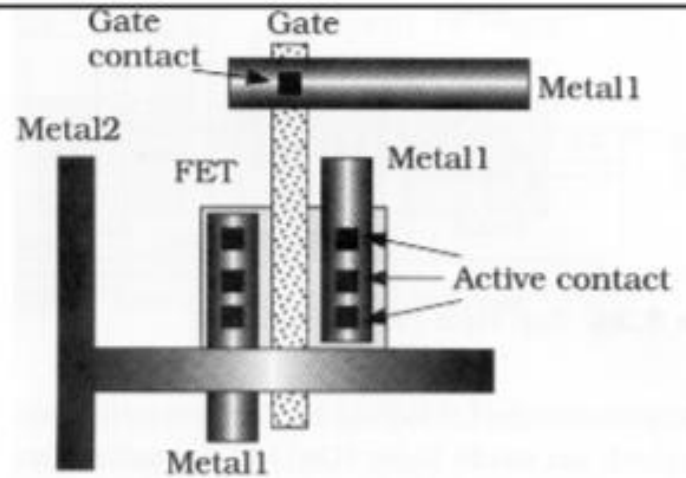
Upper CMOS Layers

- Cover lower layers with oxide insulator, Ox1
- Contacts through oxide, Ox1
  - metal1 contacts to poly and active
- Metal 1
- Insulator Ox2
- Via contacts
- Metal 2
- Repeat insulator/via/metal

only Metal 1 has direct contact to lower layers

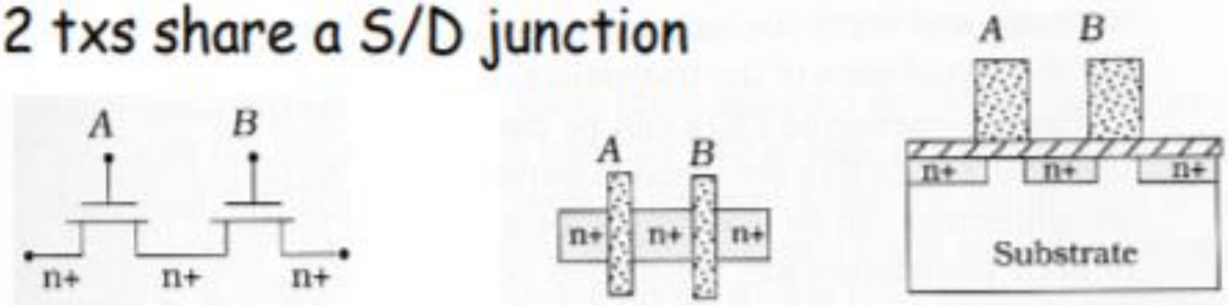


- Full Device Illustration
  - active
  - poly gate
  - contacts (active & gate)
  - metal1
  - via
  - metal2



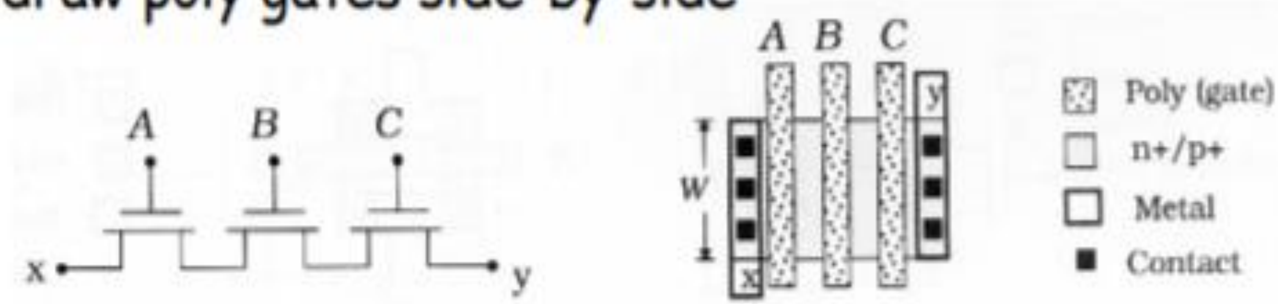
Series MOSFET Layout

- Series txs
  - 2 txs share a S/D junction



(a) Schematic (b) Surface pattern (c) Side view

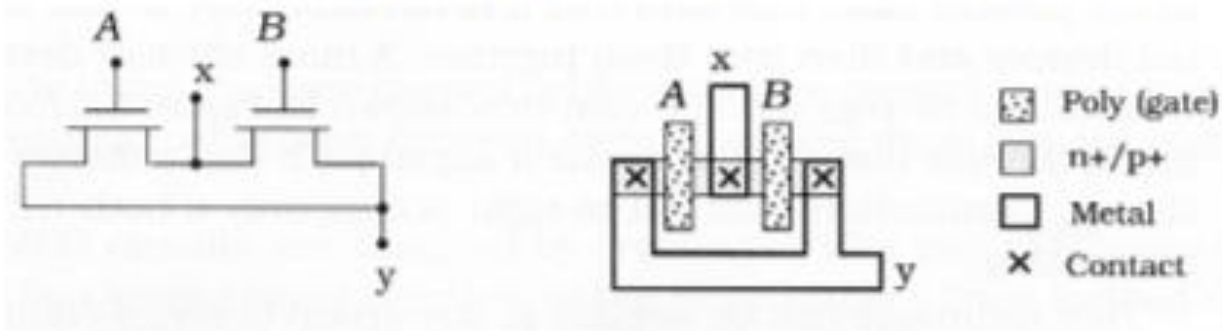
- Multiple series transistors
  - draw poly gates side-by-side



(a) Schematic (b) Surface pattern

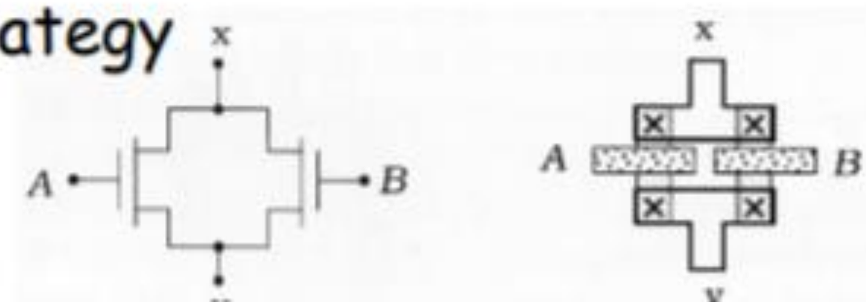
Parallel MOSFET Layout

- Parallel txs
  - one shared S/D junction with contact
  - short other S/D using interconnect layer (metal1)



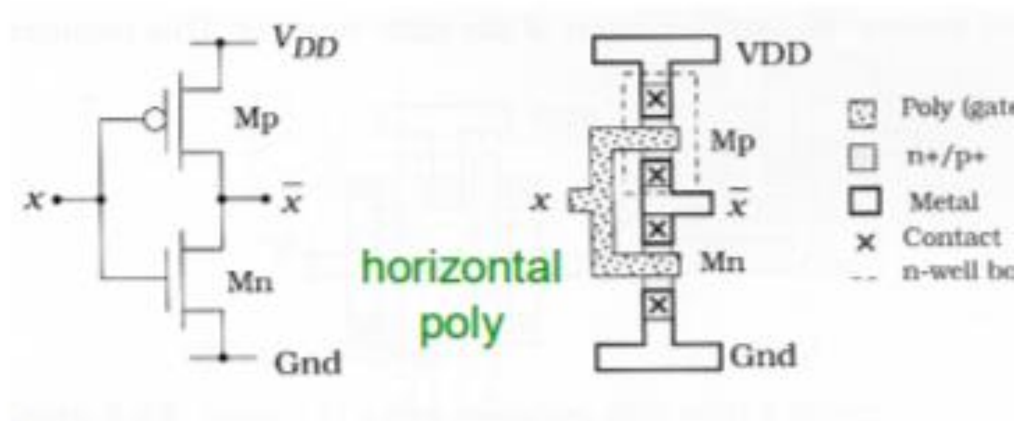
(a) Schematic (b) Surface pattern

- Alternate layout strategy
  - horizontal gates

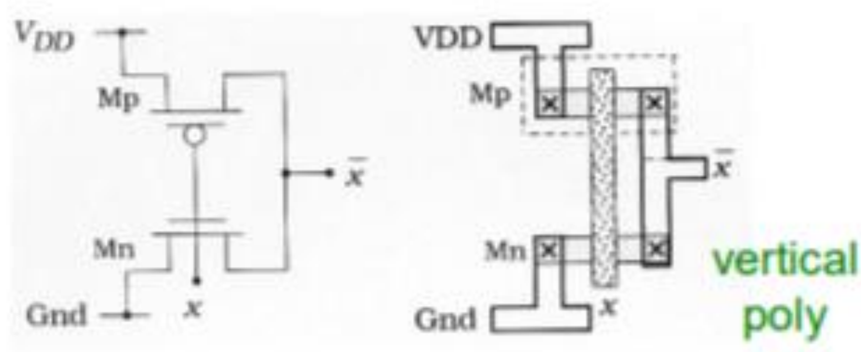


Inverter Layout

- Features
  - VDD & Ground 'rail'
    - using Metal1 layer
  - N-well region
    - for pMOS
  - Active layers
    - different n+ and p+
  - Contacts
    - n+/p+ to metal
    - poly to metal
- Alternate layout
  - advantage
    - simple poly routing
  - disadvantage
    - harder to make W large



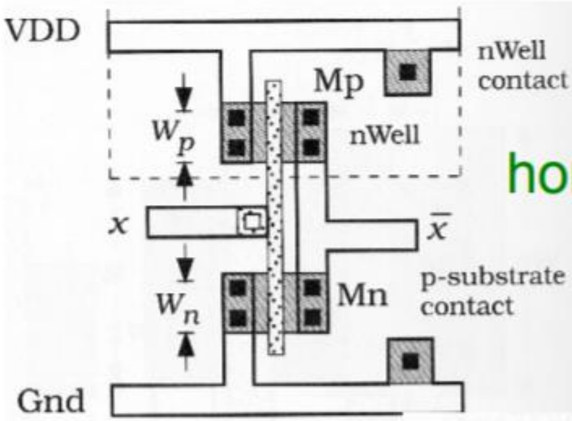
(a) Circuit (b) Layer patterning



(a) Circuit (b) Layer patt

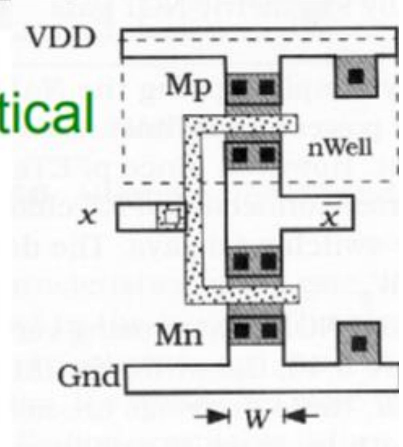
Inverter Layout Options

- Layout with Horizontal Tx
  - pitch sets max tx size
- Layout with Vertical Tx
  - allows scaling without changing pitch
- Vertical Tx with 2x scaling
- Vertical Tx with Rn=Rp scaling

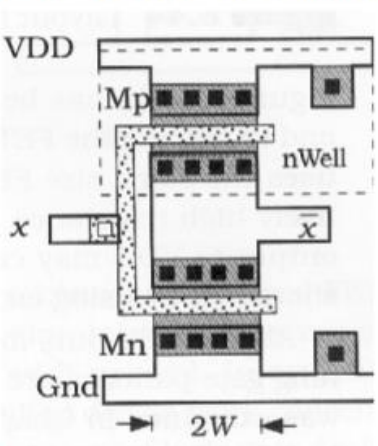


horizontal

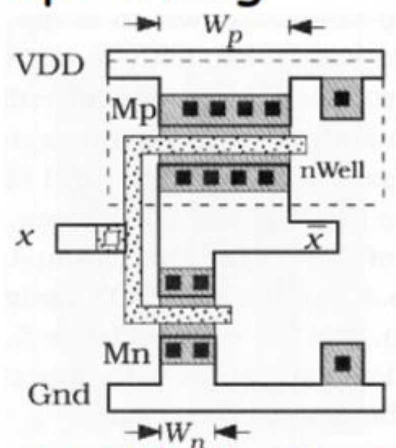
vertical



(a) Basic cell



(b) 2X cell



matched, Rn=Rp

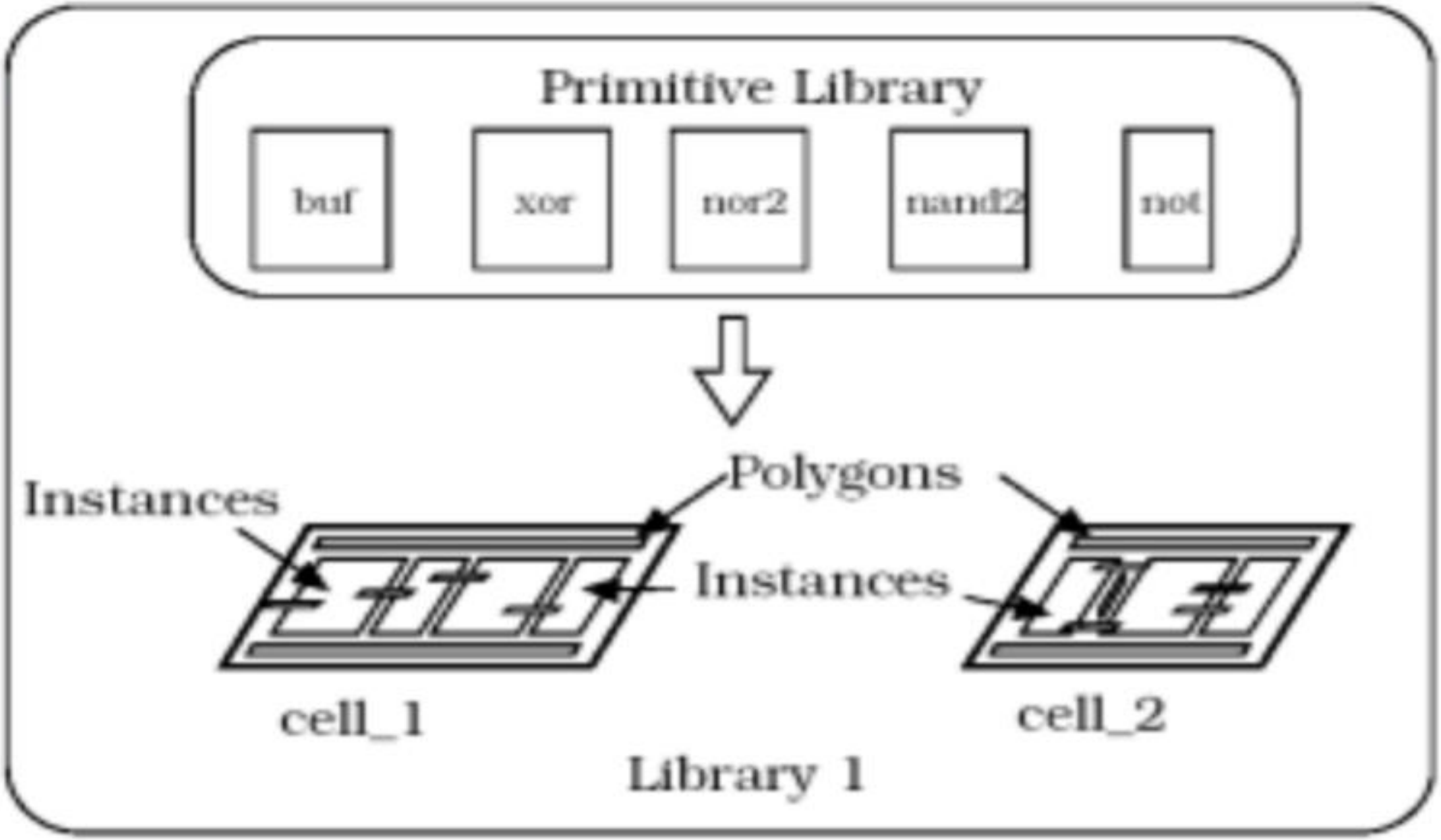


Figure 5.49 (p. 186)
Expanding the library with more complex cells.

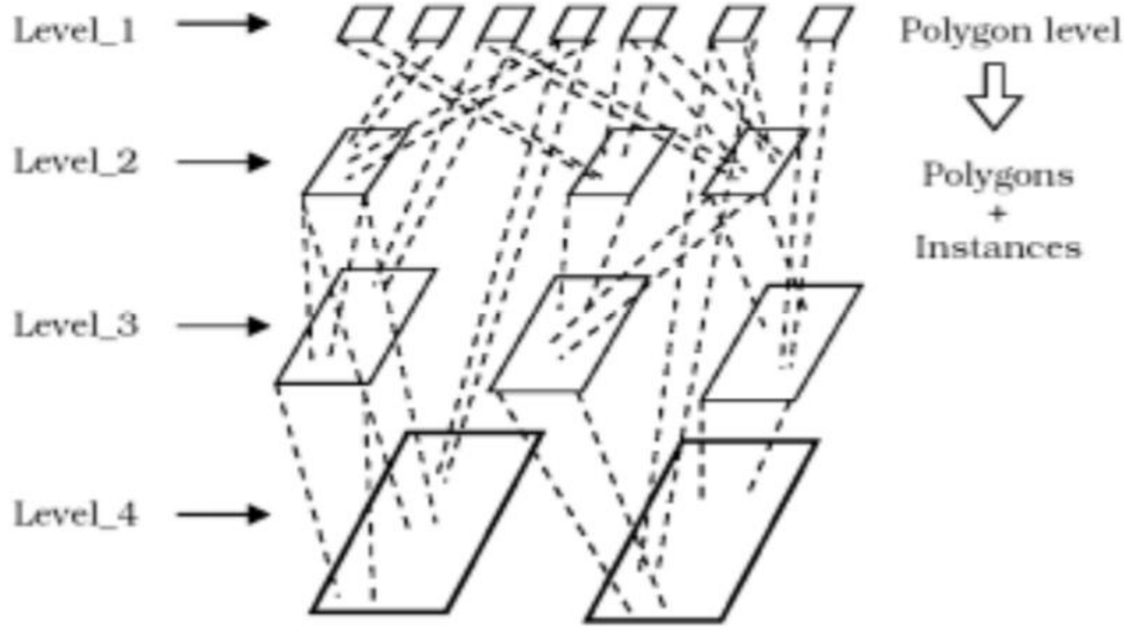
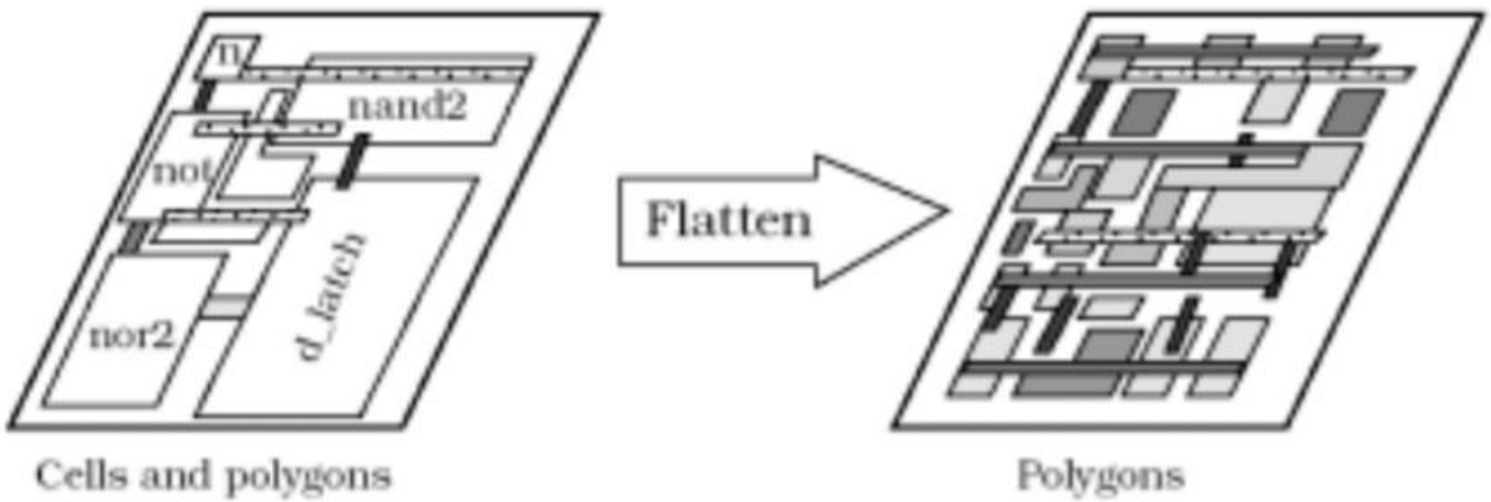
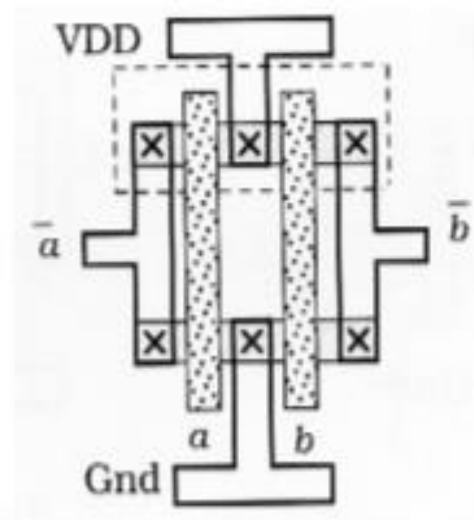


Figure 5.50 (p. 186)
Cell hierarchy.

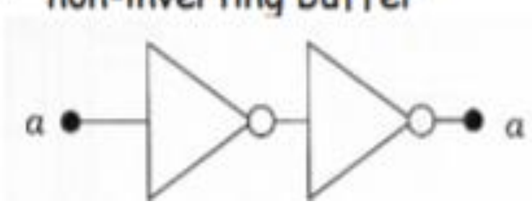


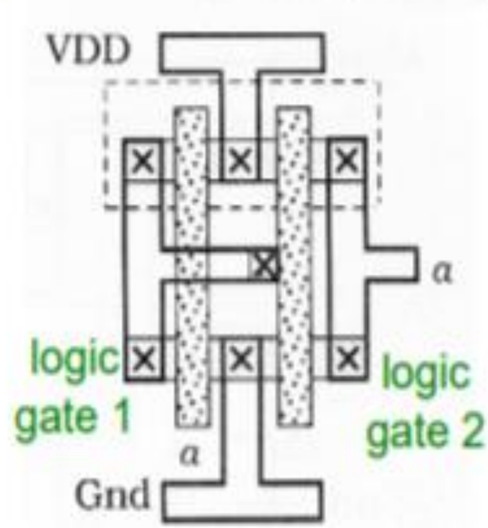
Multiple Gate Layouts

- Sharing power supply rail connections
  - independent gate inputs and outputs
  - shared power supply nodes
  - logic function?



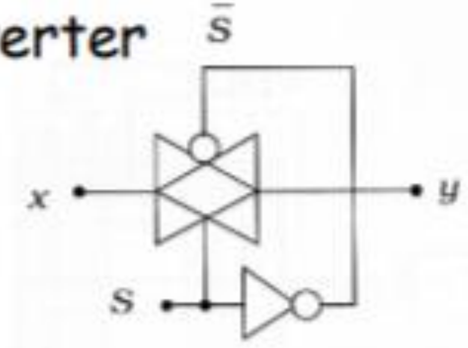
- Cascaded Gates
  - output of gate 1 = input of gate 2
    - g1 output metal connected (via contact) to g2 gate poly
  - shared power supply node
  - function?
    - non-inverting buffer

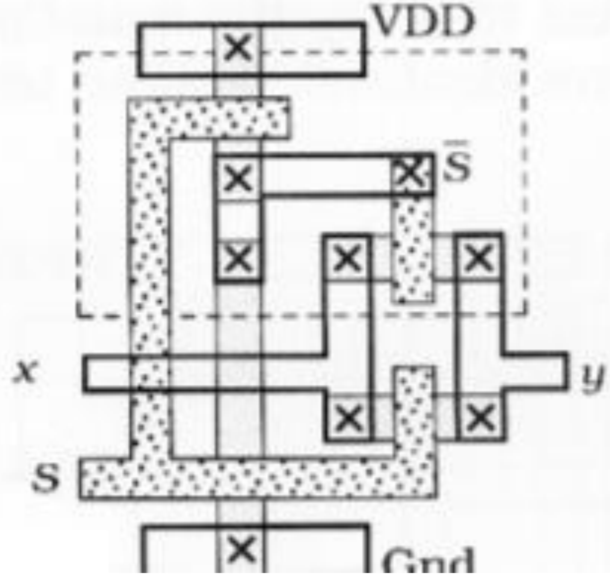




Complex inter-cell routing

- Transmission gate with built-in select inverter
  - one TG gate driven by s at inverter input
  - one TG gate driven by s' at inverter output
  - complicates poly routing inside the cell
    - figures uses n+ to route signal under metal 1
      - not great choice due to higher S/D junction capacitance





- Routing rules
  - poly can cross all layers except
    - poly (can't cross itself)
    - active (n+/p+), this forms a transistor
  - metal can cross all layers except
    - metal (can't cross itself)