ضع السؤال نسخ لصق بالاضافة للصورة مع الجواب الصحيح لكي تستطيع عمل بحث بسرعة

==========

- Threshold voltage in CMOS Defined as : The Threshold voltage, VT for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current, IDS effectively drops to zero.

Threshold voltage in CMOS Defined as : The Threshold voltage, VT for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current, IDS effectively drops to zero.

- (●) True
- ( ) False

==========

- Fringe Capacitance for wire becomes less important as process goes low

Fringe Capacitance for wire becomes less important as process goes low

- ( ) True
- (●) False

==========

- The minimum width and minimum spacing provided by:

The minimum width and minimum spacing provided by:

- (●) A. process file
- ( ) B. Layout Engineer
- ( ) C. only by design owner
- ( ) D. Logic designer

==========

==========

- What are the operation regions for a MOS transistor?

What are the operation regions foe a MOS transistor?

- [x] A. Cutoff region
- [x] B. Linear region
- [ ] C. None
- [x] D. Saturation Region
- [ ] E. MOS device has only one region only

==========

- Choose the option below that is regarded as a step in the process of preparing various Silicon wafers process

Choose the option below that is regarded as a step in the process of preparing various Silicon wafers process

- [x] A. Etching and Wafer cleaning.
- [ ] B. Verilog code preparation
- [x] C. Crystal growth & doping
- [x] D. Wafer polishing

==========

Some of advantages of IC are :

Some of advantages of IC are :

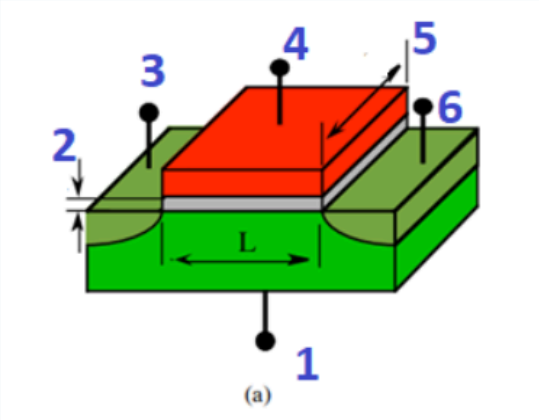
- [ ] A. Design Complexity is large
- [ ] B. Cost is High
- [x] C. Size is less
- [x] D. Less Power Dissipation
- [x] E. High Speed

==========

==========

- Please correctly associate the number with the corresponding transistor part .

Please correctly associate the number with the corresponding transistor part .



Gate 4

Width 5

Drain 6

Tox 2

Source 3

==========

- ---------- connects between 2 segments of metal layers

Question 1

Complete

Mark 1.00 out of 1.00

Flag question

---------- connects between 2 segments of metal layers

A. contact

B. via

C. poly

D. diffusion

The correct answer is: via

==========

==========

- For constraints, the clock period has to be _____ than the data path delay

Question 7
Complete
Mark 1.00 out of 1.00
Flag question

For constraints, the clock period has to be _____ than the data path delay

A. same
B. NA
C. shorter
D. longer

The correct answer is: longer

==========

- We always have to _____ our fast paths down so they arrive along with our slowest path

Question 6
Complete
Mark 1.00 out of 1.00
Flag question

We always have to _____ our fast paths down so they arrive along with our slowest path

A. NA
B. fasten
C. slow
D. keep the same

The correct answer is: slow

==========

- Indicate whether each of the following has been increasing (↑) or decreasing (↓) with process scaling for synchronous integrated circuits.
- Dynamic power consumption as a proportion of total power consumption:

Question 3
Complete
Mark 0.75 out of 1.00
Remove flag

Indicate whether each of the following has been increasing (↑) or decreasing (↓) with process scaling for synchronous integrated circuits.

Dynamic power consumption as a proportion of total power consumption: ↑
Power consumption per device per switching event: ↓
(a) Clock frequency: ↑
tox: ↓

The correct answer is: Dynamic power consumption as a proportion of total power consumption: → ↓, Power consumption per device per switching event: → ↓, (a) Clock frequency: → ↑, tox: → ↓

==========

==========

- Which of these is considered a process for IC fabrication?

Which of these is considered a process for IC fabrication?

- [x] A. Isolation technique
- [x] B. Assembly processing & Packaging
- [x] C. Silicon wafer Preparation
- [x] D. Photolithography
- [x] E. Ion Implantation
- [ ] F. Simulations
- [x] G. Epitaxial Growth
- [x] H. Metallization

==========

- Temperature does not affect RC of the wire ?

Temperature does not affect RC of the wire ?

- ○ True
- ◉ False

==========

- If we could make all paths have equal delays, we wouldn't need sequential logic

Question **4**
Complete
Mark 0.00 out of 1.00
Flag question

If we could make all paths have equal delays, we wouldn't need sequential logic

- ○ True
- ◉ False

The correct answer is 'True'.

==========

==========

- Determine Elmore delay between nose s and d.

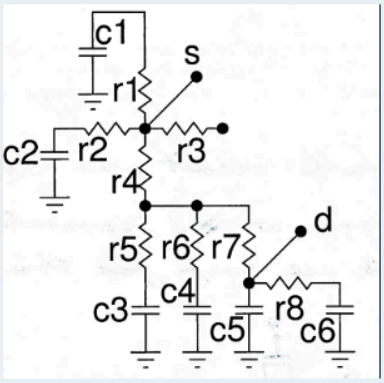
Question **2**

Complete

Mark 1.00 out of 1.00

Flag question

Determine Elmore delay between nose **s** and **d.**



d

A. T = (C3+C4+C5+C6)R4+(C5+C6)(R4+R7)

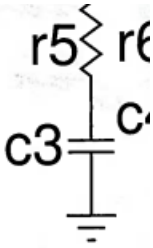
B. T = (C3+C4)R7+(C5+C6)(R7)

C. T = (C3+C4+C5+C6)(R4+R7)

D. T = (C3+C4)R4+(C5+C6)(R4+R7)

$T = C_3(r_4) + C_4(r_4) +$
$C_5(r_4 + r_7) +$
$C_6(r_4 + r_7)$

$T = (C_3 + C_4)r_4 + (C_5 + C_6)(r_4 + r_7)$



==========

- ---------- The data path is so short that it passes through several registers during the same clock cycle.

Question **5**

Complete

Mark 1.00 out of 1.00

Flag question

---------- The data path is so short that it passes through several registers during the same clock cycle.

A. buffer delay

B. NA

C. Max Delay

D. Min Delay

The correct answer is: Min Delay

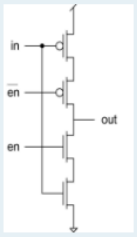
==========

==========

- what function this circuit represent

Question 4
Complete
Mark 1.00 out of 1.00
Flag question

what function this circuit represent



A. tri-state buffer
B. NA
C. pass gate
D. latch
E. flip-flop

==========

- _____ occur due to the logic changing before thold has passed. This is not a function of cycle time – it is relative to a single clock edge

Question 5
Complete
Mark 1.00 out of 1.00
Flag question

_____ occur due to the logic changing before thold has passed. This is not a function of cycle time – it is relative to a single clock edge

A. Hold problems
B. NA
C. Setup problems

The correct answer is: Hold problems

==========

- ---------- The data path is so short that it passes through several registers during the same clock cycle.

Question 7
Complete
Mark 1.00 out of 1.00
Flag question

---------- The data path is so short that it passes through several registers during the same clock cycle.

A. Max Delay
B. Min Delay
C. buffer delay
D. NA

The correct answer is: Min Delay

==========

==========

- We are given a synchronous network with:

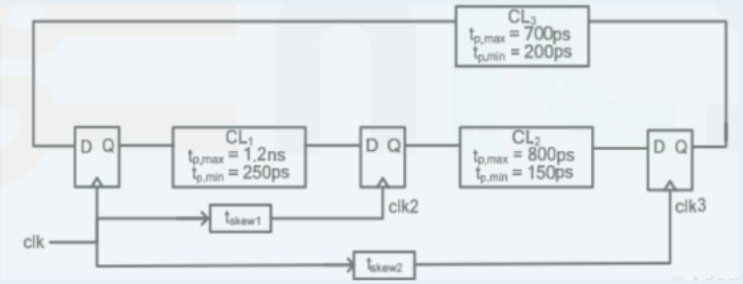
Complete

Mark 5.00 out of 5.00

Flag question

$t_{CQ} = 150ps, t_{setup} = 50ps, t_{hold} = 100ps, t_{jitter} = 0$

$t_{skew1} = -100ps, \quad t_{skew2} = 50ps$

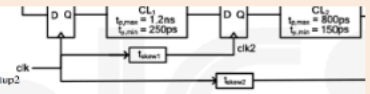


How many paths are there ?

What is the Max frequency can run at

- [x] A. 3 paths
- [x] B. 666MHZ
- [ ] C. 1.05GHz
- [ ] D. 1.17GHz

- **We'll find the setup constraints for each path:**



Path 1: $T_1 + t_{skew1} > t_{cq1} + t_{p,max}(CL_1) + t_{setup2}$

$T_1 > 150p + 1.2n + 50p + 100p = 1500p = 1.5ns \rightarrow 666MHz$

Path 2: $T_2 + (t_{skew2} - t_{skew1}) > t_{cq2} + t_{p,max}(CL_2) + t_{setup3}$

$T_2 > 150p + 800p + 50p - 150p = 850p \rightarrow 1.17GHz$

Path 3: $T_3 + (0 - t_{skew2}) > t_{cq3} + t_{p,max}(CL_3) + t_{setup1}$

$T_3 > 150p + 700p + 50p + 50p = 950p \rightarrow 1.05GHz$

- ***So the critical path is Path 1 and the maximum frequency is 666MHz.***

==========

- Determine the Elmore delay from Node a to Node b in the following circuit

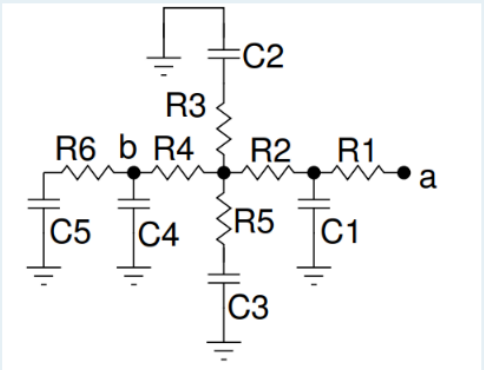
Question 2

Complete

Mark 0.00 out of 1.00

Flag question

Determine the Elmore delay from Node a to Node b in the following circuit



- [ ] A. delay = R1(C1 +C2 +C3) +R2(C2 +C3 +C4) +R4(C4 +C5)
- [ ] B. delay = (R1 +R2+R3+R4)(C4 +C5)
- [ ] C. delay = R1(C1 +C2 +C3 +C4 +C5) +R2(C2 +C3 +C4 +C5) +R4(C4 +C5)
- [ ] D. delay = R1(C1 +C2 +C3 +C4) +R2(C2 +C3 +C4) +R4(C4 +C5)

The correct answer is: delay = R1(C1 +C2 +C3 +C4 +C5) +R2(C2 +C3 +C4 +C5) +R4(C4 +C5)

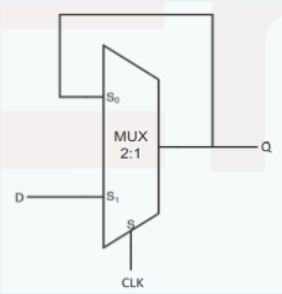
==========

==========

- the below figure represents

Question 6
Complete
Mark 0.00 out of 1.00
Flag question

the below figure represents



A. static latch
B. dynamic mux
C. dynamic flip flop
D. dynamic latch

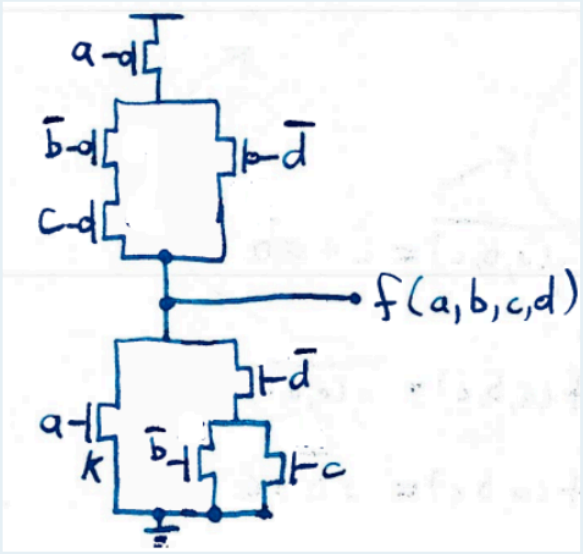
The correct answer is: static latch

==========

- What is the function f(a,b,c,d) ?

Question 1
Complete
Mark 1.00 out of 1.00
Flag question

What is the function f(a,b,c,d) ?



A. F=a'(b'c'+d)
B. F=a'bc'+d
C. F=a(bc'+d)
D. F=a'(bc+d')
E. F=a'(bc'+d)

==========

==========

- Threshold voltage increases for narrow NMOSFETs.

Question **2**
Complete
Mark 1.00 out of 1.00
Flag question

Threshold voltage increases for narrow NMOSFETs.

- (•) True
- ( ) False

The correct answer is 'True'.

==========

- Threshold voltage decreases for very short NMOSFETs

Question **3**
Complete
Mark 1.00 out of 1.00
Flag question

Threshold voltage decreases for very short NMOSFETs

- (•) True
- ( ) False

The correct answer is 'True'.

==========

- List the following interconnect fabrication steps in chronological order:

Question **4**
Complete
Mark 0.20 out of 1.00
Flag question

List the following interconnect fabrication steps in chronological order:

• Etch metal. • Expose photoresist using mask. • Remove all photoresist. • Deposit photoresist. • Deposit metal everywhere.

1) Deposit photoresist.
2) • Expose photoresist using mask.
4) Etch metal
3) Remove all photoresist.
5) Deposit metal everywhere

The correct answer is: 1) → Deposit metal everywhere, 2) → Deposit photoresist., 4) → Etch metal, 3) → • Expose photoresist using mask., 5) → Remove all photoresist.

==========

==========

- Consider the following transfer curve
- What are its NMH and NML?
- What is VM

Question **5**

Complete

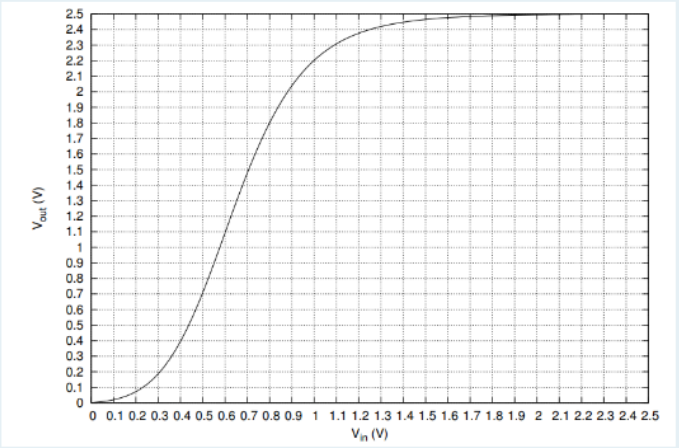
Mark 1.00 out of 1.00

Remove flag

Consider the following transfer curve

What are its NMH and NML?

What is VM



NMH ≈ 1.5 V

NML ≈ 0.25 V

VM ≈ 0.77 V

==========

- Report /Estimate NML and NMH for this technology. Consider the transfer function shown in the following figure.

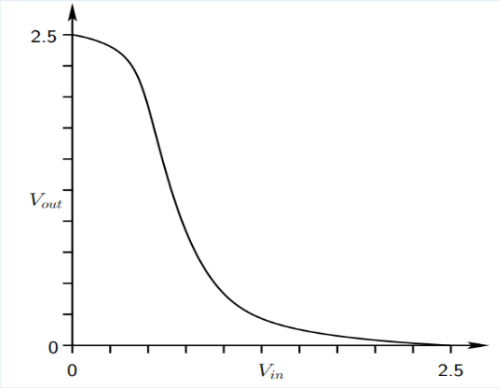
Question **6**

Complete

Mark 1.00 out of 1.00

Flag question

Report /Estimate NML and NMH for this technology. Consider the transfer function shown in the following figure.



- A. NMH = 1.375 V
- B. NML = 0.375 V
- C. NMH = 0.375 V
- D. NMH = 0.375 V

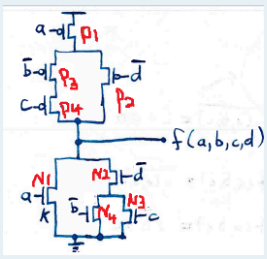
==========

==========

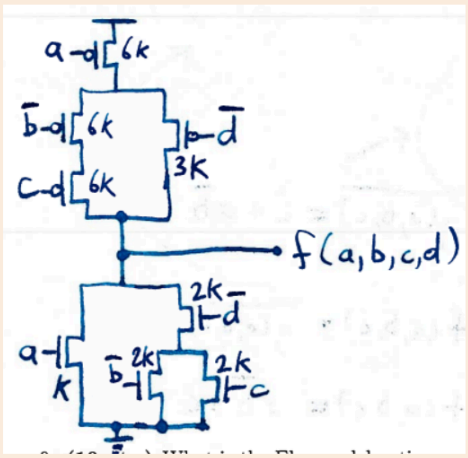
- Match each transistor size based on an invertor of 1k for NMOS and 2k for PMOS

Question 7
Complete
Mark 0.20 out of 1.00
Flag question

Match each transistor size based on an invertor of 1k for NMOS and 2k for PMOS



N2= 6k
P5= 1k
N4= 27k
N5= 2k
N3= 18k
P3= 3k
P2= 2k
P4= 2k
P1= 2k
N1= 1k



The correct answer is: N2= → 2k, P5= → 6k, N4= → 2k, N5= → 2k, N3= → 2k, P3= → 6k, P2= → 3k, P4= → 6k, P1= → 6k, N1= → 1k

==========

==========

- Consider the NMOS inverter given.
- VDD = 5 V, R D = 22 Hohm
- Vtn =:1.5 V, KN = 100 uA/V2
- Detrmine VOL(min) when Vi =Vdd
- Examle for answer to be written VOL(min)=9.4v

Question **8**

Complete

Mark 0.00 out of 1.00

Flag question

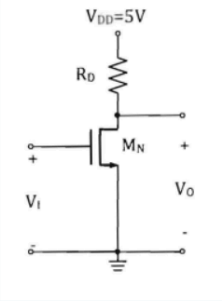
Consider the NMOS inverter given.

VDD = 5 V, R D = 22 Hohm

Vtn =:1.5 V, KN = 100 uA/V2

Detrmine VOL(min) when Vi =Vdd

Examle for answer to be written **VOL(min)=9.4v**



Answer: VOL(min)= 1.5v

$V_I = V_{DD} = 5V \Rightarrow V_o = V_{OL(min)}$

Approximate method :

NMOS is NONSAT and

$V_{OL(min)} << V_I - V_{T_n}$

$R_n = \frac{1}{2K_n(V_{DD}-V_{GS})} = \frac{1}{2(0.1\,mA/V^2)(3.5V)} = \frac{1}{0.7\,mA/V} = 1.43K$

$V_{OL(min)} = \frac{R_N}{R_D+R_N} V_{DD} = \frac{1.43}{22+1.43} \cdot 5V$

$V_{OL(min)} = 0.3V << V_I - V_{T_n} = 3.5V$

The correct answer is: VOL(min)=3.5v

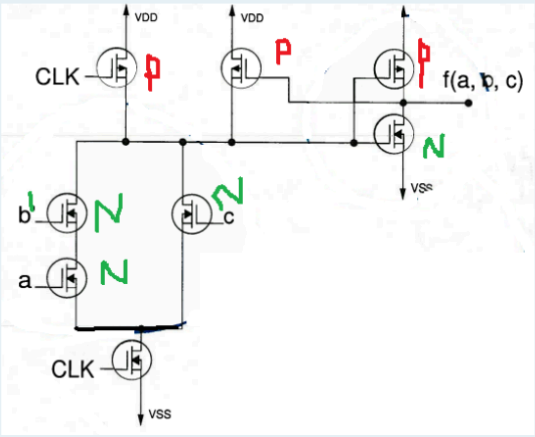
==========

==========

- What is the output F(a,b,c,d) for a given circuit shown below

Question 9
Complete
Mark 1.00 out of 1.00
Flag question

What is the output F(a,b,c,d) for a given circuit shown below



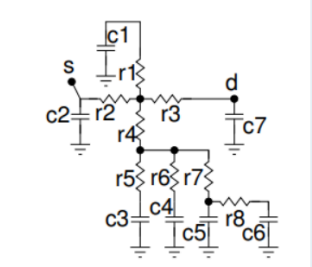
- A. ab'+c
- B. ab+c
- C. a+b'.c
- D. ab'c

==========

- Derive an expression for the time constant when driving node d. Vs changes from 0 V to 2.5 V at time zero. (delay from s to d)

Question 10
Complete
Mark 1.00 out of 1.00
Flag question

Derive an expression for the time constant when driving node **d**. **Vs** changes from 0 V to 2.5 V at time zero. (delay from s to d)



- A. τd = r2 (c1 + c3) + (r2 + r3+ c4 + c5 + c6) c7.
- B. τd = r2 (c2 + r3+ c4 + c5 + c6) c7.
- C. τd = r2 (c1 + c3 + c4 + c5 + c6) + (r2 + r3) c7.
- D. τd = r2 (c1 + c3 + c4) + (r2 + r3+ c5 + c6) c7.

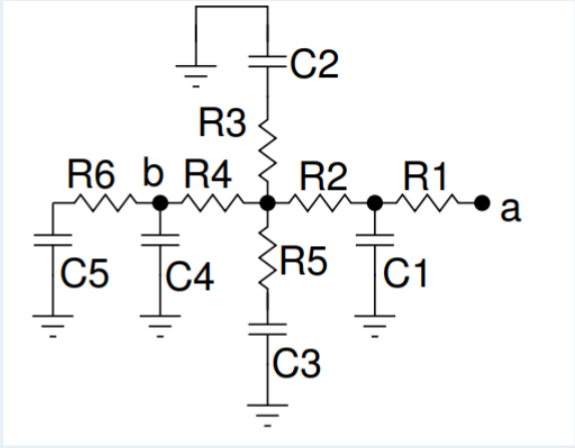
==========

==========

- Determine the Elmore delay from Node a to Node b in the following circuit
-

Question 11
Complete
Mark 0.00 out of 1.00
Flag question

Determine the Elmore delay from Node a to Node b in the following circuit



A. delay = (R1 +R2+R3+R4)(C4 +C5)
B. delay = R1(C1 +C2 +C3 +C4) +R2(C2 +C3 +C4) +R4(C4 +C5)
C. delay = R1(C1 +C2 +C3) +R2(C2 +C3 +C4) +R4(C4 +C5)
D. delay = R1(C1 +C2 +C3 +C4 +C5) +R2(C2 +C3 +C4 +C5) +R4(C4 +C5)

The correct answer is: delay = R1(C1 +C2 +C3 +C4 +C5) +R2(C2 +C3 +C4 +C5) +R4(C4 +C5)

==========

- The PMOSFETs and NMOSFETs in an inverter have been sized to achieve balanced rise and fall times by making the NMOS larger than the PMOS .

Question 3
Complete
Mark 0.00 out of 1.00
Remove flag

The PMOSFETs and NMOSFETs in an inverter have been sized to achieve balanced rise and fall times by making the NMOS larger than the PMOS .

True
False

The correct answer is 'False'.

==========

==========

- List the following interconnect fabrication steps in chronological order:
- • Etch metal. • Expose photoresist using mask. • Remove all photoresist. • Deposit photoresist. • Deposit metal everywhere

Question **4**

Complete

Mark 1.00 out of 1.00

Flag question

List the following interconnect fabrication steps in chronological order:

• Etch metal. • Expose photoresist using mask. • Remove all photoresist. • Deposit photoresist. • Deposit metal everywhere.

3) • Expose photoresist using mask.
5) Remove all photoresist.
2) Deposit photoresist.
4) Etch metal
1) Deposit metal everywhere

The correct answer is: 3) → • Expose photoresist using mask., 5) → Remove all photoresist., 2) → Deposit photoresist., 4) → Etch metal, 1) → Deposit metal everywhere

==========

- Consider the following transfer curve
- What are its NMH and NML?
- What is VM

Question **6**

Complete

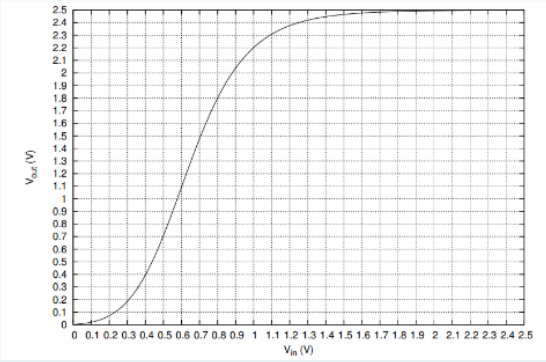
Mark 1.00 out of 1.00

Flag question

Consider the following transfer curve

What are its NMH and NML?

What is VM



NMH ≈ 1.5 V
VM ≈ 0.77 V
NML ≈ 0.25 V

The correct answer is: NMH ≈ → 1.5 V, VM ≈ → 0.77 V, NML ≈ → 0.25 V

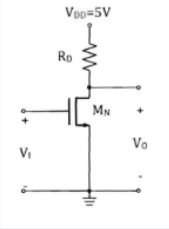
==========

==========

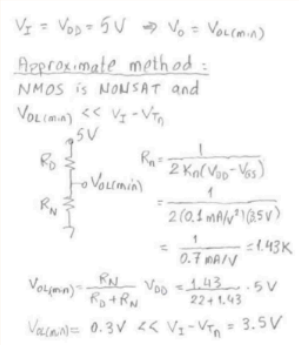
- Consider the NMOS inverter given.
- VDD = 5 V, R D = 22 Hohm
- Vtn =:1.5 V, KN = 100 uA/V2 Detrmine VOL(min) when Vi =VddExamle for answer to be written VOL(min)=9.4v

Question 8
Complete
Mark 0.00 out of 1.00
Flag question

Consider the NMOS inverter given.
VDD = 5 V, R D = 22 Hohm
Vtn =:1.5 V, KN = 100 uA/V2
Detrmine VOL(min) when Vi =Vdd
Examle for answer to be written **VOL(min)=9.4v**



Answer: VOL(min) = 1.5v



The correct answer is: VOL(min)=3.5v

==========

- holes generally travel more slowly than electrons in IC semiconductors.

Question 3
Complete
Mark 1.00 out of 1.00
Flag question

holes generally travel more slowly than electrons in IC semiconductors.

- (•) True
- ( ) False

Use up to two sentences to explain why holes generally travel more slowly than electrons in IC semiconductors. Took multiple answers, e.g., "higher particle mass for holes than electrons" or "more likely interaction with holes and semiconductor lattice results in higher probability of change in particle direction"

The correct answer is 'True'.

==========

==========

- In the following circuit, the capacitance of CL is 50 fF.
- CL is initially charged to 2.5 V. At time zero, its gate is attached ground, as shown in the figure. VT P = -0.5 V.
- 1) If we replace the PMOSFET with a 2 kΩ resistor, how long does it take for the capacitor to discharge to 1.25 V? *Your answer should be be like this (1)120ps)*
- 2) If we consider the transistor cut-off, what is the final voltage of the capacitor?
- *Your answer should be like this (2) 200v)*

Question **6**
Complete
Mark 0.00 out of 1.00
Remove flag

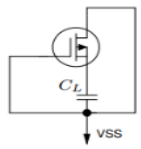
In the following circuit, the capacitance of CL is 50 fF.

CL is initially charged to 2.5 V. At time zero, its gate is attached ground, as shown in the figure. VT P = -0.5 V.

1) If we replace the PMOSFET with a 2 kΩ resistor, how long does it take for the capacitor to discharge to 1.25 V? *Your answer should be be like this (1)120ps)*

2) If we consider the transistor cut-off, what is the final voltage of the capacitor?

Your answer should be like this (2) 200v)



PMOSFET with grounded gate.

- [x] A. 1) 9ps
- [ ] B. 2)0.5v
- [ ] C. 1) 0.69ps
- [ ] D. 1) 69ps
- [x] E. 2)2.25v
- [ ] F. 2)2.5v
- [ ] G. 2)2.0v

$$
\begin{aligned}
2.5\,\mathrm{V}/2 &= 2.5\,\mathrm{V}\cdot e^{\frac{-t}{50\,\mathrm{fF}\cdot 2\,\mathrm{k\Omega}}} \\
1/2 &= e^{\frac{-t}{100\,\mathrm{ps}}} \\
\log 1/2 &= \frac{-t}{100\,\mathrm{ps}} \\
0.69 &= \frac{t}{100\,\mathrm{ps}} \\
t &= 69\,\mathrm{ps}
\end{aligned}
$$

==========

- Temperature does not affect RC of the wire ?

Temperature does not affect RC of the wire ?

- [ ] True
- [x] False

The correct answer is 'False'.

==========

==========

- ---------- The data doesn't have enough time to pass from one register to the next before the next clock edge.

---------- The data doesn't have enough time to pass from one register to the next before the next clock edge.

A. NA
B. Min Delay
C. Max Delay
D. Buffer delay

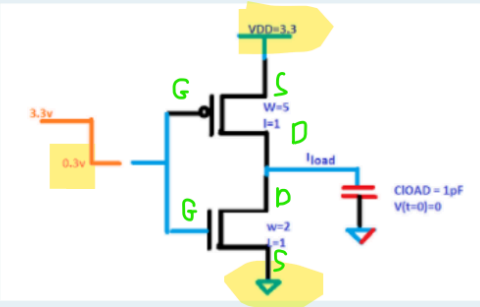
The correct answer is: Max Delay

==========

- A step input is applied at time t=O to the loaded inverter with dimensions and initial conditions as shown below.

A step input is applied at time t=O to the loaded inverter with dimensions and initial conditions as shown below.

For all transistors: $L_{min} = 1\ \mu m$, $W_{min} = 1\ \mu m$, $V_{T,p} = -1\ V$, $\mu_p C_{ox} = (1/6) \times 10^{-3}\ A/V^2$, $\lambda_p = 0.0V^{-1}$, $V_{T,n} = 1\ V$, $\mu_n C_{ox} = (1/2) \times 10^{-3}\ A/V^2$, $\lambda_n = 0.0V^{-1}$.



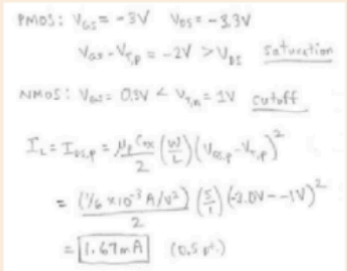
What region the PMOS will be in? (Linear, Cutoff, Saturation) — Saturation ✔

What region the NMOS will be in ? — Cutoff ✔

What is the current Iload immediately after the step is applied in mA? — 1.67 ✔

Note: do not add a unit, just the number

Your answer is correct.



The correct answer is:
What region the PMOS will be in? (Linear, Cutoff, Saturation) → Saturation,
What region the NMOS will be in ? → Cutoff,
What is the current Iload immediately after the step is applied in mA?
Note: do not add a unit, just the number → 1.67

==========

==========

- Some of advantages of IC are :

Question 4

Complete

Marked out of 1.00

Some of advantages of IC are :

- A. Cost is High
- B. Design Complexity is large
- C. High Speed
- D. Less Power Dissipation
- E. Size is less

==========

- Match to the correct answer
- Performance
- Area
- Body (substrate) normally connected

Match to the correct answer

Performance	Directly affects cost ✗
Area	Directly affects cost ✓
Body (substrate) normally connected to ---------- for NMOS	Power-Delay Product ✗
The interface between designer and process (CMOS fabrication) engineer	Design Rules ✓
used in chip manufacturing	Silicon ✓
Raising source voltage increases ---------- of transistor	Threshold Voltage ✓

Your answer is partially correct.

You have correctly selected 4.

The correct answer is:

Performance → Power-Delay Product,

Area → Directly affects cost,

Body (substrate) normally connected to ---------- for NMOS → Threshold Voltage,

The interface between designer and process (CMOS fabrication) engineer → Design Rules,

used in chip manufacturing → Silicon,

Raising source voltage increases ---------- of transistor → Threshold Voltage

==========

==========

- Which is faster Holes or Electrons?

Question 8
Correct
Mark 1.00 out of 1.00
Flag question

Which is faster Holes or Electrons?

Answer: Electrons ✔

==========

- Increasing fan-out, NCREASE OR DECREASES the propagation delay
-

Question 9
Correct
Mark 1.00 out of 1.00
Flag question

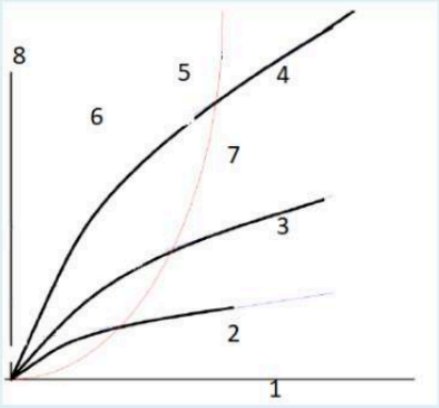
Increasing fan-out, INCREASE OR DECREASES the propagation delay

Answer: INCREASE ✔

==========

- For the simulation Image shown below match the number to the right answer

For the simulation Image shown below match the number to the right answer

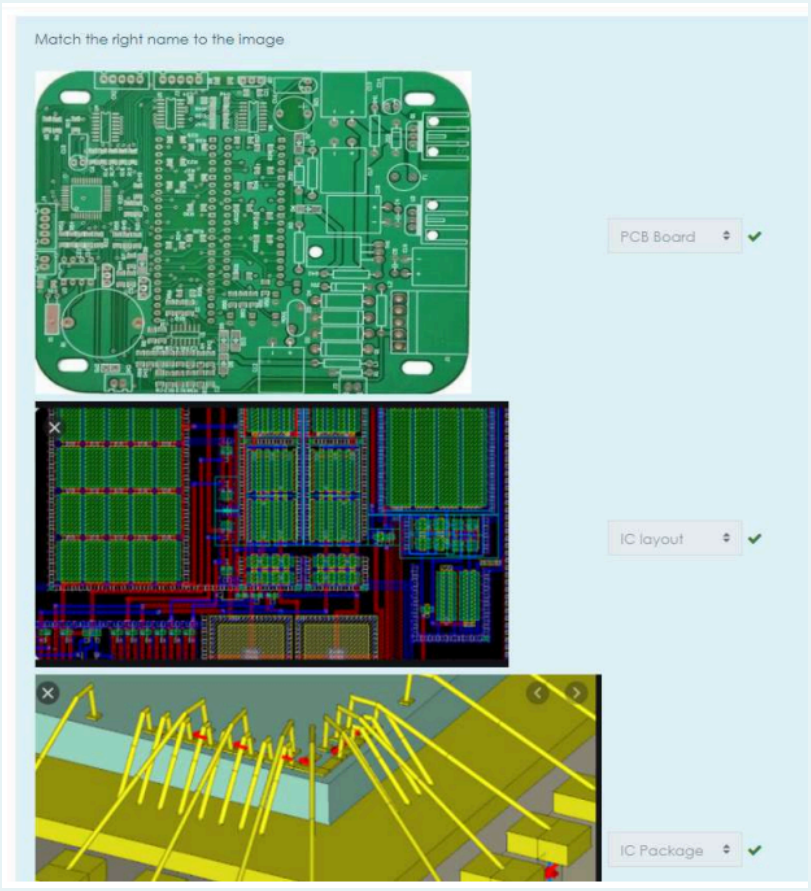


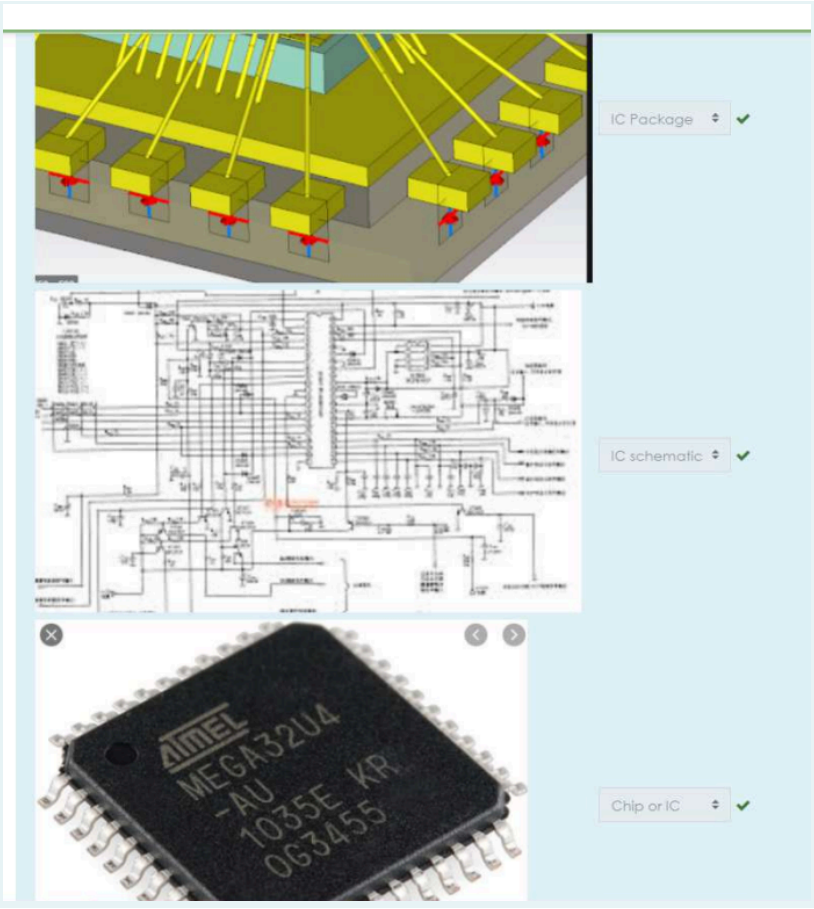
1	VDS	✔
5	VGS-VT	✔
7	Saturation	✔
6	Non Saturation	✔
3	VGS2	✔
2	VGS1	✔
8	Id	✔
4	VGS3	✔

==========

==========

- Match the right name to the image

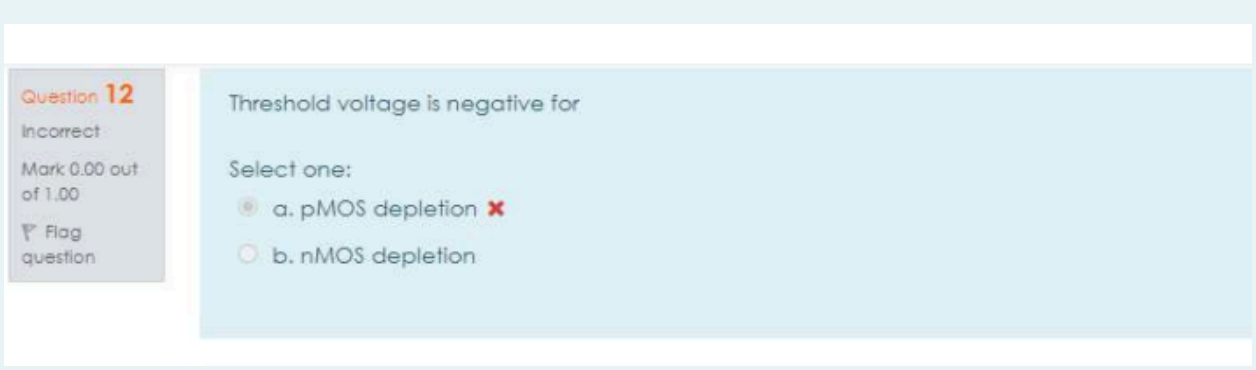




==========

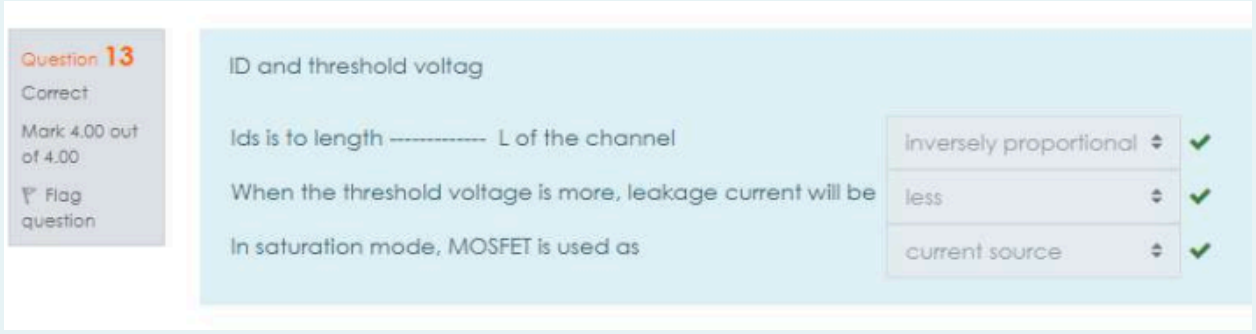
==========

- Threshold voltage is negative for



==========

- ID and threshold voltag



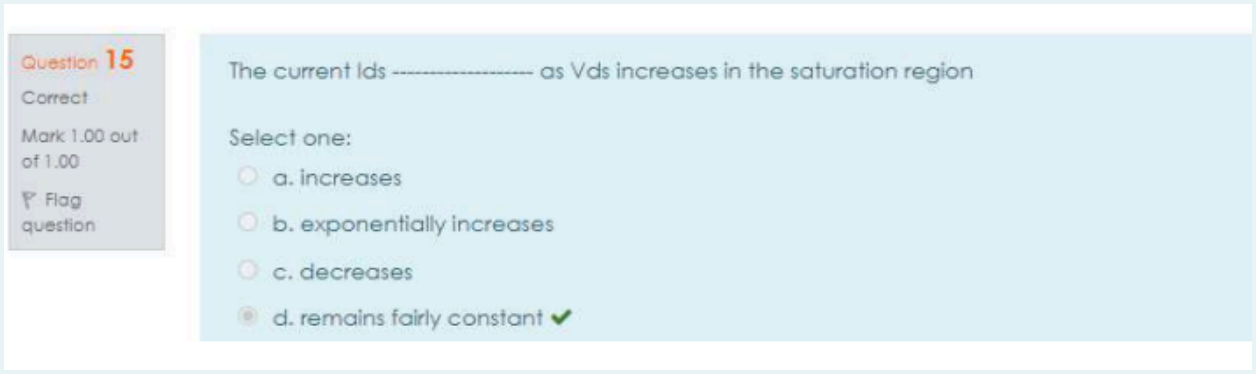
==========

- There are _____ of operations for MOSFET

==========

==========

- The current Ids _____ as Vds increases in the saturation region



==========

- CMOS technology is used in developing

==========

- Ids versus Vds Relationships

==========

==========

- In CMOS fabrication,the photoresist layer is exposed to _____

In CMOS fabrication,the photoresist layer is exposed to ---

Select one:

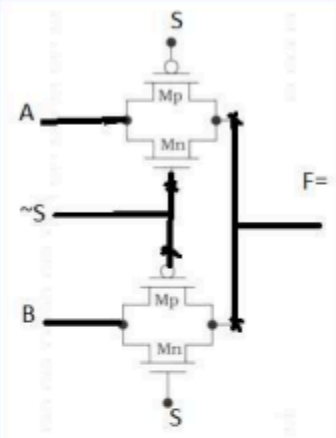
- a. visible light
- b. ultraviolet light ✔
- c. infra red light
- d. no light at all

==========

- What does output F equal base on the circuit below?

Question 1
Complete
Mark 1.50 out of 1.50
Flag question

What does output **F** equal base on the circuit below?



- a. (S.A)+ (~S.B)
- b. (~S.A)+ (~S.B)
- c. (~S.A)+ (S.B)
- d. (~S.A)+ (S.~B)
- e. (S.A)+ (S.B)

The correct answer is:
(~S.A)+ (S.B)

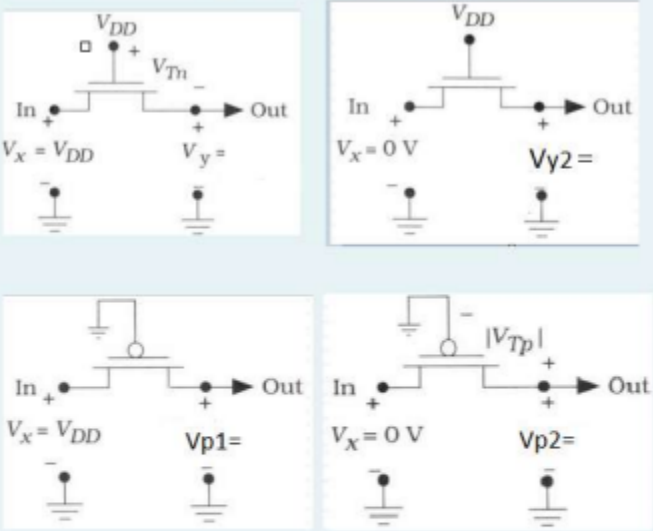
==========

==========

- Based on the devices shown below, answer the following questions

Question 2
Complete
Mark 4.00 out of 4.00
Flag question

Based on the devices shown below, answer the following questions :



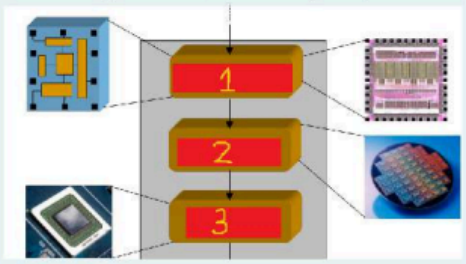
Vy2= 0
Vp2= | Vtp |
Vp1= VDD
Vy= VDD-Vtn

==========

- Glven the Image below to represent IC design flow , match the number to the right step name

Question 3
Complete
Mark 2.00 out of 2.00
Flag question

Glven the Image below to represent IC design flow , match the number to the right step name



Fabrication 2
In step 1, what does the left picture reprecent top level cell view
Packaging 3
Physical Design 1

The correct answer is:
Fabrication → 2,
In step 1, what does the left picture reprecent → top level cell view,
Packaging → 3,
Physical Design → 1

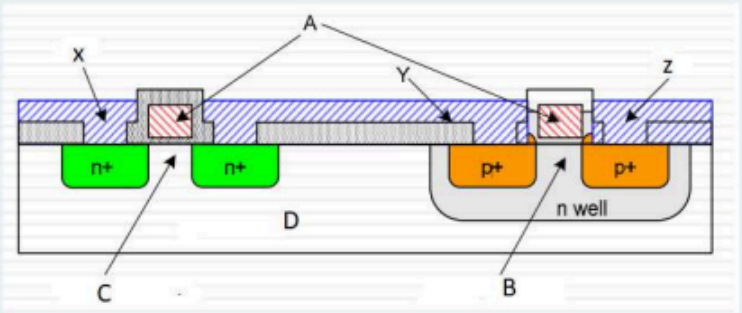
==========

==========

- Based on the cross-section shown below, map each letter to the right name

Question 4
Complete
Mark 4.50 out of 4.50
Flag question

Based on the cross-section shown below, map each letter to the right name



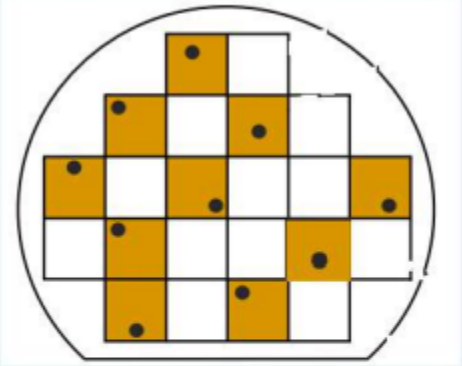
D	substrate
C	NMOS-device
Z	VDD
X	GND
A	Poly
Y	output
the cross-section represent	Invertor
B	PMOS-Device

==========

- Givin the image below, answer the following questions

Question 5
Complete
Mark 3.00 out of 3.00
Flag question

Givin the Image below, answer the following questions



How many dies are there?	22
what is the defect % ? your answer should be In this form 13/40	12/22
How many wafer we have in the picture	1

==========

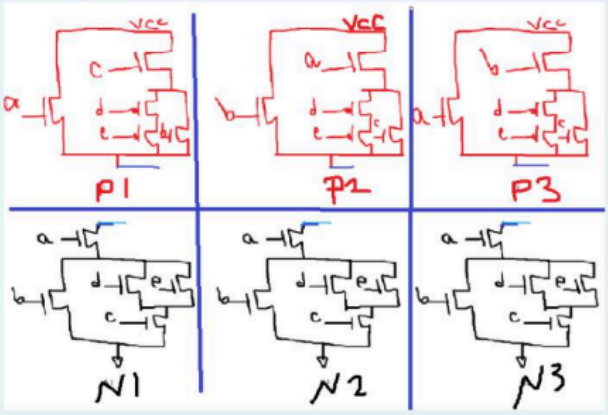
==========

- Based on the structure shown below which N tree you connect to which P tree to form this function

Question 6
Complete
Mark 3.00 out of 3.00
Flag question

Based on the structure shown below which N tree you connect to which P tree to form this function

$f = \overline{a.(b+c.(d+e))}$



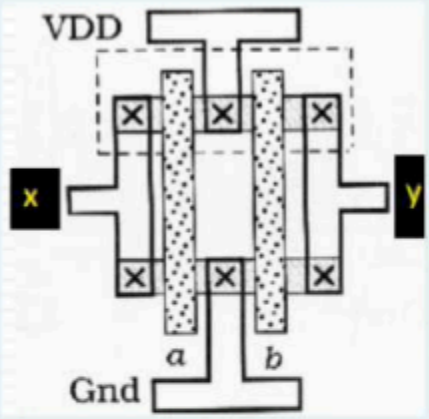
a. P2 with N3
b. P2 with N1
c. P1 with N1
d. P1 with N2
e. P3 with N3
f. P1 with N3
g. P3 with N2

==========

- Givin physical design below what will be the value for X and Y ?

Question 7
Complete
Mark 0.00 out of 2.00
Flag question

Givin physical design below what will be the value for X and Y ?



X= ~(A OR B)
Y= ~(A OR B)

The correct answer is:
X= → ~A,
Y= → ~B

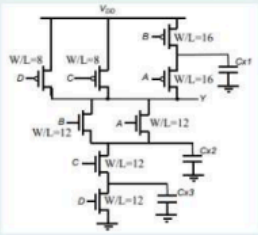
==========

==========

- Given the design shown below, answer the following questions

Question 8
Complete
Mark 0.00 out of 5.00
Flag question

Given the design shown below, answer the following questions



are the devices sized correctly giving that the output resistance is the same as that of an inverter with an NMOS W/L = 4 and PMOS W/L = 8. — no

What is the logic function implemented by the CMOS transistor network? — Y = ~((AB). C+D)

What are the VALUES OF THE INTERNAL NODES caps that give the best-case tpHL — tpHL happens when the internal node capacitances (Cx2 and Cx3) are charged before the high to low transition

which has a bigger cap Cx1or Cx2, ignore material type factor — cx1

The correct answer is:
are the devices sized correctly giving that the output resistance is the same as that of an inverter with an NMOS W/L = 4 and PMOS W/L = 8. → yes,

What is the logic function implemented by the CMOS transistor network? → Y = (~A+~B).(~C+~D),

What are the VALUES OF THE INTERNAL NODES caps that give the best-case tpHL → tpHL happens when the internal node capacitances (Cx2 and Cx3) are discharged before the high to low transition,

which has a bigger cap Cx1or Cx2, ignore material type factor → cx2

==========

- **Fabrication Steps**

Question 9
Complete
Mark 2.00 out of 2.00
Flag question

Fabrication Steps

Spin on photoresist	Photoresist
Expose photoresist through n-well mask	Lithography
Grow SiO2 on top of Si wafer	Oxidation
Polysilicon	Deposit very thin layer of gate oxide

The correct answer is:
Spin on photoresist → Photoresist,

Expose photoresist through n-well mask → Lithography,

Grow SiO2 on top of Si wafer → Oxidation,

Polysilicon → Deposit very thin layer of gate oxide

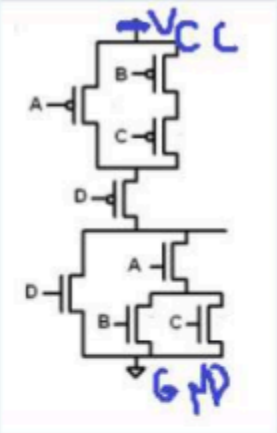
==========

==========

- Given that Rp/Rn=3 size the following circult TO HAVE EQUAL Tr and Tf accordingly

Question 10
Complete
Mark 1.50 out of 3.00
Flag question

Given that Rp/Rn=3 size the following circult TO HAVE EQUAL Tr and Tf accordingly



D-Pdevice	6
B-Pdevice	12
B-Ndevice	6
A-Pdevice	6
A-Ndevice	6
D-Ndevice	3

The correct answer is:
D-Pdevice → 18,
B-Pdevice → 36,
B-Ndevice → 6,
A-Pdevice → 18,
A-Ndevice → 6,
D-Ndevice → 3

==========

- When the channel pinches off?

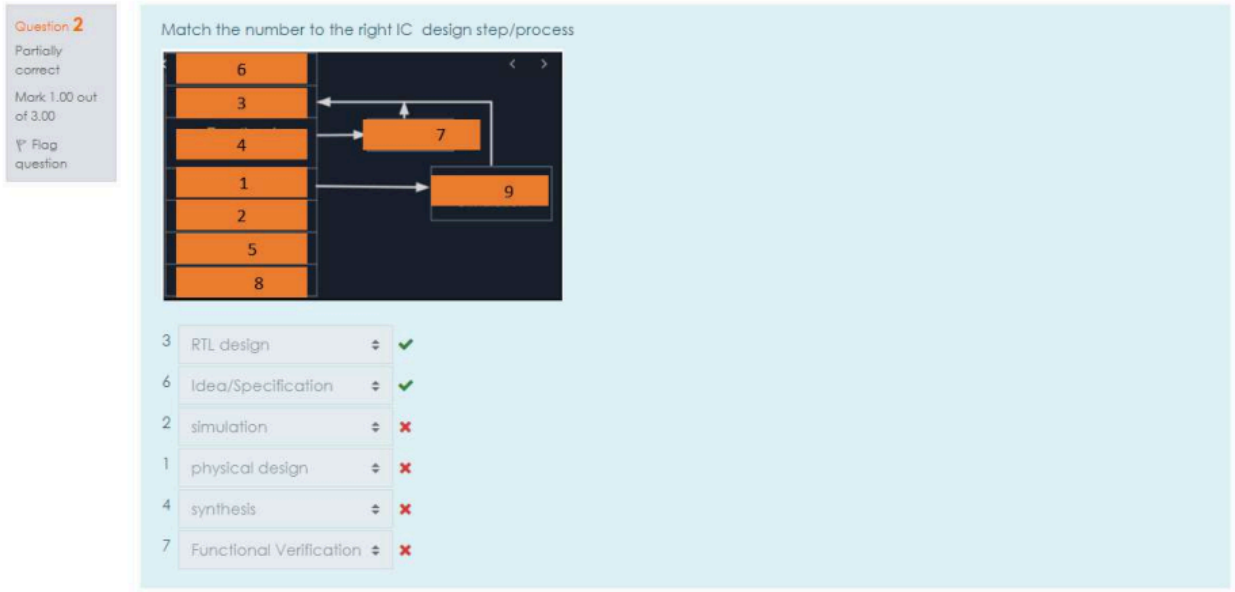
When the channel pinches off?

Select one:
- a. Vgs>Vds
- b. Vds>Vgs
- c. Vds>(Vgs-Vth) ✔
- d. Vgs>(Vds-Vth)

==========

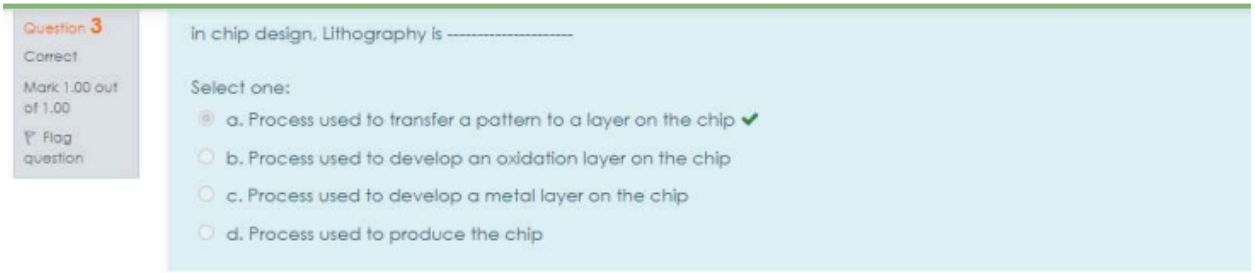
==========

- Match the number to the right IC design step/process



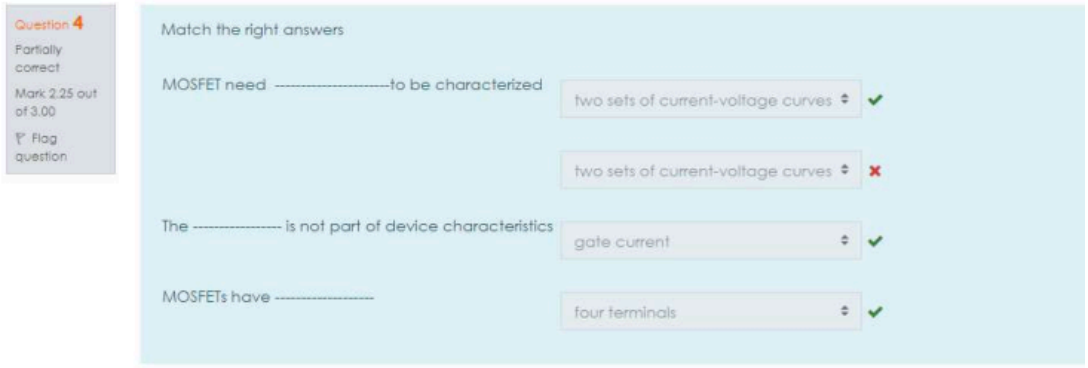
==========

- in chip design. Lithography is



==========

- Match the right answers
  - MOSFET need _____ to be characterized
  - The _____ is not part of device characteristics
  - MOSFETs have _____



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- NMOS devices

Question 5
Correct
Mark 5.00 out of 5.00
Flag question

NMOS devices

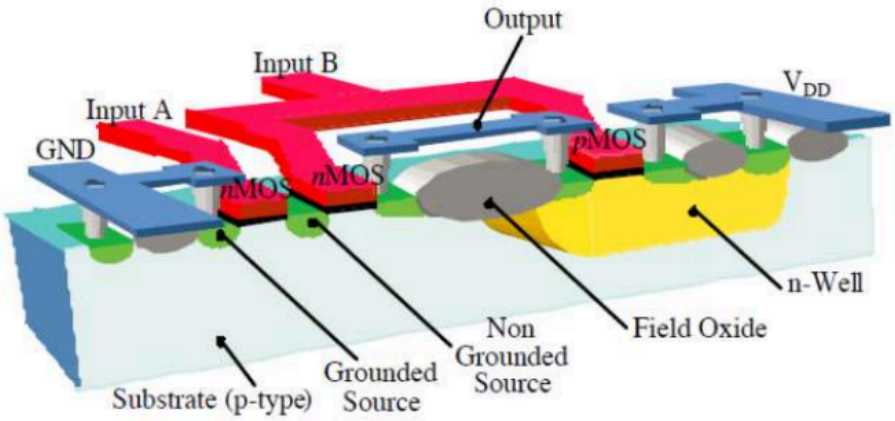
In n channel MOSFET, ---------- is constant	channel length ✔
Source and drain in nMOS device are isolated by	diodes ✔
NMOS devices are formed in	p-type substrate of moderate doping level ✔
Interconnection pattern is made on	metal layer ✔
In nMOS device, gate material could be	polysilicon ✔

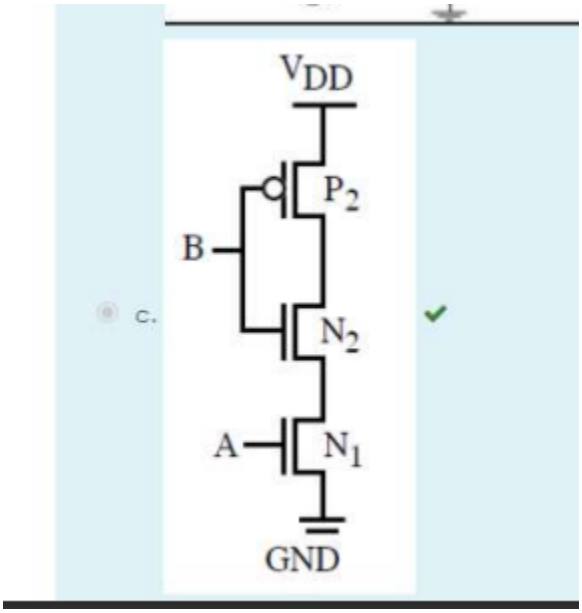
==========

- Select the right schematic for the cross-section given below

Question 7
Correct
Mark 3.00 out of 3.00
Flag question

Select the right schematic for the cross-section given below





c. ✔

==========

==========

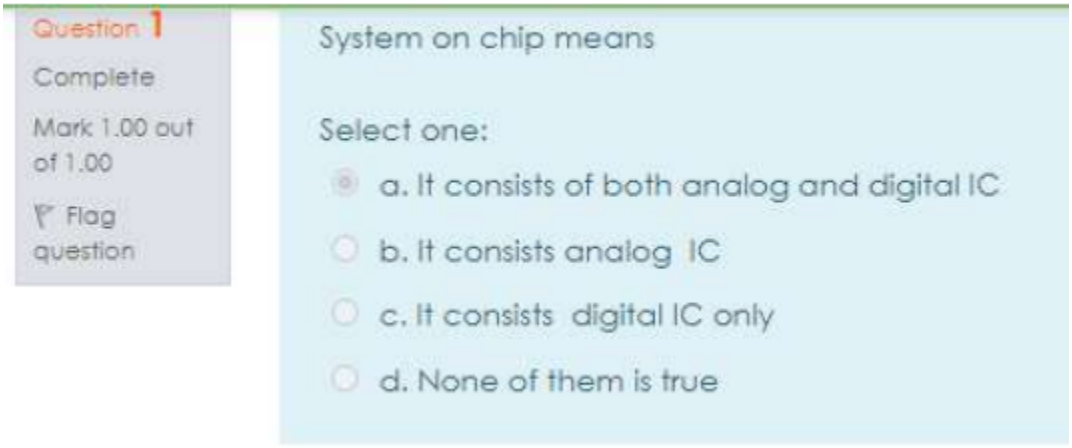
- In CMOS fabrication, nMOS and pMOS are integrated in the same substrate

==========

- Goal of library cell Characterization:

==========

- System on chip means



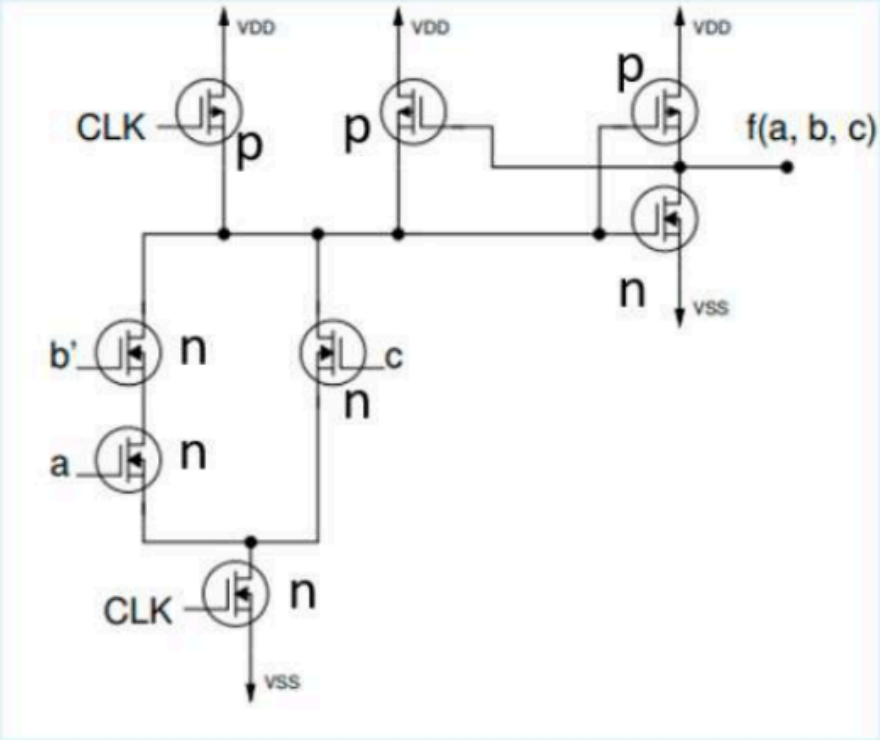
==========

==========

- What function f(a, b, c) does the following circuit implement?

Question 2
Complete
Mark 2.00 out of 2.00
Flag question

What function f(a, b, c) does the following circuit implement?



Select one:

- a. c+ab
- b. (c+ab')'
- c. (a+b;)c)
- d. ab'+c

==========

- Optical masking is used in IC design for

Question 3
Complete
Mark 1.00 out of 1.00
Flag question

Optical masking is used in IC design for

Select one:

- a. Protection of layer
- b. Pattern transfer
- c. Cleaning unwanted materials
- d. none of them

==========

==========

- n-type semiconductors are

Question 4
Complete
Mark 0.00 out of 1.00
Flag question

n-type semiconductors are

Select one:
- a. None of them
- b. Negatively charged
- c. Positively charged
- d. Neutral charged

==========

- The packaging is used in IC for

Question 5
Complete
Mark 1.00 out of 1.00
Flag question

The packaging is used in IC for

Select one:
- a. safety and protection
- b. power delivery to each circuit
- c. none of them
- d. wire local blocks

==========

- Indicate whether each of the following has been increasing or decreasing with process scaling for synchronous integrated circuits.

Question 6
Complete
Mark 2.00 out of 2.00
Flag question

Indicate whether each of the following has been increasing (↑) or decreasing (↓) with process scaling for synchronous integrated circuits.

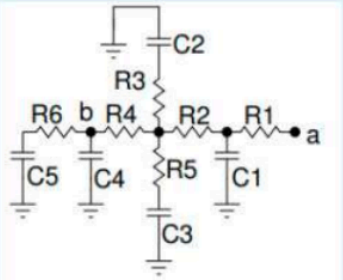
tox	decreasing
Power consumption per device per switching event	decreasing
Clock frequency	increasing
Dynamic power consumption as a proportion of total power consumption	decreasing

==========

- Determine the Elmore delay from Node a to Node b in the following circuit.

Question 7
Complete
Mark 2.00 out of 2.00
Flag question

Determine the Elmore delay from Node a to Node b in the following circuit.



Select one:
- a. $\tau_{ab} = R1(C1 + C2 + C3 + C4 + C5) + R2(C2 + C3 + C4 + C5) + R4(C4)$
- b. $\tau_{ab} = R1(C1 + C2 + C3 + C4 + C5) + R2(C2 + C3 + C4 + C5) + R4(C4 + C5)$
- c. $\tau_{ab} = R1(C1 + C2 + C3 + C4) + R2(C2 + C3 + C4 + C5) + R4(C4 + C5)$
- d. $\tau_{ab} = R1(C1 + C2 + C3 + C5) + R2(C2 + C3 + C5) + R4(C4 + C5)$

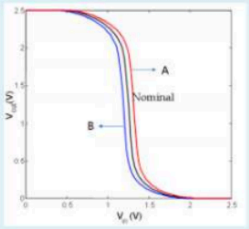
==========

==========

- The PMOSFETs and NMOSFETs in an inverter have been sized to achieve balanced rise and fall times. However, process variation has caused the implementation to deviate from the design. The A line in Figure below is associated with an inverter that has

Question 8
Complete
Mark 2.00 out of 2.00
Flag question

The PMOSFETs and NMOSFETs in an inverter have been sized to achieve balanced rise and fall times. However, process variation has caused the implementation to deviate from the design. The A line in Figure below is associated with an inverter that has



Select one:

- a. Lower-than-planned resistance PMOSFET and higher-than-planned resistance NMOSFET.
- b. Higher-than-planned resistance PMOSFET and lower-than-planned resistance NMOSFET.
- c. no change of resistance for PMOSFET and resistance of NMOSFET.

==========

- The mobiity s given by:

Question 9
Complete
Mark 1.00 out of 1.00
Flag question

The mobiity is given by :

Select one:

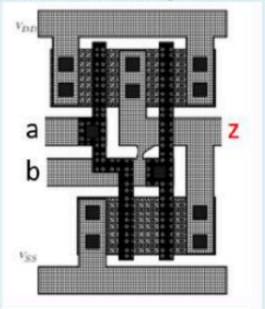
- a. $\mu = E_o V_o$
- b. $\mu = V_o / E_o$
- c. $\mu = E_o / V_o$

==========

- A dust particle did something horible to a mask, causing the implemented layout to differ from the desgned layout. Consider the corrupted layout shown in Figure below

Question 10
Complete
Mark 3.00 out of 3.00
Flag question

A dust particle did something horible to a mask, causing the implemented layout to differ from the designed layout. Consider the corrupted layout shown in Figure below



Is there any input vector (a, b) for which the output and power consumption will be as the designer originally intended? If so, indicate the input vector	a'b
What type of gate was the designer most likely trying to implement?	NAND2
IF you draw a schematic for the gate actually implemented,then	input b shorted to output z

==========

==========

- Stick diagrams are those which convey layer information through?

Question 11
Complete
Mark 1.00 out of 1.00
Flag question

Stick diagrams are those which convey layer information through?

Select one:

- a. thickness
- b. color
- c. shape
- d. design rules

==========

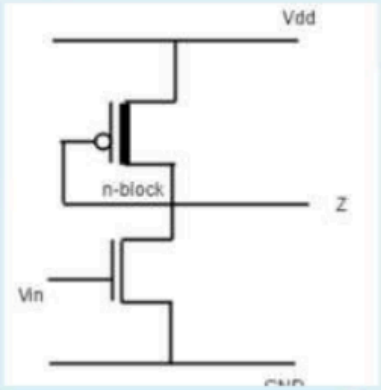
- CMOS domino logic can be expressed diagrammafically as

Question 12
Complete
Mark 1.00 out of 1.00
Flag question

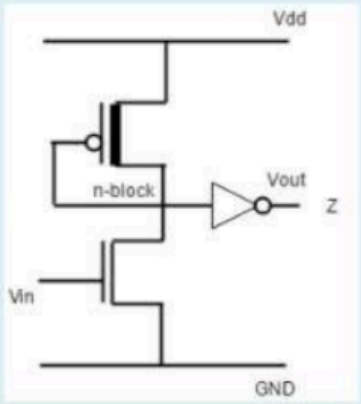
CMOS domino logic can be expressed diagrammatically as

Select one:

a.



b.



==========

==========

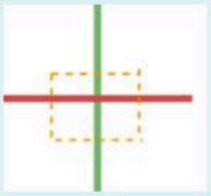
- How is nMOS depletion-mode transistor represented? given that diffusion is green, poly is red and well is dotted yellow line

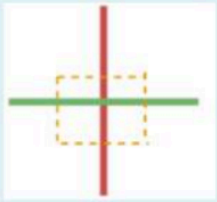
Question 13
Complete
Mark 0.00 out of 1.00
Flag question

How is nMOS depletion-mode transistor represented? given that diffusion is green, poly is red and well is dotted yellow line

Select one:

a. 

b. 

c. 

==========

- Which contributes to the wiring capacitance?

Question 14
Complete
Mark 1.00 out of 1.00
Flag question

Which contributes to the wiring capacitance?

Select one:

- a. interlayer capacitance
- b. fringing fields
- c. all of the mentioned
- d. peripheral capacitance

==========

- Which has a high voltage drop?

Question 16
Complete
Mark 1.00 out of 1.00
Flag question

Which has a high voltage drop?

Select one:

- a. metal 6 layer
- b. metal layer
- c. polysilicon layer
- d. diffusion layer

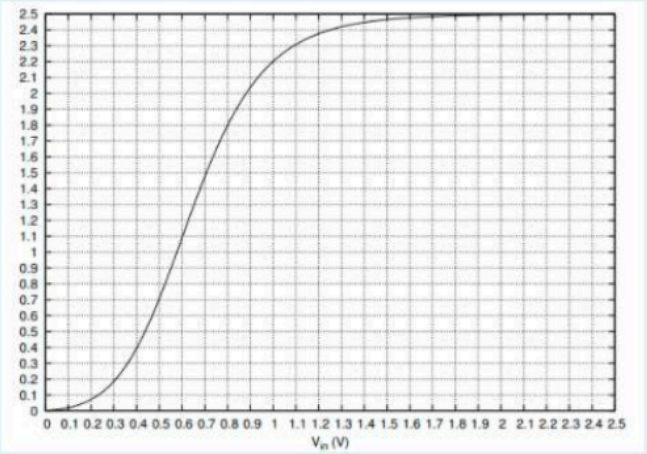
==========

==========

- Consider the following transfer curve

Question 15
Complete
Mark 2.00 out of 3.00
Flag question

Consider the following transfer curve



What type of device is this? Buffer
What are its NML? ~0.45v
What are its NMH ? ~1.5v

==========

- Match to the correct answer
  - Threshold voltage is negative for
  - Two metal layers can be joined by using
  - When polysilicon crosses a diffusion
  - will be formed

Question 17
Complete
Mark 3.00 out of 3.00
Flag question

Match to the correct answer

Threshold voltage is negative for _____ pmos
Two metal layers can be joined by using via
When polysilicon crosses a diffusion _____ will be formed transistor

==========

- The overall delay is __ to the relative resistance r.

Question 19
Complete
Mark 1.00 out of 1.00
Flag question

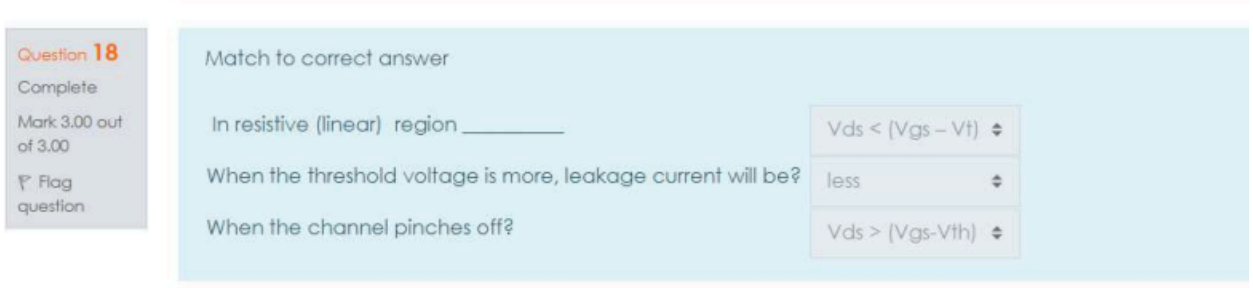
The overall delay is _____ to the relative resistance r.

Select one:
- a. exponentially proportional
- b. inversely proportional
- c. directly proportional

==========

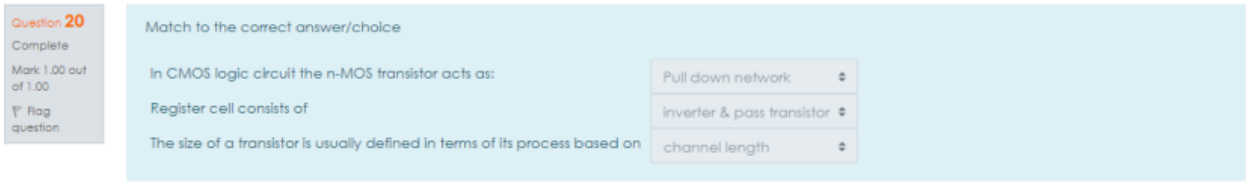
==========

- Match to correct answer
  - In resistive (linear) region
  - When the threshold voltage is more, leakage current will be?
  - When the channel pinches off?



==========

- Match to the correct answer/choice
  - In CMOS logic circuit the n-MOS transistor acts as:
  - Register cell consists of
  - The size of a transistor is usually defined in terms of its process based on



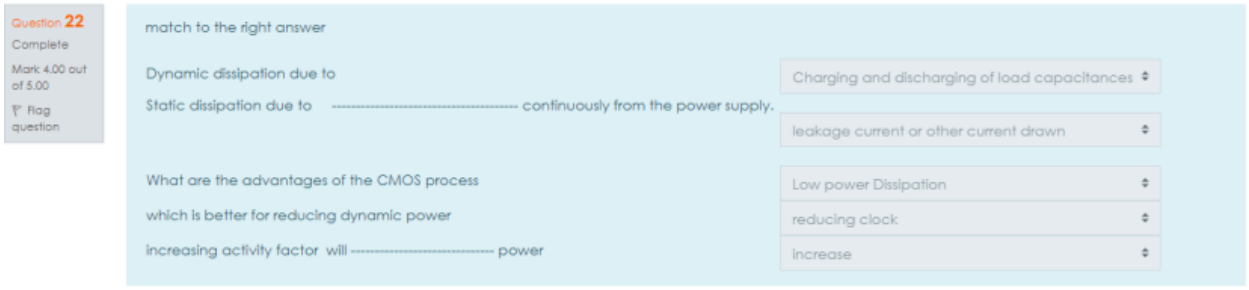
==========

- match/selec the right answer
  - Time, before the latch closes, that the data must arrive to guarantee the data is captured correctly after the latch closes
  - The transistor current changes with the operating temperature, as T increases mobiity
  - ff is the fime taken for a waveform to fall from 90% to 10% of its steady-state value.

==========

==========

- match to the right answer
    - Dynamic dissipation due to
    - Static dissipation due to _____ continuously from the power supply.
    - What are the advantages of the CMOS process
    - which is better for reducing dynamic power
    - increasing activity factor will _____ power



==========

- Main Issues In Dynamic Design

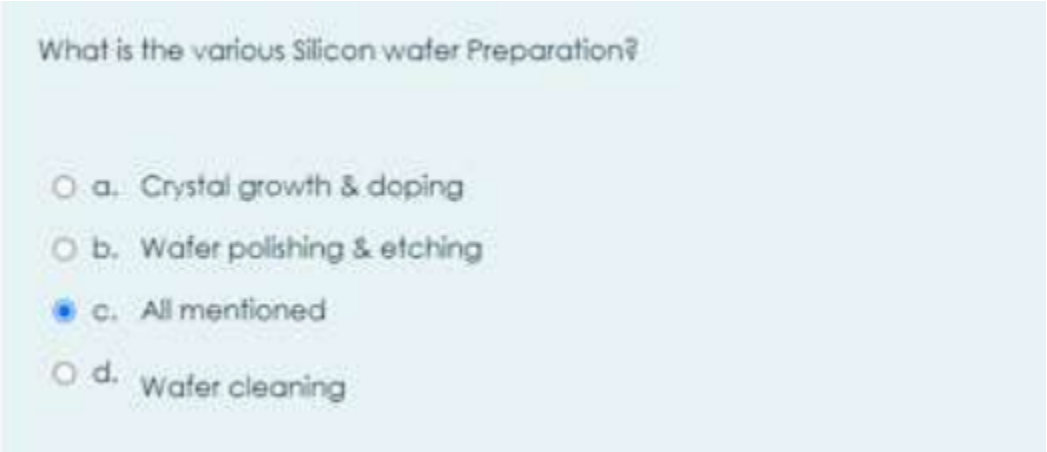
==========

- Usually in IC design, the late signal (slow) will be connected:

==========

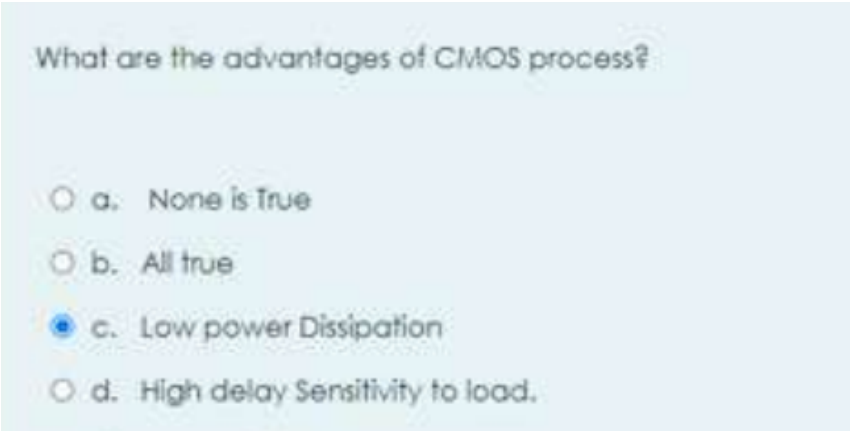
==========

- What is the various Silicon wafer Preparation?



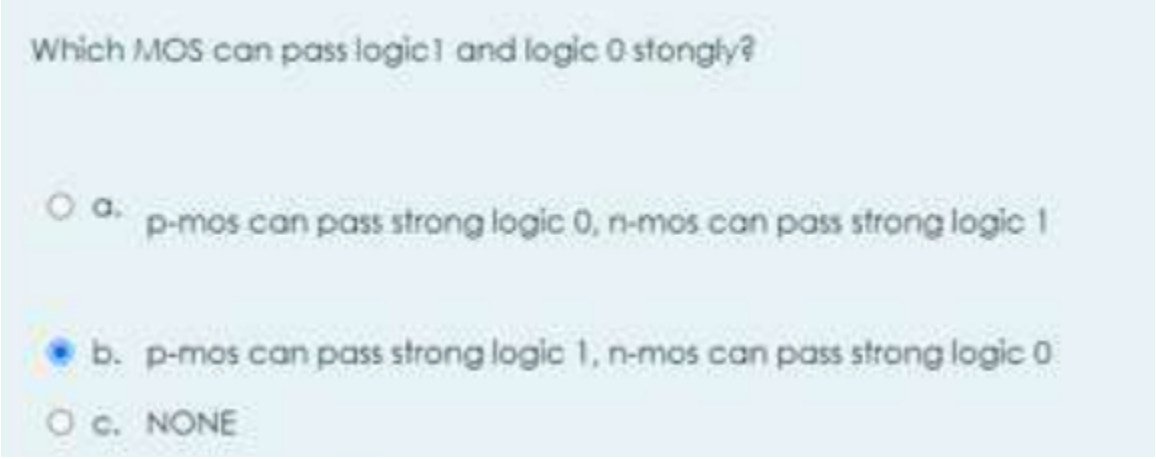
==========

- What are the advantages of CMOS process?



==========

- Which MOS can pass logic1 and logic 0 stongly?



==========

==========

- Ids depends on

==========

- Design rules does not specify

==========

- In basic inverter circuit _____ is connected to ground

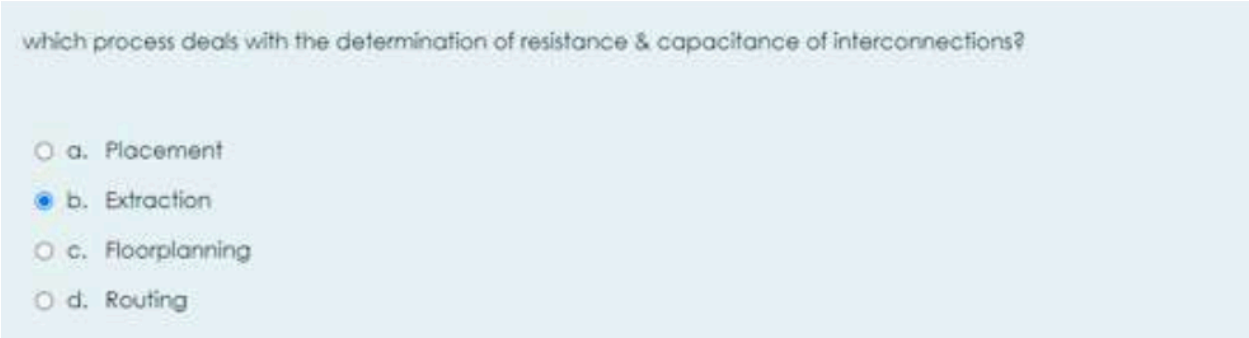
==========

- Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?

==========

==========

- which process deals with the determination of resistance & capacitance of interconnections?



==========

- Which type of digital systems exhibit the necessity for the exlstence of at least one teedback path from output to input?

==========

- The time required for an Input data for settie _____ the friggering edge of clock is known as 'Setup Time".

==========

==========

- Hold fime is defined as the time required for the data to ____ after the triggering edge of clock.

==========

- ICs are generally made of

==========

- Dynomic power:

==========

==========

- For Standard Cell Physical Structure layout

==========

- The design flow of IC design system is : 1. architecture design 2. market requirement 3.Layout 4. HDL coding 5. logic design

The design flow of IC design system is :

1. architecture design 2. market requirement 3.Layout 4. HDL coding 5. logic design

A. 5-1-2-4-3
B. 2-1-5-3-4
C. 2-1-5-4-3
D. 4-1-3-2-5
E. 5-3-2-1-4

==========

- CMOS NANS gate is better than CMOS NOR gates because

CMOS NANS gate is better than CMOS NOR gates because

A. CMOS nor takes more space than NAND
B. CMOS NOR uses P channel transistor in parallel.
C. CMOS NAND uses P channel transistor in parallel.
D. Only A and C is correct.
E. All (A and B and C) are correct

==========

- How many transistors are required to implement a four-input OR using CMOS design style?

How many transistors are required to implement a four-input OR using CMOS design style?

A. 6
B. 8
C. 10
D. 12
E. None

==========

==========

- In order to have "pass" logic gate We need

In order to have "pass" logic gate We need

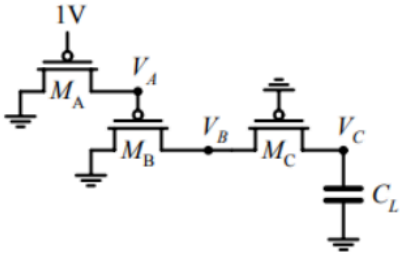
A. An N-channel and P-Channel transistor in series
B. We need only p-channel so it will pass good one.
C. We need only N-channel so it will pass good zero.
D. An N-channel and P-Channel transistor in parallel
E. None

==========

- For the circuit in Fig. below, determine the final value of VA, VB, VC, assuming initial condition at each of the nodes is 3V and VTP = -0.5V (ignore body effect).

For the circuit in Fig. below, determine the final value of VA, VB, VC, assuming initial condition at each of the nodes is 3V and VTP = −0.5V (ignore body effect).

A. VA = 3V VB = 2V VC = 1.5V
B. VA = 1.5V VB = 1.5V VC = 1.5V
C. VA = 2V VB = 2V VC = 2V
D. VA = 1.5V VB = 2V VC = 2V
E. None

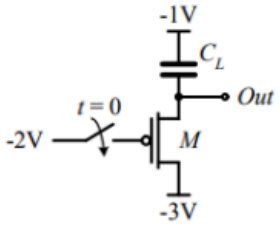


==========

- Assuming that switch as shown in figure below closes at time t = 0, what is the output voltage at t = 0+ and t = oo? CL was initially discharged, VTP = -0.5V.

6. Assuming that switch as shown in figure below closes at time t = 0, what is the output voltage at t = 0+ and t = ∞? CL was initially discharged, VTP = −0.5V.

A. Vout (t = 0+) = +1V Vout (t = ∞) = −1.5V
B. Vout (t = 0+) = −1V Vout (t = ∞) = +1.5V
C. Vout (t = 0+) = −1V Vout (t = ∞) = −1.5V
D. Vout (t = 0+) = +1V Vout (t = ∞) = +1.5V
E. None



==========

==========

- The delay of a static CMOS inverter is minimized if(W/L)p/ (W/L)n=μη /μp.

7. **The delay of a static CMOS inverter is minimized** if (W/L)p / (W/L)n = μn / μp.
   - **A.** True
   - **B.** False
   - **C.** None

==========

- The load capacitance of a static CMOS gate has no effect on its VTC

8. **The load capacitance of a static CMOS gate has no effect on its VTC**
   - **A.** False
   - **B.** True
   - **C.** None

==========

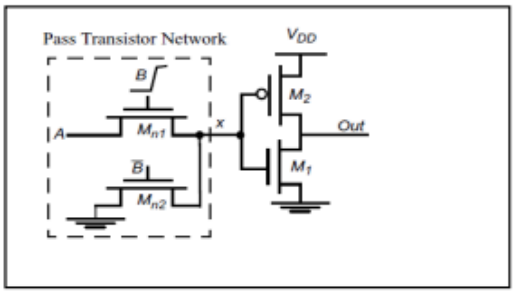
- CMOS Transmission (Pass) Gates , capable of passing both '1' and '0'

10. **CMOS Transmission (Pass) Gates , capable of passing both '1' and '0'**
    - **A. Good "1"**
    - **B. Good "0"**
    - **C. Poor "1"**
    - **D. Poor "0"**
    - **E. Both A and B only**

==========

- What is the logic function performed by this circuit?

11. **What is the logic function performed by this circuit?**
    - **A. The circuit is a NOR gate.**
    - **B. The circuit is a XOR gate.**
    - **C. The circuit is a NAND gate.**
    - **D. The circuit is a NOT gate.**
    - **E. None**



==========

==========

- Increasing power supply voltage, VDD, will

12. Increasing power supply voltage, VDD, will

A. Does not change the speed performance of CMOS gates.
B. Increase the speed performance of CMOS gates.
C. Decrease the speed performance of CMOS gates.
D. None

==========

- The IN and OUT bus lines in IC design should be in

13. The IN and OUT bus lines in IC design should be in

A. Metal
B. Contact
C. Polysilicon
D. Diffusion
E. Silicon
F. None

==========

- If an NMOSFET gate's dielectric were changed from SiO2 to a low-k material with half the permittivity of SiO2, what would happen to its ID? You may assume that VGS ≥ VTN

14. If an NMOSFET gate's dielectric were changed from SiO2 to a low-κ material with half the permittivity of SiO2, what would happen to its ID? You may assume that VGS ≥ VTN

A. Id does not change.
B. ID being halved.
C. ID doubled.
D. Id does not change.
E. None

==========

- Which one is the right order for the following the following interconnect fabrication steps : . Etch metal. · Expose photoresist using mask. · Remove all photoresist. · Deposit photoresist. . Deposit metal everywhere.

15. Which one is the right order for the following the following interconnect fabrication steps :
• Etch metal. • Expose photoresist using mask. • Remove all photoresist.
• Deposit photoresist. • Deposit metal everywhere.

A. 1)Deposit metal everywhere. 2) Expose photoresist using mask. 3). Deposit photoresist 4) Etch metal. 5) Remove all photoresist
B. 1)) Deposit photoresist 2) Deposit metal everywhere 3) Expose photoresist using mask. 4) Etch metal. 5) Remove all photoresist
C. 1)Deposit metal everywhere. 2) Deposit photoresist. 3) Expose photoresist using mask. 4) Etch metal. 5) Remove all photoresist
D. 1)Deposit metal everywhere. 2) Expose photoresist using mask. 3) Deposit photoresist. 4) Etch metal. 5) Remove all photoresist
E. None

==========

==========

- CMOS stands for:

CMOS stands for:

A. complementary material oxide semiconductor
B. complementary metal oxide semiconductor
C. complex metal oxide semiconductor
D. complex material oxide semiconductor

==========

- Chip Yield refers :

Chip Yield refers :

A. Yield drops as chip area increases
B. low yield means high cost
C. Yield depends on process parameters
D. All of the above

==========

- Which of the following metal layer has Maximum resistance?

Which of the following metal layer has Maximum resistance?

A. Metal1
B. Metal2
C. Metal3
D. Metal4

==========

- How do you size NMOS and PMOS transistors to increase the threshold voltage?

How do you size NMOS and PMOS transistors to increase the threshold voltage?

A. Increase voltage on gate
B. Increase voltage on the bias(substrate)
C. Lower drain voltage
D. Lower drain current

==========

==========

- What happens to delay if you increase load capacitance?

What happens to delay if you increase load capacitance?

A. Increase if driver size stay the same
B. Decrease if driver size stay the same
C. Has no effect if we make driver smaller
D. Delay stay the same

==========

- What are the limitations in increasing the voltage (power supply) to reduce delay?

What are the limitations in increasing the voltage (power supply) to reduce delay?

A. Delay limits: Increasing voltage increases delay
B. Power limits: Increasing voltage will result in more power
C. Area limits: increasing voltage will affect chip area significantly
D. A and B

==========

- What happens if we increase the number of contacts or via from one metal layer to the next?

What happens if we increase the number of contacts or via from one metal layer to the next?

A. Power dissipation decreased
B. Increases resistance and power dissipation
C. Overall resistance decrease
D. A and C

==========

- What is the difference between LVS and DRC FOR LAYOUT?

What is the difference between LVS and DRC FOR LAYOUT?

A. The layout must be drawn according to certain strict design rules DRC
B. Both used in layout to verify delay
C. None of the above
D. LVS compares the netlist extracted from the layout with the schematic to ensure that the layout is an identical match to the cell schematic
E. A and D

==========

==========

- What are pros/cons of using low Vt, high Vt cells?

What are pros/cons of using low Vt, high Vt cells?

A. low Vt cell violates design rules DRC
B. high Vt cells affect delay of the cell so we should not use in speed path
C. high Vt cells affect leakage power
D. None of the above
E. B and C

==========

- The main variables/parasitic that affects power dissipations

.The main variables/parasitic that affects power dissipations

A. low Vt cell violates design rules DRC
B. high Vt cells affect delay of the cell so we should not use in speed path
C. high Vt cells affect leakage power
D. None of the above
E. B and C

==========

- In MOS transistors ____ is used for their gate

7. In MOS transistors,____ is used for their gate
a) metal b) silicon-di-oxide c) polysilicon d) gallium
In MOS transistors, polycrystalline silicon is used for their gate region instead of metal. Polysilicon gates have replaced all other older devices.

==========

- In N channel MOSFET which is the more negative of the elements?

10. In N channel MOSFET which is the more negative of the elements?
a) source b) gate c) drain
In N channel MOSFET, source is the more negative of the elements and in the case of P channel MOSFET, it is the more positive of the elements.

==========

- MOS transistors consists of what layers ?

6. MOS transistors consists of what layers ?

Metal layer, oxide layer and a semiconductor layer.

==========

==========

- SIlicon-di-oxide is WHAT TYPE OF MATERIALS?

12. SIlicon-di-oxide is WHAT TYPE OF MATERIALS?

Oxide Material.

==========

- In CMOS fabrication, nMOS and pMOS are integrated in the same substrate. IS THAT TRUE ?

14. In CMOS fabrication, nMOS and pMOS are integrated in the same substrate. IS THAT TRUE ?

In CMOS fabrication, nMOS and pMOS are integrated in the same chip substrate. n-type and p-type devices are formed in the same structure.

==========

- Which type of CMOS circuits are good and better?

16. Which type of CMOS circuits are good and better?

a) p well b) n well c) all of the mentioned d) none of the mentioned

N-well CMOS circuits are better than p-well CMOS circuits because of lower substrate bias effect.

==========

- Which layer has high capacitance value? metal or diffusion?

25. Which layer has high capacitance value? metal or diffusion?

Diffusion or active layer has high capacitance value due to which it has low or moderate IR drop.

==========

- Which layer has high resistance value? polysilicon or metal ?

26. Which layer has high resistance value? polysilicon or metal ?

Polysilicon layer has high resistance value and due to this it has high IR drop.

==========

- Overall delay increases as n_____ where n is the number of pass transistors connected in series. increases or decreases?

30. Overall delay increases as n_____ where n is the number of pass transistors connected in series. increases or decreases?

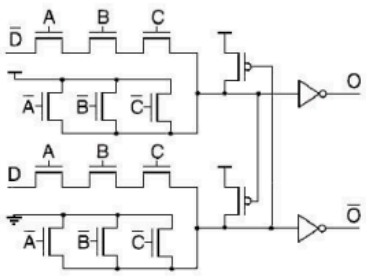
Overall delay increases as n increases where n is the number of pass transistors connected in series. The overall delay is directly proportional to n^2

==========

==========

- What is the logic function of the following gate?

1. **What is the logic function of the following gate?**

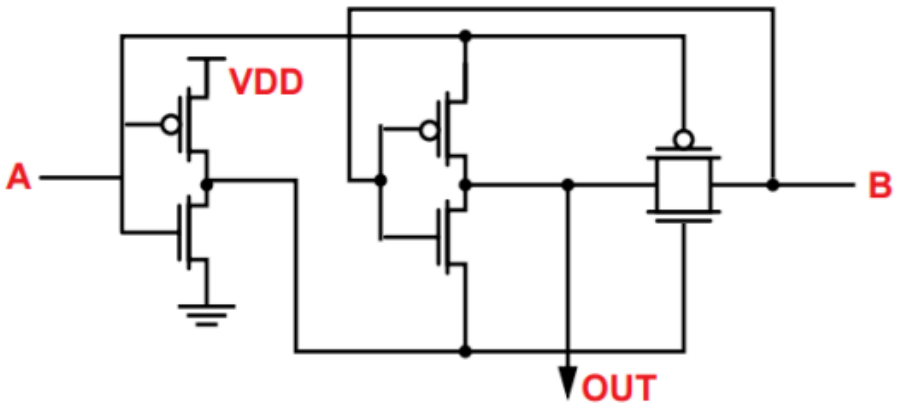


O=ABCD

==========

- What is the output function of the following circuit?

6. What is the output function of the following circuit?



XOR

==========

==========

True or False

- (T) Transmission gates are needed to pass both 0 and 1
- (T) nMOS pass transistors pull no higher than VDD-Vtn
- (T) Process can be defined as – a sequence of steps used to form circuits on a wafer
- (T) Field Oxide used for Isolation between devices
- (T) Transistor's current saturates at high Vds values
- (T) Nwell and Substrate must be connected to the power supply within each cell
- (T) If we now want to create an n-type channel below the Si-SiO2 surface we need to
- increase VGS. As VGS is increased the Si close to the surface first becomes depleted of holes and only then (at higher VGS) electrons start to build the channel.
- (T) We can define the 'threshold voltage' as the VGS that below it the transistor's current (IDS) effectively drops to zero
- (T) Poly or gate materials have a high-resistance conductor (can be used for short routing)
- (T) We have Design Rules because the fabrication process has minimum/maximum feature sizes that can be produced for each layer
- (F) To set the switching threshold (midpoint) voltage, Vm, to VDD/2 in a CMOS inverter, the nMOS transistor must be wider than the pMOS.
- (T) Increasing power supply voltage, VDD, will increase the speed performance of CMOS gates.
- (F) The best way to improve the speed performance of a CMOS circuit is to decrease the channel
- (T) CMOS = Complementary MOS use of both nMOS and pMOS to form a circuit with lowest power consumption.
- (T) Electric Fields: vertical field through gate oxide determines charge induced in channel while horizontal field across channel determines source-to-drain current flow
- (F) pMOS switching behavior device will be on = closed, when Vin > VDD - |Vtp| and will be off = open, when Vin < VDD - |Vtp|
- (T) 'source' is at lowest potential for nMOS and highest potential for pMOS
- (F) Logic gates are created by using sets of controlled switches. nMOS acts like an assert-low switch and pMOS acts like an assert-high switch
- (T) CMOS is inherently Inverting logic,
- (T) CMOS Transmission Gates , capable of passing both '1' and '0'
- (T) Speed power product is measured as the product of switching delay and gate power dissipation is that true?
- (T) Lithography is Process used to transfer a pattern to a layer on the chip , IS THAT TRUE
- (F) CMOS inverter has 2 regions of operation ,is that true?
- (F) Polysilicon is suitable for connecting to VDD or vss grid , is that true ?

- (T) During the floor planning step the overall cell is defined, including: cell size, supply network, etc
- (T) If a designer wants a perfectly balanced rise time and fall time for a CMOS inverter driving a capacitive load, Since the mobility of electrons is normally twice the mobility of holes, we need to make the width of PMOS twice as large as the width of NMOS.
- (T) Does the IC have a good chance of implementing the desired logic functions

==========

- Select the correct statement regarding pipeline concept in sequential circuit

Question **7**

Complete

Mark 1.00 out of 1.00

Select the correct statement regarding pipeline concept in sequential circuit

- A. using a pipeline, we can make our fastest path shorter and therefore increase the delay between actions.
- B. NA
- C. using a pipeline, we can make our slowest path shorter and therefore reduce the delay between actions.
- D. some stages may be faster than others, so we need to hold the input to each stage constant until the previous stage is done. We achieve this by adding a register in between the stages

The correct answers are: some stages may be faster than others, so we need to hold the input to each stage constant until the previous stage is done. We achieve this by adding a register in between the stages, using a pipeline, we can make our slowest path shorter and therefore reduce the delay between actions.

==========

- Large (1)---------- means small (2)---------- , but large (3)----------

Large (1)---------- means small (2)---------- , but large (3)----------
-

- A. (1) W 2(R) 3(C)
- B. (1) C 2(R) 3(W)
- C. (1) R 2(W) 3(C)
- D. (1) C 2(R) 3(W)

The correct answer is: (1) W 2(R) 3(C)

==========

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SOC-51204796

1. Define Threshold voltage in CMOS ? SELECT ALL RIGHT ANSWER

A The Threshold voltage, VT for a MOS transistor can be defined as the voltage applied between the gate and the drain of the MOS transistor below which the gate to source current, IGS effectively drops to zero

B The Threshold voltage, VT for a MOS transistor can be defined as the voltage applied between the gate and the bulk of the MOS transistor below which the drain to source current, IDS effectively reach maximum value

C The Threshold voltage, VT for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current, IDS effectively drops to zero

D All are true

2. a MOS transistor can be considered as ---------- (select all that apply)

A resistive load in leaner region

B current source in saturation region

C short circuit in cutt off

D open circuit all the time

3. If a large ------ is applied this voltage with deplete the Inversion layer .This Voltage effectively pinches off the channel near the source

A VGS

B VDS

C VSB

D VGB

4. There are four main different layers in MOS transistors which are

A Drain , Source, Gate , bulk

B capacitance , resistance, inductance , voltage

C waver , package, diod , voltage

5. The transistor **current changes** with the operating temperature but is not affected by mobility

False

6. As the channel length decreases, the depletion region below the gate can no longer be approximated as a rectangular region. So, as L ----------

A does not change

B increases

C decreases

7. As Vd is higher, the drain depletion region increases, causing a ---------- in Vt.

A decrease

B increase

8. For MOS devices, leakage current occurs in what region

A Linear

B Saturation

C cutt off

9. For the same VDS, as VGS increases, The IDS will ----------

A increase

B decrease

C does not change

D has no effect

10. Hot-e degradation will occure when : When,

A a MOS transistor is in Linear region, , the electric field across the pinch-off region may be high enough that carriers gain there enough energy to excite electron-hole pairs.

B a MOS transistor is in cutt off region, the electric field across the pinch-off region may be high enough that carriers gain there enough energy to excite electron-hole pairs.

C a MOS transistor is in saturation , the electric field across the pinch-off region may be high enough that carriers gain there enough energy to excite electron-hole pairs.

D In all regions

Add a Question

Multiple Choice **True / False** **Short Answer**

socrative

Name _____
Date _____

ENCS333 QZ1 MARCH 24

Score _____

1. What are the different operating regions foe a MOS transistor?

(A) Cutoff region

(B) Non- Saturated Region

(C) Saturated Region

(D) All are correct

2. What are the different MOS layers?

(A) n-diffusion

(B) p-diffusion

(C) Polysilicon

(D) Metal

(E) all of the above

3. What are the various Silicon wafer Preparation?

(A) Crystal growth & doping

(B) Ingot trimming & grinding

(C) Verilog code preparation

(D) Wafer polishing & etching and Wafer cleaning.

(E) all of the above are correct except Verilog code preparation

4. If a large Vds is applied this voltage with deplete the Inversion layer .This Voltage effectively pinches off the channel near the source.

(T) True

(F) False

5. There are only three different layers in MOS transistors which are Drain , Source & Gate

(T) True

(F) False

6. Threshold voltage in CMOS Defined as : The Threshold voltage, VT for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current, IDS effectively drops to zero.

(T) True

(F) False

7. The Channel-length modulatio , the The current between **drain and source terminals is constant and** independent of the applied voltage over the terminals. This is not entirely correct. The effective length of the conductive channel is actually modulated by the applied VDS, increasing VDS causes the depletion region at the drain junction to grow, reducing the length of the effective channel.

(T) True

(F) False

8. Define Rise time ? which device nMOS or PMOS determines the Rise time?

In slides rise related to p device size, we mesure 20-80% of the rise signal

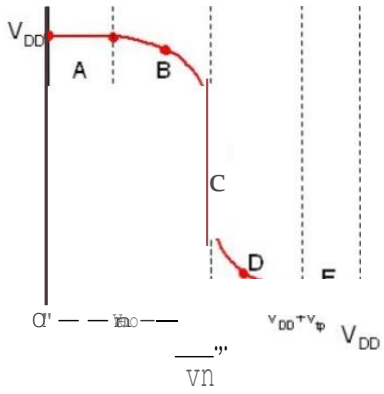
9. Define Fall time ? which device nMOS or PMOS determines the fall time?

In slides fall related to ndevice, same we mesure 20-80% of fall time

10. Define Delay time ?

In slides
Between two signal or input and output measured at 50%

11. What are the different operating regions for an NMOS transistor IN EACH REGION AS SHOWN IN THE FIGURE?



In slides

REGION	nMos	pMOS
A		
B		
C		
D		
E		

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Save and Exit

ENCS333_SEC2_SEP22

Align Quiz to Standard

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SOC-50727200

1. To have a complement CMOS we do not need

A n-type transistors

B p-type transistors

C package

2. What are the different parts of MOS transistors?

A Drain , Source & Gate and bulk

B Source & Gate

C Drain , Source

D Drain , Source & Gate

E bulk, Drain , Source

3. we can classify IC according to

A Signal Type

B Signal Name

C Analog or digital

4. The first transistor was created in

A Bell Labs

B China

C circuit design

5. Moore's law stated that the number of transistors in ICs doubles every ------ months

A 2 years

B 17 months

C 16 months

D 18 months

6. Technology shrinks or scaling , refers to which parameter of the transistor

A Drain

B source

C Gate length

D bulk

7. We need a ---------- to run spice simulations

A device model

B power

C ground

D netlist

E all mentioned

8. in chip design, Wafer made of

A silicon

B Germanium

C copper

D None of mentioned

9. Die is larger than a waver

False

10. package is technology used to interface between die and outside word

True

11. CMOS stands for ----------

A complementary material oxide state

B commuter material or silicon

C commuter metal organization states

D complementary metal oxide silicon

E Non of above

12. which sentences is true a bout Ntype and Ptype transistor

A they both made of silicon

B they both use as switch

C Ntype is slow

D ptype is faster than ntype

E Both use to build CMOS logic

Add a Question

Multiple Choice **True / False** **Short Answer**

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Save and Exit

ENCS333_SEC1_SEP22

Align Quiz to Standard

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SOC-50660792

1. What is the transistors CMOS technology provides?

A n-type transistors only

B p-type transistors only

C n-type transistors and p-type transistors

D non of the above

2. What are the different layers in MOS transistors?

A Drain

B Source & Gate

C Drain , Source

D Drain , Source & Gate

E bulk, Drain , Source

F Drain , Source & Gate and bulk

3. IC Classified according to

A Signal Type

B Signal Name

C Number of devices used

4. 1948 , The first ---------- was created in Bell Labs

A computer

B transistor

C high performance computer

5. Moore's law was discovered, according to which the number of transistors in ICs doubles every ------ months

A 3 years

B 24 months

C 18 months

D 6 months

6. Technology shrinks or scaling , refers to which parameter of the transistor

A Drain

10. package is technology used to interface between die and outside word

True

11. CMOS stands for ----------

A complementary material oxide state

B commuter material or silicon

C commuter metal organization states

D complementary metal oxide silicon

E Non of above

12. which sentences is true a bout Ntype and Ptype transistor

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Add a Question