



**Faculty of Engineering and Technology
Electrical and Computer Engineering
Department**

**ENEE2102
CIRCUITS LAB**

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Pre lab

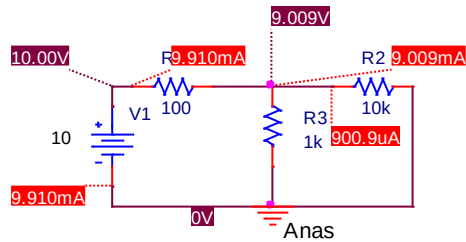
17/12/2017

Eng: Qais samara

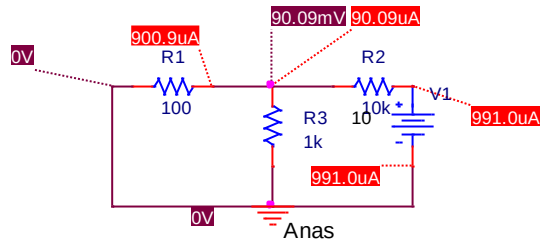
DR: Hakam shhada

Q1)

case one: $V_2=0$

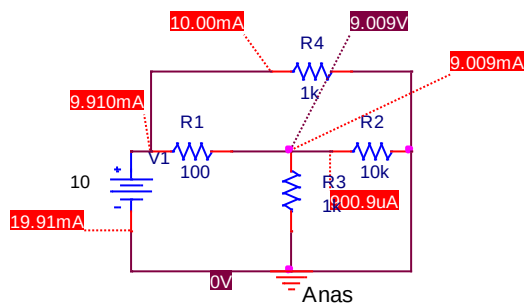


Case two: $V_1=0$

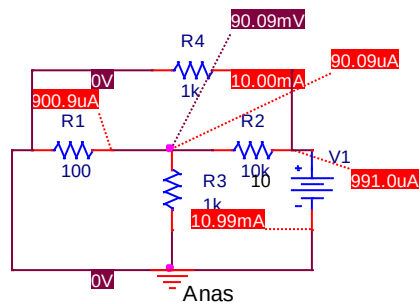


Q2)

Case 1: $V_2=0$

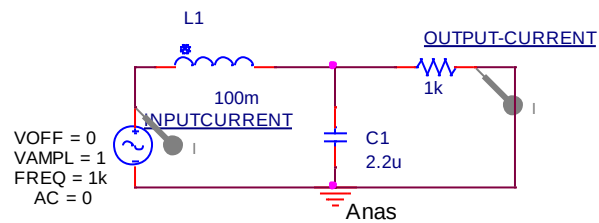


Case2: $V_1=0$

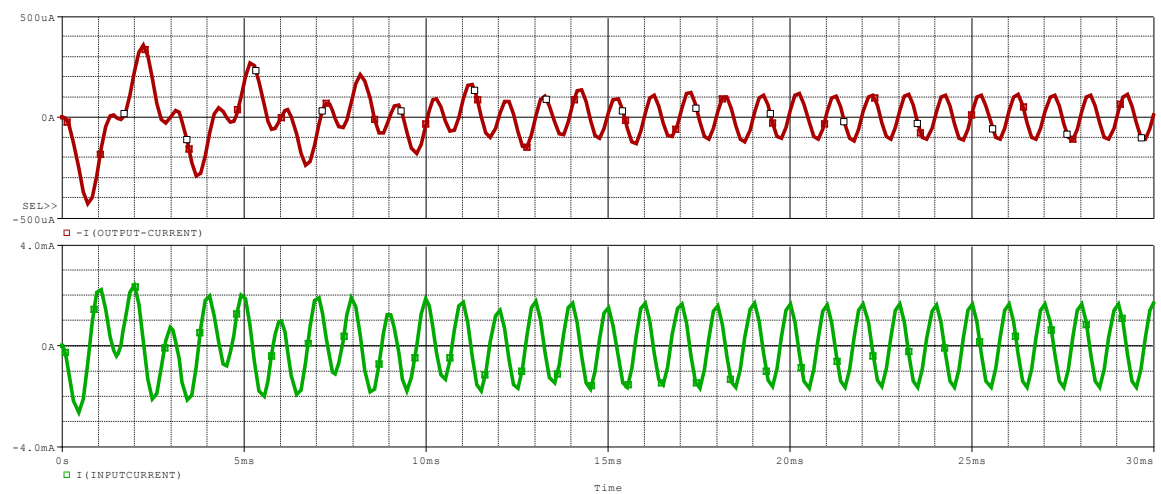


Q3)

Case 1 : $v_2=0$



The result:



Case 2: V1 is open:

