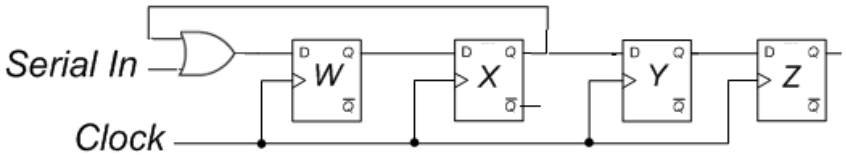
ENCS2340 I Section 2 I Fall 2024/2025
Chapter 6 - Extra Exercises

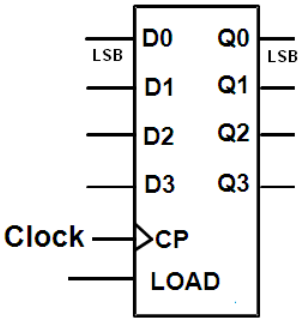
Notes: → Always show clearly all work used to get your answers
For Questions 4 use the template on page 3 for the connection diagram.

1. Initially the feedback D-type shift register shown has the contents WXYZ = 0110. For the sequence of the serial input shown in the table below, fill in the spaces in the table to indicate the register contents following the arrival of each of the next five clock pulses. In the last column, express the contents in HEX.



Clock Pulse #	Serial Input, just before the arrival of the next clock pulse	W	X	Y	Z	Register Contents (in Hex)
Initial State	1	0	1	1	0	6
1	0					
2	0					
3	1					
4	0					
5	1					

2. Given the 4-bit synchronous binary down counter with a parallel load synchronous input (LOAD) (shown opposite).



   a. Add the required logic to obtain a counter that follows the following counting sequence: …11, 10, 9, 8, 7, 6, 5, 11, 10, 9, 8, 7, 6, 5, …..

   b. This counter is a modulo- _____ counter.

   c. This counter is a divide-by- _____ counter.

   d. Sketch the Q3 output (the MSB) for the counting sequence given in (a) above and use the result to verify your answer in (c).

   e. With a clock frequency of 1400 pulses per second, the signal at output Q3 of the counter has a frequency of _____ pulses per second.

3. A 4-bit BCD down counter has the state table shown. States above 9 lead to "don't care" states. We would like to design such a counter using each of the following methods:

   a. JK flip flops + AND-OR gates, where needed at the combined JK inputs, to control the toggling of the various counter stages (**Note: J and K inputs of each FF are connected together**).
   b. D flip flops + XOR gates, where needed at the D inputs, to control toggling of the various counter stages. The XOR controls feedback from the FF Q output.
   c. D flip flops + AND-OR gates, where needed at the D inputs, to determine the next output of the various counter stages directly through setting or resetting at the D input.

State Table for BCD Down Counter

Present State				Next State			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	0	1	1
0	1	0	1	0	1	0	0
0	1	1	0	0	1	0	1
0	1	1	1	0	1	1	0
1	0	0	0	0	1	1	1
1	0	0	1	1	0	0	0

6. Using a 4-bit D-type register (Q3Q2Q1Q0), a 4-bit adder/$\overline{\text{Subtractor}}$, MUXs, and additional logic gates where needed, design a 4-bit counter that has 3 synchronous control inputs as shown in the given functional table.

$\overline{\text{CLR}}$	**Load**	Up/ $\overline{\text{Down}}$	**Action Taken on Next Clock Edge**
0	X	X	Clear counter
1	1	X	Parallel Load with External Inputs (I3I2I1I0)
1	0	0	Decrement by 3
1	0	1	Increment by 2

7. Using *D* flip-flop(s) and MUX(s) **only** (i.e., other components are not allowed), draw the logic diagram for a **4-bit register** (Q3Q2Q1Q0) with mode selection inputs S_1S_0. The register should operate according to the following table:

S_1S_0	Register operation
00	Hold the current contents of the register (i.e. stay the same)
01	Parallel load (load external data inputs (I3I2I1I0) in parallel into register)
10	Rotate ***right*** (i.e., shift register contents to the ***right*** (Q3→Q2→Q1→Q0) and feeding in the shifted bit out of Q0 as input to the Q3 stage. See illustration.
11	Load the register with the 1's complement of the current content.

You must clearly label the D flip-flop(s) and MUX(s) used together with all inputs and outputs.