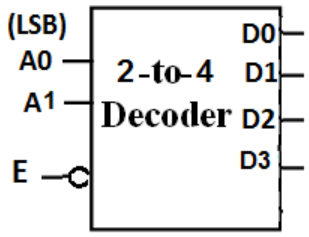
ENCS2340 | Section 2 | Fall 2024/2025
Chapter 4
Extra Exercises - 02

1. Consider a 2-to-4 decoder with **active-high** outputs and **active-low** Enable input E. (See label shown)



   a. Give the complete truth table for the decoder with E = 0.

   b. With E = 1, all the outputs will be _____(0/1) regardless of the inputs

   c. If the decoder is implemented directly by deriving the minterms of the input, give a complete logic diagram of the decoder including the Enable capability.

   d. Give a logic diagram for using the minimum number of this 2-to-4 decoder (and additional gates as required) to obtain:
      i. A 1-to-4 Demultiplexer
      ii. An 4-to-1 Multiplexer
      iii. A 3-to-8 Decoder
      iv. A half adder

2. An 8-to-3 priority encode has inputs D7D6…D0 and outputs A2A1A0 (A0 the LSB). D7 represents the lowest priority input and D0 the highest priority input.

   a. With the encoder output A2A1A0 = 100:
      i. Give the corresponding input bit pattern D7D6…D0, assigning X to the bits where the input can be either 0 or 1 (don't care).
      ii. How many changes can be applied at the input without affecting the output code (100) generated?

   b. With the input D7D6……D1D0 = 11011000, the output A2A1A0 = _____(in binary)

3. Use only one decoder of the appropriate size and 3 OR gates to implement a circuit that converts a 4-bit signed-1's complement binary number X (X = X3X2X1X0) to its 3-bit magnitude Y (Y=Y2Y1Y0), i.e. Y = |X|. X0 and Y0 are the LSBs of X and Y, respectively,

4. A combination circuit has 3 outputs, each being a function of 3 inputs X, Y, Z (Z is the LSB):

$$F1 = (X + \overline{Y})(X + Z)$$
$$F2 = \Sigma(0,1,5,6)$$
$$F3 = \Pi(1,4,6,7)$$

   a. Derive the truth table for the complete circuit

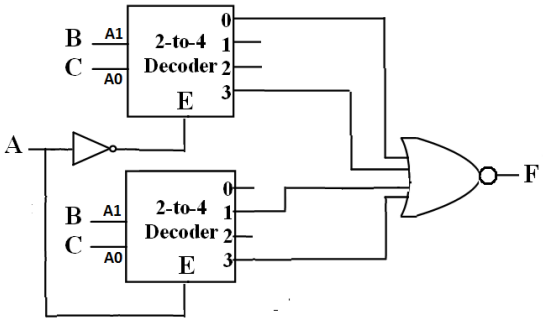
   b. Show the logic diagram for implementing F1 only using a suitable decoder and an OR gate.

   c. Implement function F2 using the decoder in (b) and a NOR gate of the appropriate size. Show your solution on the same figure for part (b).

   d. Implement function F3 using:

      i. A 4-to-1 multiplexer and one inverter (if needed).
      ii. A 2-to-1 multiplexer with minimum additional logic (Use K-maps of the appropriate size to do the logic minimization)

5. Analyze the circuit shown and express the output F:



   a. In the canonical form Σm ().
   b. As an algebraic product of maxterms.

   Note: The 3 inputs ABC have C as the least significant bit (LSB) and A as the most significant bit (MSB).

   Hint: Start by labeling D0, D1, …D7 of the resulting larger decoder.

Important Note for Questions 6 to 7:

In each of the following two questions, give a neat block diagram and indicate the functional block type. Clearly label all inputs and outputs of each block.

6. Solve Problem 3 using a functional block-based approach utilizing the following function blocks and logic components: Quad 2-to-1 Multiplexer, inverters as required. Give a neat logic diagram and clearly label all block inputs and outputs.

7. Use the minimum number required any of the following components: **inverters, multiplexers, 4-bit adder(1)/subtractor(0), 4-bit magnitude comparators**, to design a circuit that takes two 4-bit unsigned binary numbers $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$ and a 2-bit user selection input $S = S_1S_0$. The circuit should produce a 4-bit output $O = O_3O_2O_1O_0$ according to the following table:

S_1S_0	Output O is equal to
00	Min(A, B)
01	Floor(A/2)
10	A-B
11	A+B