11–7 NETWORK FUNCTION DESIGN

Finding and using a network function of a given circuit is an *s*-domain **analysis** problem. An *s*-domain **synthesis** problem involves finding a circuit that realizes a given network function. For linear circuits, an analysis problem always has a unique solution. In contrast, a synthesis problem may have many solutions because different circuits can have the same network function. A transfer function design problem involves synthesizing several circuits that realize a given function and evaluating the alternative designs, using criteria such as input or output impedance, cost, and power consumption.

The design process discussed here begins with a given transfer function $T_V(s)$. We partition this transfer function into a product of simpler functions.

$$T_V(s) = T_{V1}(s)T_{V2}(s)\cdots T_{Vk}(s)$$

We then realize each of these simpler functions using basic circuit modules such as voltage dividers, inverting amplifiers, and noninverting amplifiers. The overall transfer function is then achieved by connecting the individual stages in cascade, as indicated in Figure 11–32.

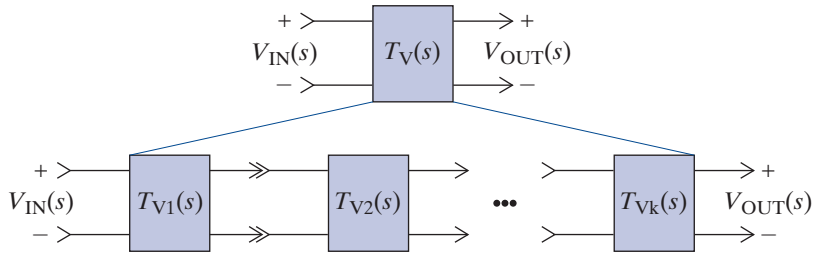


FIGURE 11–32 *Cascade connection transfer functions.*

Of course, this approach assumes that the chain rule applies. In other words, we must avoid loading when designing the stages in the cascade realization. This is accomplished by coordinating the input and output impedances of adjacent stages or using OP AMP voltage followers to isolate the individual stages.

Before turning to examples, we discuss the design of simple one-pole modules that serve as the building block stages in a cascade design.

FIRST-ORDER VOLTAGE-DIVIDER CIRCUIT DESIGN

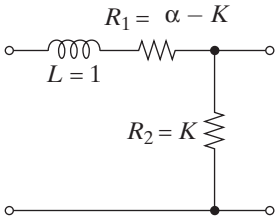
We begin our study of transfer function design by developing a voltage-divider realization of a first-order transfer function of the form $K/(s+\alpha)$. The impedances $Z_1(s)$ and $Z_2(s)$ are related to the given transfer function using the voltage-divider relationship.

$$T_V(s) = \frac{K}{s+\alpha} = \frac{Z_2(s)}{Z_1(s)+Z_2(s)} \qquad (11\text{–}26)$$

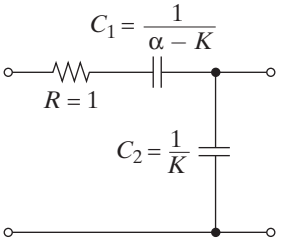
To obtain a circuit realization, we must assign part of the given $T_V(s)$ to $Z_2(s)$ and the remainder to $Z_1(s)$. There are many possible realizations of $Z_1(s)$ and $Z_2(s)$ because there is no unique way to make this assignment. For example, simply equating the numerators and denominators in Eq. (11–26) yields

$$Z_2(s) = K \quad \text{and} \quad Z_1(s) = s+\alpha-Z_2(s) = s+\alpha-K \qquad (11\text{–}27)$$

Inspecting this result, we see that $Z_2(s)$ is realizable as a resistance ($R_2 = K\Omega$) and $Z_1(s)$ as an inductance ($L_1 = 1\,\text{H}$) in series with a resistance $[R_1 = (\alpha - K)\Omega]$. The resulting circuit diagram is shown in Figure 11–33(a). For $K = \alpha$ the resistance R_1 can be replaced by a short circuit because its resistance is zero. A gain restriction $K \le \alpha$ is necessary because a negative R_1 is not physically realizable as a single component.



(a) *RL* design



(b) *RC* design

FIGURE 11–33 *Circuit realizations of $T(s) = K/(s+\alpha)$ for $K \le \alpha$.*

An alternative synthesis approach involves factoring s out of the denominator of the given transfer function. In this case, Eq. (11–26) is rewritten in the form

$$T_V(s) = \frac{K/s}{1 + \alpha/s} = \frac{Z_2(s)}{Z_1(s) + Z_2(s)} \tag{11–28}$$

Equating numerators and denominators yields the branch impedances

$$Z_2(s) = \frac{K}{s} \quad \text{and} \quad Z_1(s) = 1 + \frac{\alpha}{s} - Z_2(s) = 1 + \frac{\alpha - K}{s} \tag{11–29}$$

In this case we see that $Z_2(s)$ is realizable as a capacitance ($C_2 = 1/K$ F) and $Z_1(s)$ as a resistance ($R_1 = 1\,\Omega$) in series with a capacitance [$C_1 = 1/(\alpha - K)$ F]. The resulting circuit diagram is shown in Figure 11–33(b). For $K = \alpha$, the capacitance C_1 can be replaced by a short circuit because its capacitance is infinite. A gain restriction $K \leq \alpha$ is required to keep C_1 from being negative.

As a second design example, consider a voltage-divider realization of the transfer function $Ks/(s + \alpha)$. We can find two voltage-divider realizations by writing the specified transfer function in the following two ways:

$$T(s) = \frac{Ks}{s + \alpha} = \frac{Z_2(s)}{Z_1(s) + Z_2(s)} \tag{11–30a}$$

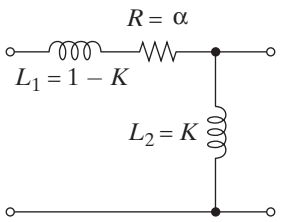
$$T(s) = \frac{K}{1 + \alpha/s} = \frac{Z_2(s)}{Z_1(s) + Z_2(s)} \tag{11–30b}$$

Equation (11–30a) uses the transfer function as given, while Eq. (11–30b) factors s out of the numerator and denominator. Equating the numerators and denominators in Eqs. (11–30a) and (11–30b) yields two possible impedance assignments:

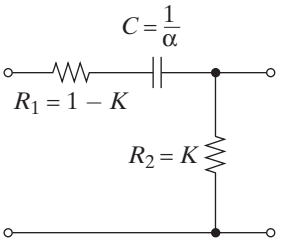
$$\text{Using Eq. (11–30a): } Z_2 = Ks \quad \text{and} \quad Z_1 = s + \alpha - Z_2 = (1 - K)s + \alpha \tag{11–31a}$$

$$\text{Using Eq. (11–30b): } Z_2 = K \quad \text{and} \quad Z_1 = 1 + \frac{\alpha}{s} - Z_2 = (1 - K) + \frac{\alpha}{s} \tag{11–31b}$$

The assignment in Eq. (11–31a) yields $Z_2(s)$ as an inductance $L_2 = K$ H and $Z_1(s)$ as an inductance [$L_1 = (1 - K)$ H] in series with a resistance ($R_1 = \alpha\,\Omega$). The assignment in Eq. (11–31b) yields $Z_2(s)$ as a resistance ($R_2 = K\Omega$) and $Z_1(s)$ as a resistance [$R_1 = (1 - K)\Omega$] in series with a capacitance ($C_1 = 1/\alpha$ F). The two realizations are shown in Figure 11–34. Both realizations require $K \leq 1$ for the branch impedances to be realizable and both simplify when $K = 1$.



(a) *RL* design



(b) *RC* design

FIGURE 11–34 *Circuit realizations of $T(s) = Ks/(s + \alpha)$ for $K \leq 1$.*

Design Exercise 11–23

Design an *RC* circuit to realize the following transfer function

$$T(s) = \frac{200}{s + 1000}$$

Answer: Use the circuit of Figure 11–33(b) with $R = 1\,\Omega$, $C_1 = 1250\,\mu$F, and $C_2 = 5000\,\mu$F. We will learn how to scale these answers to more practical device values later in this section.

VOLTAGE-DIVIDER AND OP AMP CASCADE CIRCUIT DESIGN

The examples in Figures 11–33 and 11–34 illustrate an important feature of voltage-divider realizations. In general, we can write a transfer function as a quotient of polynomials $T(s) = r(s)/q(s)$. A voltage-divider realization requires the impedances $Z_2(s) = r(s)$ and $Z_1(s) = q(s) - r(s)$ to be physically realizable. A voltage-divider

circuit usually places limitations on the gain K. This gain limitation can be overcome by using an OP AMP circuit in cascade with the divider circuit.

For example, a voltage-divider realization of the transfer function in Eq. (11–26) requires $K \leq \alpha$. When $K > \alpha$, then $T(s)$ is not realizable as a simple voltage divider, since $Z_2(s) = s + \alpha - K$ requires a negative resistance. However, the given transfer function can be written as a two-stage product:

$$T_v(s) = \frac{K}{s+\alpha} = \underbrace{\left[\frac{K}{\alpha}\right]}_{\text{first stage}} \underbrace{\left[\frac{\alpha}{s+\alpha}\right]}_{\text{second stage}}$$

When $K > \alpha$, the first stage has a positive gain greater than unity. This stage can be realized using a noninverting OP AMP circuit with a gain of $(R_1 + R_2)/R_1$. The first-stage design constraint is

$$\frac{K}{\alpha} = \frac{R_1 + R_2}{R_1}$$

Choosing $R_1 = 1\,\Omega$ requires that $R_2 = (K/\alpha) - 1$. An RC voltage-divider realization of the second stage is obtained by factoring an s out of the stage transfer function. This leads to the second-stage design constraint

$$\frac{\alpha/s}{1 + \alpha/s} = \frac{Z_2(s)}{Z_1(s) + Z_2(s)}$$

Equating numerators and denominators yields $Z_2(s) = \alpha/s$ and $Z_1(s) = 1$. Figure 11–35 shows a cascade connection of a noninverting first stage and the RC divider second stage. The chain rule applies to this circuit, since the first stage has an OP AMP output. The cascade circuit in Figure 11–35 realizes the first-order transfer function $K/(s + \alpha)$ for $K > \alpha$, a gain requirement that cannot be met by the divider circuit alone.

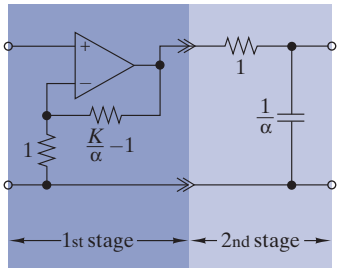


FIGURE 11–35 *Circuit realization of $T(s) = K/(s + \alpha)$ for $K > \alpha$.*

Design Exercise 11–24

Design an active RC circuit to realize the following transfer function

$$T(s) = \frac{2000}{s + 1000}$$

Answer: Use the circuit shown in Figure 11–35. The OP AMP stage has a gain of 2 by making both resistors equal. Choose the components in the second stage voltage divider so that $R = 1\ \Omega$ and $C = 1000\ \mu$F. We will leam how to scale these answers to more practical device values later in this section.

Design Exercise 11–25

Design an active RL circuit to realize the following transfer function

$$T(s) = \frac{2000}{s + 1000}$$

Answer: Use the circuit shown in Figure 11–35. The OP AMP stage has a gain of 2 by making both resistors equal. In the second stage, replace the resistor with an inductor and replace the capacitor with a resistor. Let the components in the second stage voltage divider be $R = 1\ \text{k}\Omega$ and $L = 1$ H.

DESIGN EXAMPLE 11–20

Design a circuit to realize the following transfer function using only resistors, capacitors, and OP AMPs:

$$T_V(s) = \frac{3000s}{(s+1000)(s+4000)}$$

SOLUTION:

The given transfer function can be written as a three-stage product.

$$T_v(s) = \underbrace{\left[\frac{K_1}{s+1000}\right]}_{\text{first stage}} \underbrace{[K_2]}_{\text{second stage}} \underbrace{\left[\frac{K_3 s}{s+4000}\right]}_{\text{third stage}}$$

where the stage gains K_1, K_2, and K_3 have yet to be selected. Factoring s out of the denominator of the first-stage transfer function leads to an RC divider realization:

$$\frac{K_1/s}{1+1000/s} = \frac{Z_2(s)}{Z_1(s)+Z_2(s)}$$

Equating numerators and denominators yields

$$Z_2(s) = K_1/s \quad \text{and} \quad Z_1(s) = 1 + (1000 - K_1)/s$$

The first stage $Z_1(s)$ is simpler when we select $K_1 = 1000$. Factoring s out of the denominator of the third-stage transfer function leads to an RC divider realization:

$$\frac{K_3}{1+4000/s} = \frac{Z_2(s)}{Z_1(s)+Z_2(s)}$$

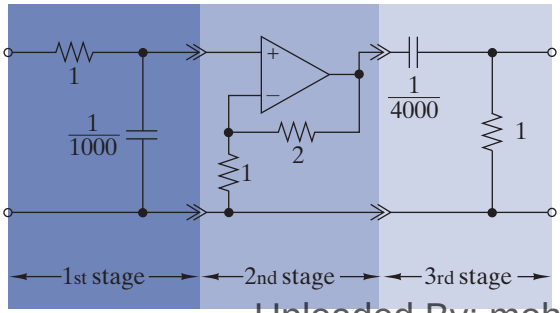
Equating numerators and denominators yields

$$Z_2(s) = K_3 \quad \text{and} \quad Z_1(s) = 1 - K_3 + 4000/s$$

The third stage $Z_1(s)$ is simpler when we select $K_3 = 1$. The stage gains must meet the constraint $K_1 \times K_2 \times K_3 = 3000$ since the overall gain of the given transfer function is 3000. We have selected $K_1 = 1000$ and $K_3 = 1$, which requires $K_2 = 3$. The second stage must have a positive gain greater than 1 and can be realized using a noninverting amplifier with $K_2 = (R_1 + R_2)/R_1 = 3$. Selecting $R_1 = 1\Omega$ requires that $R_2 = 2\Omega$.

Figure 11–36 shows the three stages connected in cascade. The chain rule applies to this cascade connection because the OP AMP in the second stage isolates the RC voltage-divider circuits in the first and third stages. The order of the first and third stages can be swapped in this design without consequence. The circuit in Figure 11–36 realizes the given transfer function but is not a realistic design because the values of resistance and capacitance are impractical. For this reason we call this circuit a **prototype** design. We will shortly discuss how to scale a prototype to obtain practical element values.

FIGURE 11–36



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Design Exercise 11–26

Design a circuit to realize the following transfer function using only resistors, capacitors, and no more than one OP AMP.

$$T_V(s) = \frac{10^6}{(s + 10^3)^2}$$

Answer: Figure 11–37 shows one possible prototypical solution.

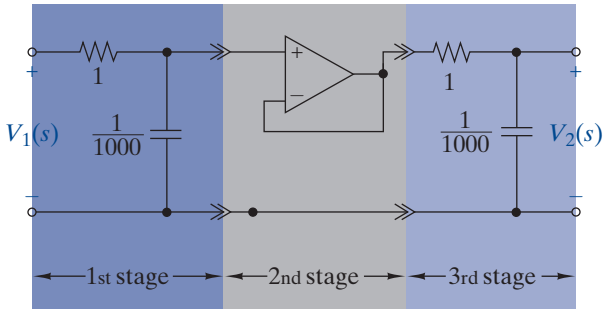

FIGURE 11–37

INVERTING OP AMP CIRCUIT DESIGN

The inverting OP AMP circuit places fewer restrictions on the form of the desired transfer function than does the basic voltage divider. To illustrate this, we will develop two inverting OP AMP designs for a general first-order transfer function of the form

$$T_V(s) = -K\,\frac{s + \gamma}{s + \alpha}$$

The general transfer function of the inverting OP AMP circuit is $-Z_2(s)/Z_1(s)$, which leads to the general design constraint

$$-K\,\frac{s + \gamma}{s + \alpha} = -\frac{Z_2(s)}{Z_1(s)} \qquad (11\text{–}32)$$

The first design is obtained by equating the numerators and denominators in Eq. (11–32) to obtain the OP AMP circuit impedances as $Z_2(s) = Ks + K\gamma$ and $Z_1(s) = s + \alpha$. Both of these impedances are of the form $Ls + R$ and can be realized by an inductance in series with a resistance, leading to the design realization in Figure 11–38(a).

A second inverting OP AMP realization is obtained by equating $Z_2(s)$ in Eq. (11–32) to the reciprocal of the denominator and equating $Z_1(s)$ to the reciprocal of the numerator. This assignment yields the impedances $Z_1(s) = 1/(Ks + K\gamma)$ and $Z_2(s) = 1/(s + \alpha)$. Both of these impedances are of the form $1/(Cs + G)$, where Cs is the admittance of a capacitor and G is the admittance of a resistor. Both impedances can be realized by a capacitance in parallel with a resistance. These impedance identifications produce the *RC* circuit in Figure 11–38(b).

Because it has fewer restrictions, it is often easier to realize transfer functions using the inverting OP AMP circuit. To use inverting circuits, the given transfer function must require an inversion or be realized using an even number of inverting stages. In some cases, the sign in front of the transfer function is immaterial and the required transfer function is specified as $\pm T_V(s)$. *Caution:* The input impedance of an inverting OP AMP circuit may load the source circuit.

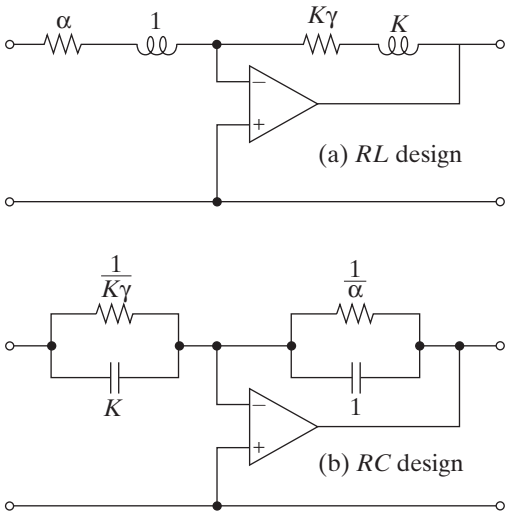

FIGURE 11–38 *Inverting OP AMP circuit realizations of* $T(s) = -K(s + \gamma)/(s + \alpha)$.

Design Exercise 11–27

Design an active *RC* prototype circuit to realize the following transfer function

$$T(s) = -100\frac{s + 50}{s + 100}$$

Answer: See Figure 11–39.

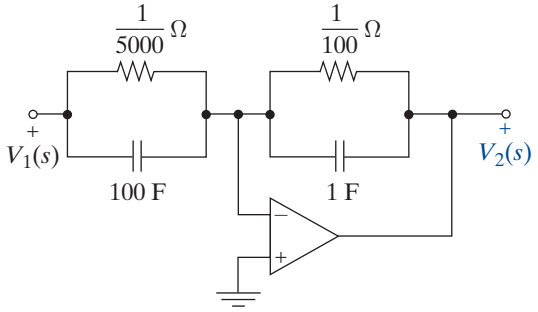

FIGURE 11–39

DESIGN EXAMPLE 11–21

Design a circuit to realize the transfer function given in Example 11–20 using inverting OP AMP circuits.

SOLUTION:

The given transfer function can be expressed as the product of two inverting transfer functions:

$$T_V(s) = \frac{3000s}{(s + 1000)(s + 4000)} = \underbrace{\left[-\frac{K_1}{s + 1000}\right]}_{\text{first stage}}\underbrace{\left[-\frac{K_2 s}{s + 4000}\right]}_{\text{second stage}}$$

where the stage gains K_1 and K_2 have yet to be selected. The first stage can be realized in an inverting OP AMP circuit since

$$-\frac{K_1}{s + 1000} = -\frac{K_1/1000}{1 + s/1000} = -\frac{Z_2(s)}{Z_1(s)}$$

Equating the $Z_2(s)$ to the reciprocal of the denominator and $Z_1(s)$ to the reciprocal of the numerator yields

$$Z_2 = \frac{1}{1 + s/1000} \quad \text{and} \quad Z_1 = 1000/K_1$$

The impedance $Z_2(s)$ is realizable as a capacitance ($C_2 = 1/1000\,\text{F}$) in parallel with a resistance ($R_2 = 1\Omega$) and $Z_1(s)$ as a resistance ($R_1 = 1000/K_1\Omega$). We select $K_1 = 1000$ so that the two resistances in the first stage are equal. Since the overall gain requires $K_1 \times K_2 = 3000$, this means that $K_2 = 3$. The second-stage transfer function can also be produced using an inverting OP AMP circuit:

$$-\frac{3s}{s + 4000} = -\frac{3}{1 + 4000/s} = -\frac{Z_2(s)}{Z_1(s)}$$

Equating numerators and denominators yields $Z_2(s) = R_2 = 3$ and $Z_1(s) = R_1 + 1/C_1 s = 1 + 4000/s$.

Figure 11–40 shows the cascade connection of the *RC* OP AMP circuits that realize each stage. The overall transfer function is noninverting because the cascade uses an even number of inverting stages. The chain rule applies here since the first stage has an OP AMP output. The circuit in Figure 11–40 is a prototype design because the values of resistance and capacitance are impractical.

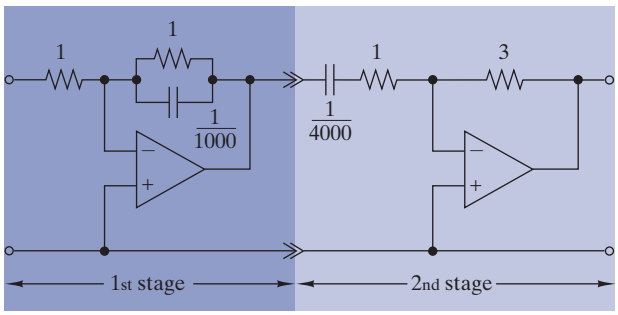

FIGURE 11–40

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Design Exercise 11–28

Design a circuit to realize the following transfer function using only resistors, capacitors, and no more than one OP AMP.

$$T_V(s) = \frac{-10^6}{(s + 10^3)^2}$$

Answer: Figure 11–41 shows one possible prototypical solution.

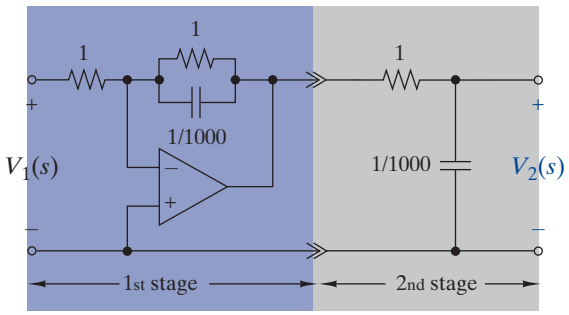

FIGURE 11–41

MAGNITUDE SCALING

The circuits obtained in Examples 11–20 and 11–21 are called prototype designs because the element values are outside of practical ranges. The allowable ranges depend on the fabrication technology used to construct the circuits. For example, monolithic integrated circuit (IC) technology limits capacitances to a few hundred picofarads, and inductors are difficult to manufacture on ICs. An OP AMP circuit should have a feedback resistance greater than 1 kΩ to keep the output current demand within the capabilities of general-purpose OP AMP devices. Other technologies and applications place different constraints on element values. For example, the power industry, where physical size is of less importance, uses devices with much larger values than the electronics industry.

There are no hard and fast rules here, but, roughly speaking, an electronic circuit is probably realizable by some means if its passive element values fall in the ranges shown in the tables on the inside rear cover, with the caveat that OP AMP circuits generally use Rs > 1 kΩ.

These are:

Capacitors[4]: 1 pF to 10,000 μF

Inductors[5]: 10 nH to 10 mH

Resistors[6]: 10 Ω to 10 MΩ.

The important idea here is that circuit designs like Figure 11–40 are impractical because 1-Ω resistors are too small for OP AMP circuits and 1-mF capacitors are too large physically.

It is often possible to scale the magnitude of circuit impedances so that the element values fall into practical ranges. The key is to scale the element values in a way that does not change the transfer function of the circuit. Multiplying the numerator and denominator of the transfer function of a voltage-divider circuit by a scale factor k_m yields

$$T_V(s) = \frac{k_m}{k_m}\frac{Z_2(s)}{Z_1(s)+Z_2(s)} = \frac{k_m Z_2(s)}{k_m Z_1(s)+k_m Z_2(s)} \tag{11–33}$$

Clearly, this modification does not change the transfer function but scales each impedance by a factor of k_m and changes the element values in the following way:

$$R_{\text{after}} = k_m R_{\text{before}} \quad L_{\text{after}} = k_m L_{\text{before}} \quad C_{\text{after}} = \frac{C_{\text{before}}}{k_m} \tag{11–34}$$

Equation (11–34) was derived using the transfer function of a voltage-divider circuit. It is easy to show that we would reach the same conclusion if we had used the transfer functions of inverting or noninverting OP AMP circuits.

In general, a circuit is magnitude scaled by multiplying all resistances, multiplying all inductances, and dividing all capacitances by a scale factor k_m. The scale factor must be positive, but can be greater than or less than 1. Different scale factors can be used for each stage of a cascade design, but only one scale factor can be used for each stage. These scaling operations do not change the voltage transfer function realized by the circuit.

---

[4]Recent innovations in dielectrics have enabled a large new class of electronic double-layer capacitors (EDLC) or *supercapacitors* with capacitances up to 5000 F. These devices are still relatively large for small electronic applications.

[5]Inductors up to 10 H, also called *chokes,* are possible but are quite large.

[6]Resistors are manufactured outside this range but are used only in specialty applications.

Our design strategy is first to create a prototype circuit whose element values may be unrealistically large or small. Applying magnitude scaling to the prototype produces a design with practical element values. Sometimes there may be no scale factor that brings the prototype element values into a practical range. When this happens, we must seek alternative realizations because the scaling process is telling us that the prototype is not a viable candidate.

EXAMPLE 11–22

Magnitude scale the circuit in Figure 11–40 so all resistances are at least 10 kΩ and all capacitances are less than 1 μF.

SOLUTION:

The resistance constraint requires $k_m R \geq 10^4\ \Omega$. The smallest resistance in the prototype circuit is 1 Ω; therefore, the resistance constraint requires $k_m \geq 10^4$. The capacitance constraint requires $C/k_m \leq 10^{-6}$ F. The largest capacitance in the prototype is 10^{-3} F; therefore, the capacitance constraint requires $k_m \geq 10^3$. The resistance condition on k_m dominates the two constraints. Selecting $k_m = 10^4$ produces the scaled design in Figure 11–42. This circuit realizes the same transfer function as the prototype in Figure 11–40 but uses practical element values.

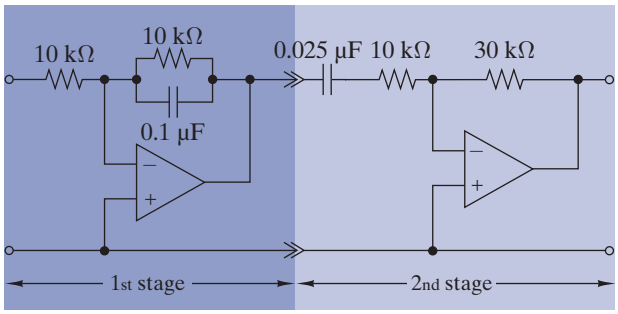

FIGURE 11–42

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Exercise 11–29

Select a magnitude scale factor for each stage in Figure 11–36 so that both capacitances are 0.01 μF and all resistances are greater than 10 kΩ.

Answer: $k_m = 10^5$ for the first stage; $k_m = 10^4$ for the second stage; $k_m = 0.25 \times 10^5$ for the third stage.

Exercise 11–30

Select a magnitude scale factor for the OP AMP circuit in Figure 11–39.

Answer: $k_m = 10^8$, any larger and the feedback resistor becomes too large, any smaller and the input capacitor becomes too large.

SECOND-ORDER CIRCUIT DESIGN

An *RLC* voltage divider can also be used to realize second-order transfer functions. For example, the transfer function

$$T_V(s) = \frac{K}{s^2 + 2\zeta\omega_0 s + \omega_0^2}$$

can be realized by factoring s out of the denominator and equating the result to the voltage-divider input-output relationship:

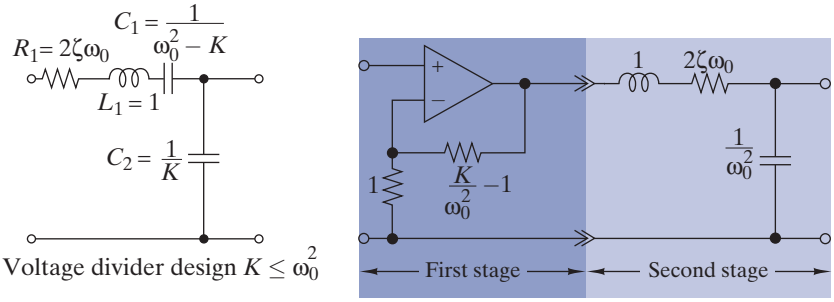
$$T_V(s) = \frac{K/s}{s + 2\zeta\omega_0 + \omega_0^2/s} = \frac{Z_2(s)}{Z_1(s) + Z_2(s)}$$

Equating numerators and denominators yields

$$Z_2(s) = \frac{K}{s} \text{ and } Z_1(s) = s + 2\zeta\omega_0 + \frac{\omega_0^2 - K}{s}$$

The impedance $Z_2(s)$ is realizable as a capacitance $(C_2 = 1/K\ \text{F})$ and $Z_1(s)$ as a series connection of an inductance $(L_1 = 1\ \text{H})$, resistance $(R_1 = 2\zeta\omega_0\ \Omega)$, and capacitance $\left[C_1 = 1/\left(\omega_0^2 - K\right)\ \text{F}\right]$. The resulting voltage-divider circuit is shown in Figure 11–43(a). The impedances in this circuit are physically realizable when $K \le \omega_0^2$. Note that the resistance controls the damping ratio ζ because it is the element that dissipates energy in the circuit. Also note that if $K = \omega_0^2$, then the capacitor C_1 is replaced by a short circuit.

FIGURE 11–43 *Second-order circuit realizations.*



(a) Voltage divider design $K \le \omega_0^2$

(b) Cascade design $K > \omega_0^2$

When $K > \omega_0^2$, we can partition the transfer function into a two-stage cascade of the form

$$T_V(s) = \underbrace{\left[\frac{K}{\omega_0^2}\right]}_{\substack{\text{first} \\ \text{stage}}} \underbrace{\left[\frac{\omega_0^2/s}{s + 2\zeta\omega_0 + \omega_0^2/s}\right]}_{\text{second stage}}$$

The first stage requires a positive gain greater than unity and can be realized using a noninverting OP AMP circuit. The second stage can be realized as a voltage divider with $Z_2(s) = \omega_0^2/s$ and $Z_1(s) = s + 2\zeta\omega_0$. The resulting cascade circuit is shown in Figure 11–43(b).

DESIGN EXAMPLE 11–23

Find a second-order realization of the transfer function given in Example 11–20.

SOLUTION:

The given transfer function can be written as

$$T_V(s) = \frac{3000s}{(s + 1000)(s + 4000)} = \frac{3000s}{s^2 + 5000s + 4 \times 10^6}$$

Factoring s out of the denominator and equating the result to the transfer function of a voltage divider gives

$$\frac{3000}{s + 5000 + 4 \times 10^6/s} = \frac{Z_2(s)}{Z_1(s) + Z_2(s)}$$

Equating the numerators and denominators yields

$$Z_2(s) = 3000 \quad \text{and} \quad Z_1(s) = s + 2000 + 4 \times 10^6/s$$

Both of these impedances are realizable, so a single-stage voltage-divider design is possible. The prototype impedance $Z_1(s)$ requires a 1-H inductor, which is a bit large. A more practical value is obtained using a scale factor of $k_m = 0.1$. The resulting scaled voltage divider circuit is shown in Figure 11–44. ■

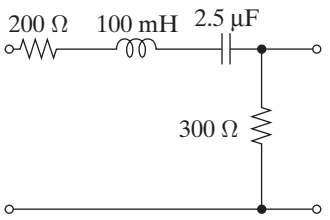


FIGURE 11–44

Design Exercise 11–31

Design a second-order circuit to realize the following transfer function:

$$T_V(s) = \frac{10^6}{(s + 10^3)^2}$$

Answer: Figure 11–45 shows one possible solution.

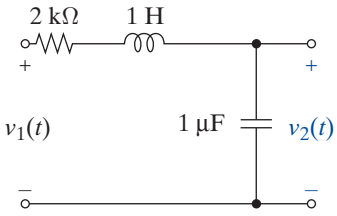


FIGURE 11–45

DESIGN EVALUATION SUMMARY

Examples 11–20, 11–21, and 11–23 show three different ways to realize the transfer function

$$T_V(s) = \frac{3000s}{(s + 1000)(s + 4000)}$$

This illustrates that a design requirement can have many solutions. Selecting the best design from among the alternatives involves additional criteria such as element count, power requirements, and output loading effects.

The element counts for each design are shown in Table 11–1. On a pure element-count basis, the *RLC* divider in Figure 11–44 in the best design. However, inductors have some serious drawbacks. They are heavy and lossy in low-frequency applications and are not easily fabricated in integrated circuit form. Fortunately, inductors are not essential to transfer function design, as shown by the two *RC* OP AMP designs.

Power requirements: The two *RC* OP AMP designs require external dc power supplies. The voltage divider cascade in Figure 11–36 requires less power since it uses only one OP AMP, compared with the two-OP-AMP inverting cascade. Thus, power requirements would favor the one-OP-AMP circuit over the two-OP-AMP circuit.

TABLE 11–1

Example	Figure	Description	Number of			
			R	*L*	*C*	OP AMP
11–20	11–36	*RC* voltage-divider cascade	4	0	2	1
11–21	11–40	*RC* inverting cascade	4	0	2	2
11–23	11–44	*RLC* voltage divider	2	1	1	0

Output loading: The output impedance of the design is important if the circuit must drive a finite load of, say, 1 kΩ. The resulting loading effects could defeat the basic purpose of the circuit by changing its transfer function. Output loading considerations favor the inverting cascade in Figure 11–40 because it has an OP AMP output that has zero output impedance.

A design problem involves more than simply finding a prototype that realizes a given transfer function. In general, the first step in a design problem involves determining an acceptable transfer function, one that meets performance requirements such as the characteristics of the step or frequency response. In other words, we must first design the transfer function and then design several circuits that realize the transfer function. To deal with transfer function design we must understand how performance characteristics are related to transfer functions. The next two chapters provide some background on this issue.

D E DESIGN AND EVALUATION EXAMPLE 11–24

Given the step response $g(t) = \pm[1 + 4e^{-500t}]u(t)$,

(a) Find the transfer function $T(s)$.
(b) Design two *RC* OP AMP circuits that realize the $T(s)$ found in part (a).
(c) Evaluate the two designs on the basis of element count, input impedance, output impedance.

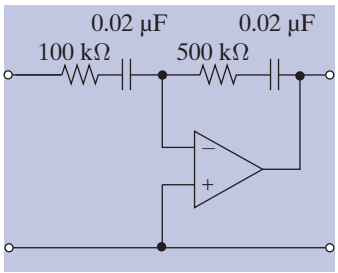
SOLUTION:

(a) The transform of the step response is

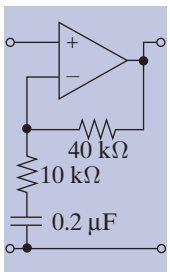
$$G(s) = \pm\mathcal{L}\{[1 + 4e^{-500t}]u(t)\} = \pm\left[\frac{1}{s} + \frac{4}{s + 500}\right] = \pm\frac{5s + 500}{s(s + 500)}$$

and the required transfer function is

$$T(s) = H(s) = sG(s) = \pm\frac{5s + 500}{s + 500}$$



C1



C2

FIGURE 11–46

(b) The first design uses an inverting OP AMP configuration. Using the minus sign on the transfer function $T(s)$ and factoring an s out of the numerator and denominator yield

$$T(s) = -\frac{5 + 500/s}{1 + 500/s} = -\frac{Z_2(s)}{Z_1(s)}$$

Equating numerators and denominators yields $Z_2(s) = 5 + 500/s$ and $Z_1(s) = 1 + 500/s$. The impedance $Z_2(s)$ is realizable as a resistance ($R_2 = 5\,\Omega$) in series with a capacitance ($C_2 = 1/500\,\text{F}$) and $Z_1(s)$ as a resistance ($R_1 = 1\,\Omega$) in series with a capacitance ($C_1 = 1/500\,\text{F}$). Using a magnitude scale factor $k_m = 10^5$ produces circuit C1 in Figure 11–46.

The second design uses a noninverting OP AMP configuration. Using the plus sign on the transfer function $T(s)$ and factoring an s out of the numerator and denominator yield

$$T(s) = \frac{5 + 500/s}{1 + 500/s} = \frac{Z_1(s) + Z_2(s)}{Z_1(s)}$$

Equating numerators and denominators yields

$$Z_1(s) = 1 + \frac{500}{s} \quad \text{and} \quad Z_2(s) = 5 + \frac{500}{s} - Z_1(s) = 4$$

The impedance $Z_1(s)$ is realizable as a resistance ($R_1 = 1\,\Omega$) in series with a capacitance ($C_1 = 1/500\,\text{F}$) and $Z_2(s)$ as a resistance ($R_2 = 4\,\Omega$). Using a scale factor of $k_m = 10^4$ produces circuit C2 in Figure 11–46.

(c) Circuit C1 uses one more capacitor than circuit C2. The OP AMP output on both circuits means that they each have almost zero output impedance. The input impedance to circuit C2 is very large, because its input is the noninverting input of the OP AMP. The input impedance of circuit C1 is $Z_1(s) = k_m(1 + 500/s)$; hence, the scale factor must be selected to avoid loading the source circuit. The final design for circuit C1 in Figure 11–46 uses $k_m = 10^5$, which means that $|Z_1| > 100\,\text{k}\Omega$, which should be high enough to avoid loading the source circuit. ■

E Evaluation Exercise 11–32

The following transfer function was realized in different ways in Figures 11–37, 11–41 and 11–45:

$$T_V(s) = \frac{\pm 10^6}{(s + 10^3)^2}$$

Compare the various designs in a table similar to Table 11–1. Which would you recommend if

(a) There was no power available?
(b) There was a desire not to invert the output and to avoid using inductors?
(c) There was a concern about loading at the output?

Answers:

(a) The *RLC* circuit in Figure 11–45 requires no power.
(b) The *RC* voltage-divider cascade in Figure 11–37 does not invert the output and does not require an inductor.
(c) None of the circuits prevents the possibility of loading at the output. One could add an OP AMP follower at the output of any of the three solutions to address loading concerns.

D DESIGN EXAMPLE 11–25

Verify that circuit C2 in Figure 11–46 meets its design requirements.

SOLUTION:

One of the important uses of computer-aided analysis is to verify that a proposed design meets the performance specifications. The circuit C2 in Figure 11–46 is designed to produce a specified step response

$$g(t) = \left[1 + 4e^{-500t}\right]u(t)\,\text{V}$$

This response jumps from zero to 5 V at $t = 0$ and then decays exponentially to 1 V at large t. The time constant of the exponential is $1/500 = 2$ ms, which means that the final value is effectively reached after about five time constants, or 10 ms.

One can use MATLAB to better visualize the specifications of a circuit design. To have MATLAB produce the step response, we use the transfer function operator, `tf`, as shown in the m-file below. In this example, after we entered the circuit's transfer function, we applied the MATLAB function `step` to plot the desired step response of the circuit in question.

```
syms s;
s = tf('s');
H = 5*(s+100)/(s+500);
step (H)
```

FIGURE 11–47

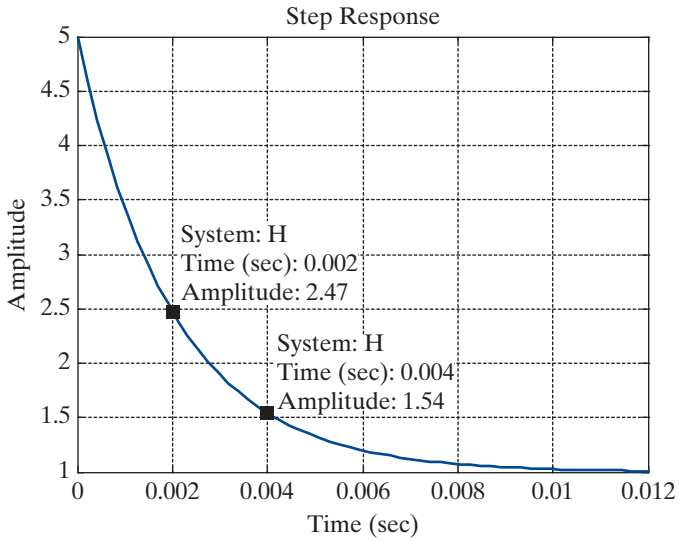


Figure 11–47 shows the step response of the circuit as plotted by MATLAB. We have selected two points for reference, namely $t = 2$ ms and $t = 4$ ms.

In Figure 11–48 we have drawn the circuit in OrCAD and stimulated it using the Time Domain (Transient) analysis function. The Probe response is also shown in the figure. We have used the Probe cursor to measure the same two points so that a comparison can be made.

The theoretical values can be also calculated directly from $g(t)$ at the same two points:

$$g(0.002) = 1 + 4e^{-500 \times 0.002} = 2.4715$$

$$g(0.004) = 1 + 4e^{-500 \times 0.004} = 1.5413$$

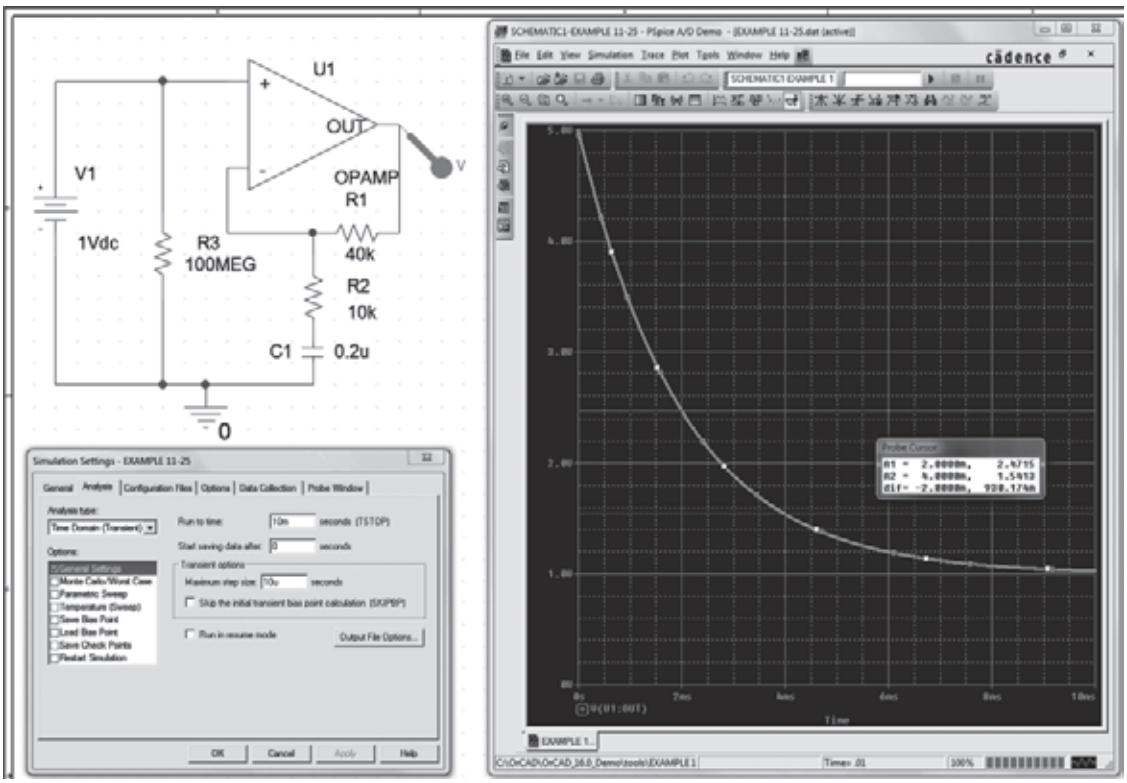


FIGURE 11–48 *Copyright © Cadence Design Systems, Inc. Used with permission.*

We summarize our results in the following table:

Technique / Time (s)	Hand Calculation	MATLAB	OrCAD
0.002	2.4715 V	2.47 V	2.4715 V
0.004	1.5413 V	1.54 V	1.5413 V

The data show that theory and simulation agree to three significant figures. ■

APPLICATION EXAMPLE 11–26

The operation of a digital system is coordinated and controlled by a periodic waveform called a clock. The *clock waveform* provides a standard timing reference to maintain synchronization between signal processing results that are generated asynchronously. Because of differences in digital circuit delays, there must be agreed-upon instants of time at which circuit outputs can be treated as valid inputs to other circuits.

Figure 11–49 shows a section of the clock distribution network in an integrated circuit. In this network the clock waveform is generated at one point and distributed to other on-chip locations by interconnections that can be modeled as lumped resistors and capacitors. Clock distribution problems arise when the *RC* circuit delays at different locations are not the same. This delay dispersion is called *clock skew*, defined as the time difference between a clock edge at one location and the corresponding edge at another location.

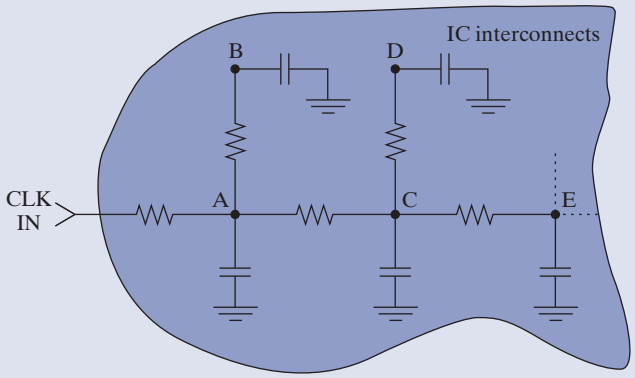


FIGURE 11–49 *Clock distribution network.*

To qualitatively calculate a clock skew, we will find the step responses in the *RC* circuit in Figure 11–50. The input $V_S(s)$ is a unit step function which simulates the leading edge of a clock pulse. The resulting step responses $V_A(s)$ and $V_B(s)$ represent the clock waveforms at points A and B in a clock distribution network. To find the step responses, we use the following *s*-domain node-voltage equations.

$$\text{Node A:} \quad \left(\frac{2}{R} + Cs\right) V_A(s) - \left(\frac{1}{R}\right) V_B(s) = \frac{V_S(s)}{R}$$

$$\text{Node B:} \quad -\left(\frac{1}{R}\right) V_A(s) + \left(\frac{1}{R} + Cs\right) V_B(s) = 0$$

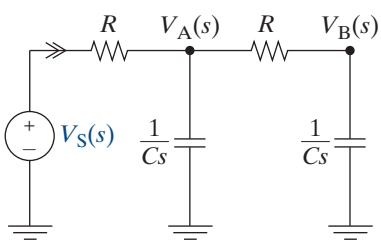


FIGURE 11–50 *Two-stage RC circuit model.*