Faculty of Engineering and Technology
Department of Electrical and Computer Engineering

ENCS5337 Chip Design Verification

Course Syllabus

Dr. Ayman Hroub

Course/Instructor Information	
Course Title	**Chip Design Verification**
Course Number	**ENCS5337**
Prerequisites	COMP2310 | Object-Oriented Programming ENCS3310 | Advanced Digital Systems Design
Semester	Spring Semester 2024/2025
Office Location	Masri515
Email	aahroub@birzeit.edu

Textbooks/References

- Chris Spear & Greg Tumbush, SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, 3rd edition, 2012, ISBN : 978-1-4614-0714-0
- Bruce Wile, John Goss and Wolfgang Roesner, Comprehensive Functional Verification, Elsevier, 2005, ISBN: 0-12-751803-7
- Janick Bergeron, Writing Testbenches: Functional Verification of HDL Models, Second Edition, Kluwer Academic Publishers, 2003, ISBN: 1-4020-7401-8
- Verification Academy
- Research papers from top conferences and journals
- Other handouts will be given by the instructor in due course

BZU Catalogue Course Description

VLSI chip design flow, design verification concepts, verification techniques and methodologies, hardware description and verification languages, hardware modeling and verification in SystemVerilog, constrained pseudo random stimuli generation, driving and checking, functional coverage, code coverage, assertion-based verification, building test-benches using Universal Verification Methodology (UVM), introduction to formal verification, EDA tools.

Learning Outcomes
At the end of this course, students are expected be able to: 1. Understand the VLSI chip design flow and the importance of design verification 2. Be familiar with the state of the art of hardware design verification techniques. 3. Be familiar with hardware design languages 4. Write a UVM (Universal Verification Methodology) testbench from scratch 5. Understand test generation, code coverage, functional coverage, and assertion based verification. 6. Get hands-on experience with EDA tools 7. Have hands-on experience on SystemVerilog and UVM

No.	Course Topics
1	Introduction to VLSI Chip Design and Design Verification
2	Verification Methods, Techniques, and EDA Tools
3	Driving and Checking
4	Verification Planning and Management
5	Hardware Design and Verification Languages
6	Introduction to SystemVerilog
7	Stimuli Generation
8	Constrained Pseudo-Random Stimuli Generation in SystemVerilog
9	Coverage in SystemVerilog
10	Assertion-based Verification
11	Universal Verification Methodology (UVM)

Grading Scheme	
Assessment Type	**Weight**
Project	20%
Midterm Exam	25%
Practical Exam	20%
Comprehensive Final Exam	35%
Total	**100%**

Teaching and Learning Methods
• Lectures, assignments, in-class activities, exams, assignments, and projects. • Modern learning methods, such as, inductive learning, flipped classroom, learning by project, etc.

Additional Notes	
Assignments	No late assignments
Makeup Exams	No makeup exam
Office Hours	Students are highly encouraged to utilize the instructor's office hours
Honor Code	Students are expected to abide by Birzeit University honor code on all aspects of their academic work. Please review that on Ritaj. Moreover, students are expected to follow the code of conduct for the course appended to this course outline.
Code of Conduct	By enrolling in this course, students agree to abide by a code of conduct that helps all participants gain the best results in a healthy and pleasant environment. This includes the following rules: • Mutual respect is a must • Students are expected to be in class on time • Cell phones should be switched off • Classroom should be very quiet • Students are expected to stay in the classroom focusing and quiet, and not leaving the class room without asking the instructor's permission