BIRZEIT UNIVERSITY

DEPARTMENT OF COMPUTER SYSTEM ENGINEERING

Digital Integrated Circuits - ENCS333

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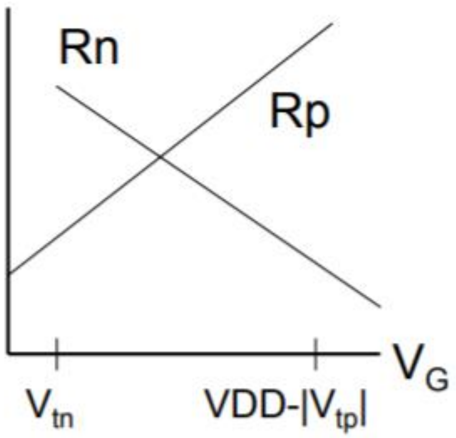
Lecture #5- Transistor_I_V_Curve and Mode of operations

Integrated-Circuit Devices and Modeling

Transistor Sizing

- Channel Resistance (from Chapter 3)
  "ON" resistance of transistors
  - $Rn = 1/(\mu_n Cox\ (W/L)\ (V_{GS}-Vtn)\ )$
  - $Rp = 1/(\mu_p Cox\ (W/L)\ (V_{SG}-|Vtp|)\ )$
    - $Cox = \varepsilon_{ox}/t_{ox}$ [F/cm²], process constant



- Channel Resistance Analysis
  - $R \propto 1/W$ (increasing W decreases R & increases Current)
  - R varies with Gate Voltage, see plot above
  - If Wn = Wp, then Rn < Rp
    - since $\mu_n > \mu_p$
    - assuming Vtn ~ |Vtp|
  - to match resistance, Rn = Rp
    - adjust Wn/Wp to balance for $\mu_n > \mu_p$

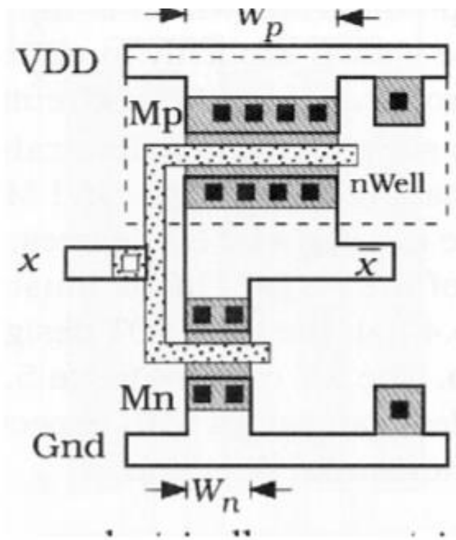
Transistor Sizing

- Channel Resistances
  - $Rn = 1/(\mu_n Cox\ (W/L)\ (V_G\text{-}Vtn)\ )$
  - $Rp = 1/(\mu_p Cox\ (W/L)\ (V_G\text{-}|Vtp|)\ )$
  - $\boxed{Rn/Rp = \mu_p/\mu_n}$
    - if $Vtn = |Vtp|$, $(W/L)_n = (W/L)_p$
- Matching Channel Resistance
  - there are performance advantage to setting Rn = Rp
    - discussed in Chapter 7
  - to set Rn = Rp
    - define mobility ratio, $\boxed{r = \mu_n/\mu_p}$
    - $\boxed{(W/L)_p = r\ (W/L)_n}$
      - pMOS must be larger than nMOS for same resistance/current
- Negative Impact
  - $\Rightarrow \boxed{C_{Gp} = r\ C_{Gn}}$ larger gate = higher capacitance

- See class notes we explained in class for sizing

Transistor Matching and Scaling

- Channel Resistance Matching
  - increase Wp so that Rn = Rp
  - pMOS larger than nMOS
  - pMOS current drive = nMOS current drive



- Scaling ratio, S
  - scaling W to increase current capabilities
  - typically in unit steps, 1x, 2x, 4x, etc.
  - generally L kept at minimum value