IC Notes for the Final Exam

Topics:

1. Key Concepts from First Hour Exam Material
2. Power
3. Combinational Logic Design (Static, Dynamic)
4. Sequential Logic Design
5. Interconnect
6. Layout and Timing

References:

1. Digital Integrated Circuits
2. CMOS VLSI Design

Prepared By: Ghazi Haj Qassem

Review

Nonideal IV effects

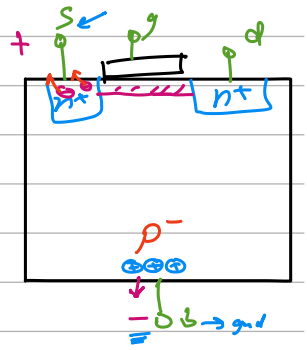
1. Body effect

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right) \quad \cdots (1)$$

(γ: body coeff., ϕ_s: surface potential)

$$\phi_s = 2 V_T \ln\frac{N_A}{n_i}, \quad \gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si} N_A} = \frac{\sqrt{2q\varepsilon_{si} N_A}}{C_{ox}}$$

($V_T = \frac{kT}{q}$, N_D, N_A)



→ For small values of V_{sb}, eqn. ① can be linearized to:

$$V_t = V_{t0} + K_y V_{sb} \quad \cdots (2) \qquad K_y = \frac{\gamma}{\sqrt{2\phi_s}}$$

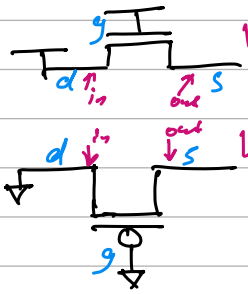
$V_{sb} = 0$

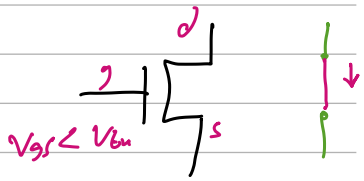
{ ① $V_{sb} \propto V_t$ ↑↑
② $N_A \propto V_t$

2. Subthreshold Leakage

$$\rightarrow I_{ds} = I_{ds0}\, e^{\frac{V_{gs} - V_{t0} + \eta V_{ds} - K_y V_{sb}}{nV_T}} \left(1 - e^{-\frac{V_{ds}}{V_T}}\right)$$

Pass Transistors

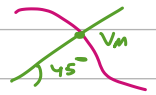




VTC

* For complementary CMOS inverter:

$V_{OH} = V_{DD}$, $V_{OL} = GND$, V_{iH}, V_{iL} are when $\frac{dV_{out}}{dV_{in}} = -1$, and V_M when $V_{in} = V_{out}$.

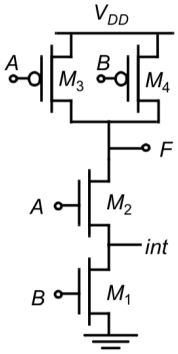


Example: Match the following transitions with their corresponding curve:

a) A=B=0→1

b) A=1, B=0→1

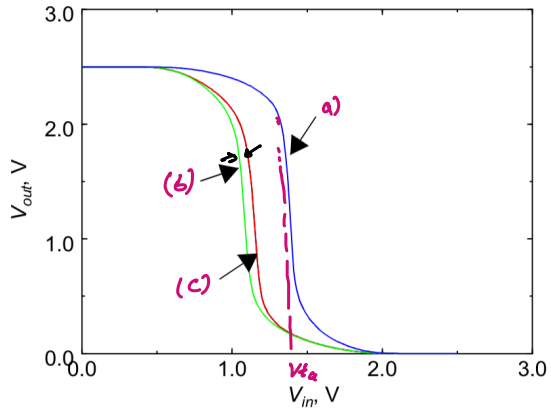
c) A=0→1, B=1



M_2: $V_t = V_{t0} + \gamma\left[\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right]$

M_1: $V_t = V_{t0} + \gamma\left[\sqrt{\phi_s + 0} - \sqrt{\phi_s}\right]$

$= V_{t0}$

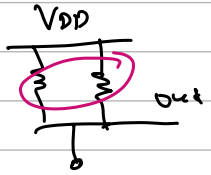


$F = \overline{A \cdot B}$

V_t ↓ M_2 on, M_1 off → on ⇒ A=1, B=0→1

V_t ↑ M_1 on, M_2 off → on ⇒ A=0→1, B=1

a)



PUN stronger PDN

Power

P

P_{static} — static current — current between supply rails (Vdd, gnd) — $P = iV$

$P_{dynamic}$ → $0 \to 1$ (switching)

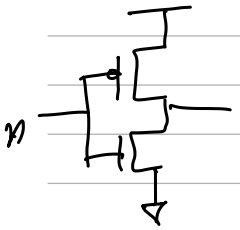
$P = \alpha_{0\to1} C_L V_{DD}^2 f$ → 3GHz

$= C_L V_{DD}^2 f_{0\to1}$ — as $\alpha \propto C \propto P_{dy}$

inputs uniformly distributed and uncorrelated

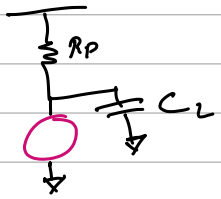
$\alpha_{0\to1} = P(0\to1) = P_0 P_1 = \frac{3}{4} \cdot \frac{1}{4} = \frac{3}{16}$

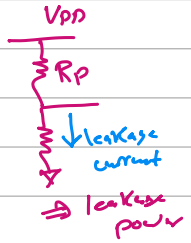
static CMOS



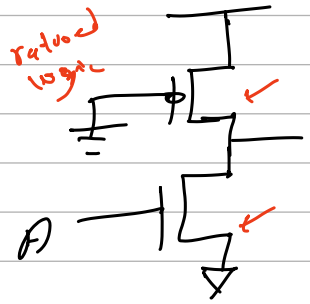
A=0

A=1





A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0



$\alpha = \frac{N_0}{2^N} \cdot \frac{N_1}{2^N} = \frac{N_0(2^N - N_0)}{2^N}$

Example: $\alpha_{0\to1}$ * n-input XOR gate

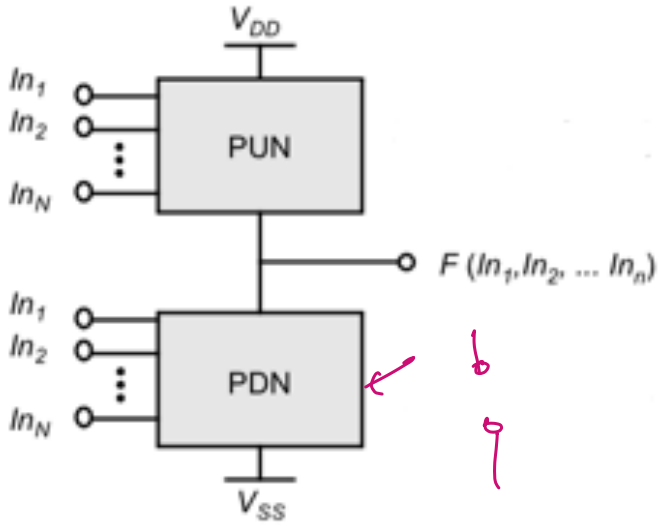
$\alpha = \frac{2^N/2}{2^N} \cdot \frac{2^N/2}{2^N} = \frac{1}{4}$

Combinational Logic Design

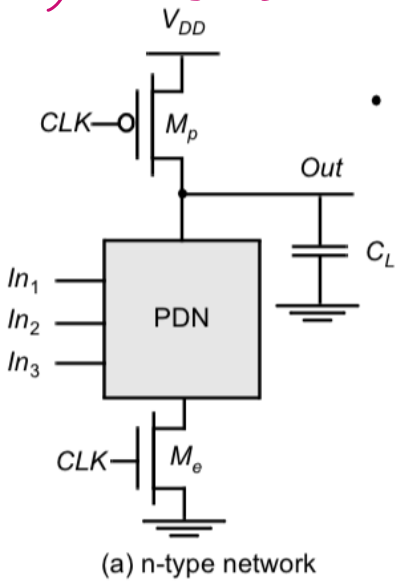
Dynamic Logic

→ static CMOS logic with a fan-in of N requires 2N devices

Complementary CMOS

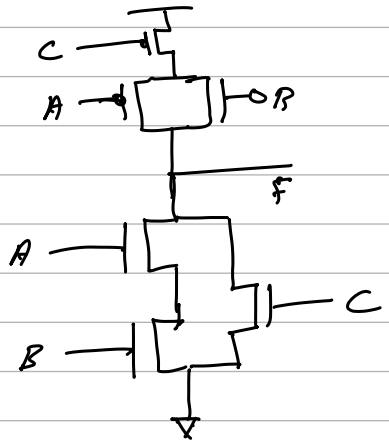


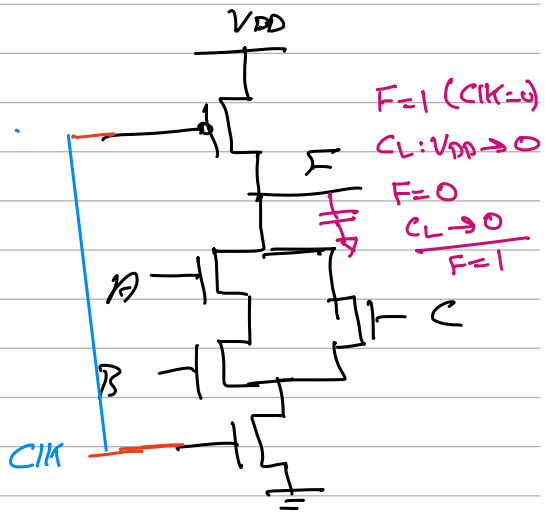
Dynamic CMOS



(a) n-type network

Example: Implement the logic function $F=\overline{AB+C}$ using complementary CMOS and dynamic CMOS





Dynamic Logic Phases:

CLK = 0 → CLK = 1 (Eval.)

C_L (V_{DD}) C_L(V_{DD}) iff F=1

C_L(V_{DD}→0) iff F=0→F=1

① Precharge [CLK = 0]

→ M_p on ⇒ Out charged to V_{DD}.

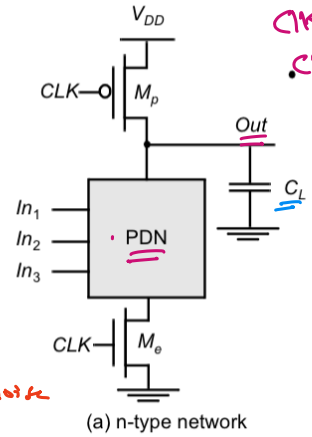
→ M_e off ⇒ no static current flows from V_{DD} to GND (no static power during precharge)

② Evaluation

→ M_e on ⇒ Out conditionally discharged.

PDN conducts: Out discharged to GND

PDN off: Precharged value is stored on C_L



(a) n-type network

CLK=0 (precharge)

CLK=1 (Eval.)

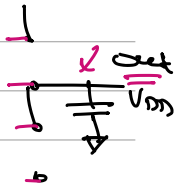
$C_L = V_{DD}$

F=0→F=1

N.B. ① Once Out is discharged, it cannot be charged until the next precharge phase. [one transition per E.P.]

② PDN off ⇒ Out in high impedance state. → susceptible to noise, crosstalk

↳ Unlike complementary CMOS, where Out is in a low impedance state.



Complementary CMOS (Static) vs Dynamic CMOS

	Static CMOS	Dynamic CMOS
transistor count	2N	N+2
switching speed	slower	faster
power dissipation	typically less	typically higher
VTC parameters	$V_{OH} = V_{DD}$, $V_{OL} = GND$; V_{IL}, V_{IH}, V_M circuit dependent	$V_{OH} = V_{DD}$, $V_{OL} = GND$; $V_{IL} = V_{IH} = V_M = V_{tn}$ → $V_{DD}/2$

① $t_{pLH} = 0$

② C_L τ = RC

(high) $NM_H = V_{DD} - V_{tn}$

$NM_L = V_{tn}$ (low)

robust

$P_{dynamic} = \alpha C V^2 f$

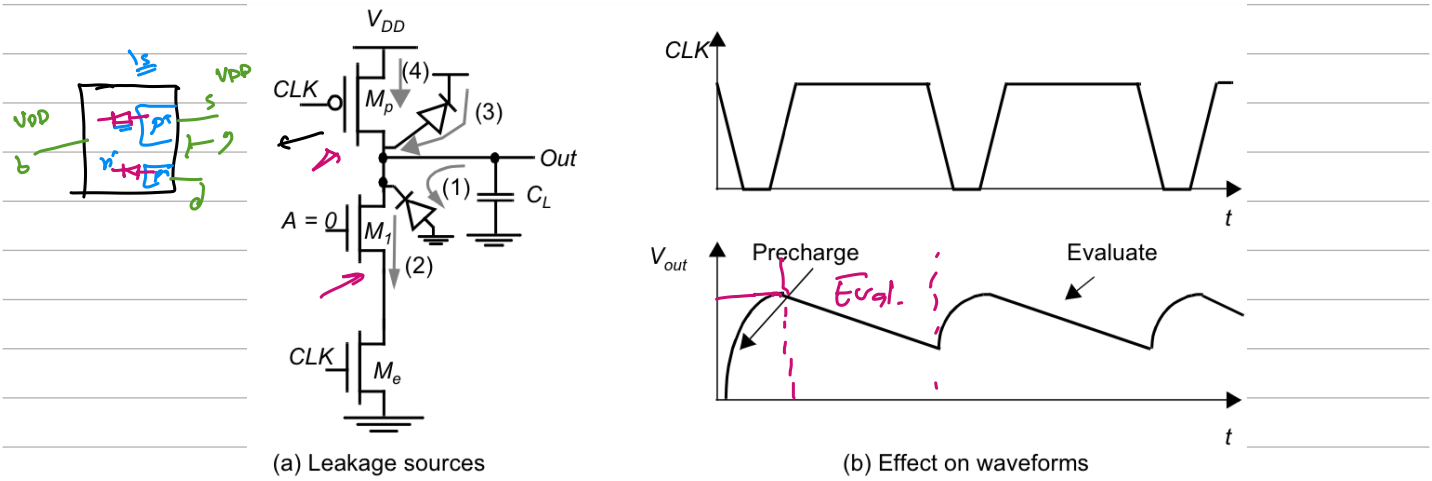
$\alpha = P_0$

V_{tn} — NML

Issues in Dynamic Design

[2] Backgate coupling [4] Clock-feedthrough

[1] Charge Leakage

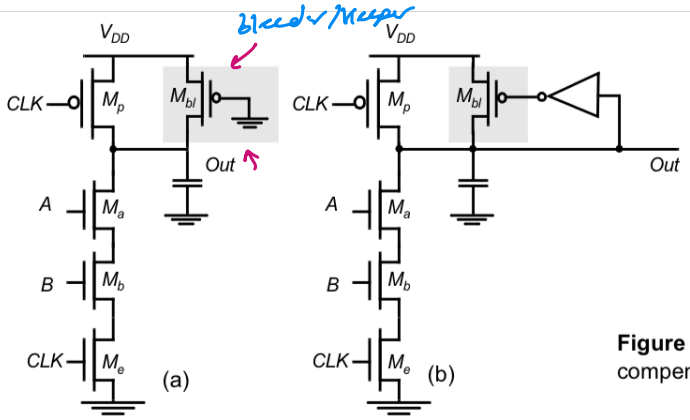


(a) Leakage sources (b) Effect on waveforms

Figure 6.56 Leakage issues in dynamic circuits.

* Leakage is caused by the high impedance state of the output node during evaluation, when PUN is off.

Solution: Reducing the output impedance of the output node during evaluation (add a bleeder transistor)



(b) is better since it eliminates the static power dissipation

Figure 6.58 Static bleeders compensates for the charge-leakage.

2 Charge Sharing

→ Initial conditions: $V_{out}(t=0) = V_{DD}$ and $V_X(t=0) = 0$

→ Two possible scenarios: $[\Delta V_{out} = V_{out}(t) - V_{out}(t=0) = V_{out}(t) - V_{DD}]$

① $\Delta V_{out} < V_{Tn}$:

$$Q_L(t=0) + Q_a(t=0) = Q_L(t) + Q_a(t) \qquad Q = CV$$

$$C_L V_{DD} = C_L V_{out}(t) + C_a[V_{DD} - V_{Tn}(V_X)]$$

$$C_L(V_{DD} - V_{out}(t)) = C_a[V_{DD} - V_{Tn}(V_X)]$$

$$\Delta V_{out} = -\frac{C_a}{C_L}[V_{DD} - V_{Tn}(V_X)]$$

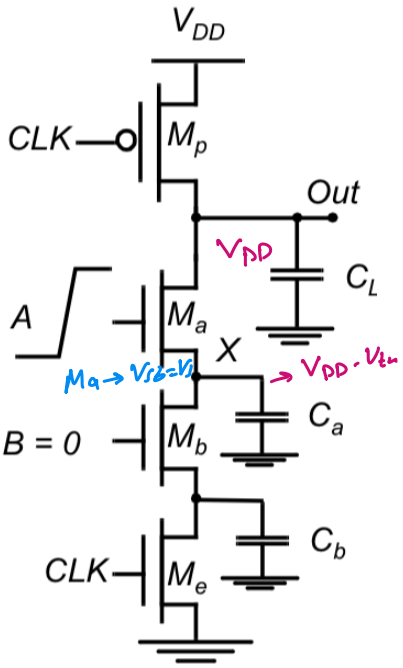
② $\Delta V_{out} > V_{Tn}$: [worst-case]

$$C_L V_{DD} = C_L V_{out}(t) + C_a \cdot \frac{C_L}{C_a + C_L} V_{DD}$$

$$V_{out}(t) - V_{DD} = \frac{-C_a}{C_a + C_L} V_{DD}$$

$$\boxed{\Delta V_{out} = -\frac{C_a}{C_a + C_L} V_{DD}} \qquad V_{out}(\infty) = \frac{C_L}{C_a + C_L} V_{DD}$$

↳ $V_{out}(t) - V_{DD} = -\frac{C_a V_{DD}}{C_a + C_L} = \frac{(C_a + C_L)V_{DD} - C_a V_{DD}}{C_a + C_L}$



Solution:

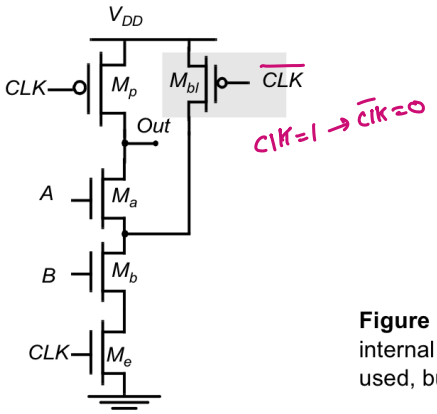


Figure 6.61 Dealing with charge-sharing by precharging internal nodes. An NMOS precharge transistor may also be used, but this requires an inverted clock.

Example: For the following circuit:

a) What is the logic function corresponding to this circuit.

b) What is the worst-case voltage drop at the output node (due to charge sharing)

c) What should be the switching threshold of the load inverter so that the circuit functions correctly.

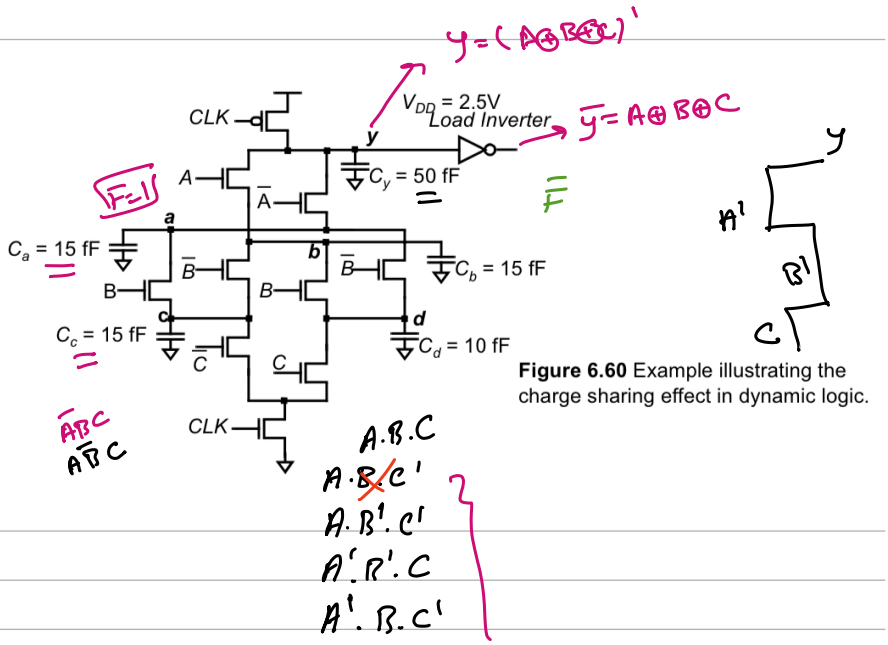


Figure 6.60 Example illustrating the charge sharing effect in dynamic logic.

b) $C_X = 15fF + 15fF$

$$\Delta V_o = \frac{-C_a}{C_a + C_L} V_{DD} = -\frac{7}{80}(2.5) = -0.94\ V$$

c) $V_{DD} + \Delta V_{out} = 2.5 - 0.94 = 1.56\ V$

A	B	C	out	
0	0	0	1	← 25fF
0	0	1	0	
0	1	0	0	
0	1	1	1	← 30fF
1	0	0	0	← 30fF
1	0	1	1	
1	1	0	1	← 25fF
1	1	1	0	note! ←

Sequential Logic Design

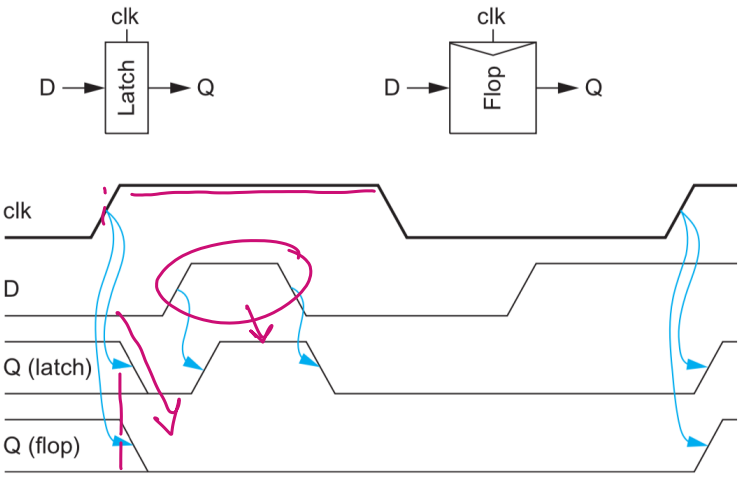
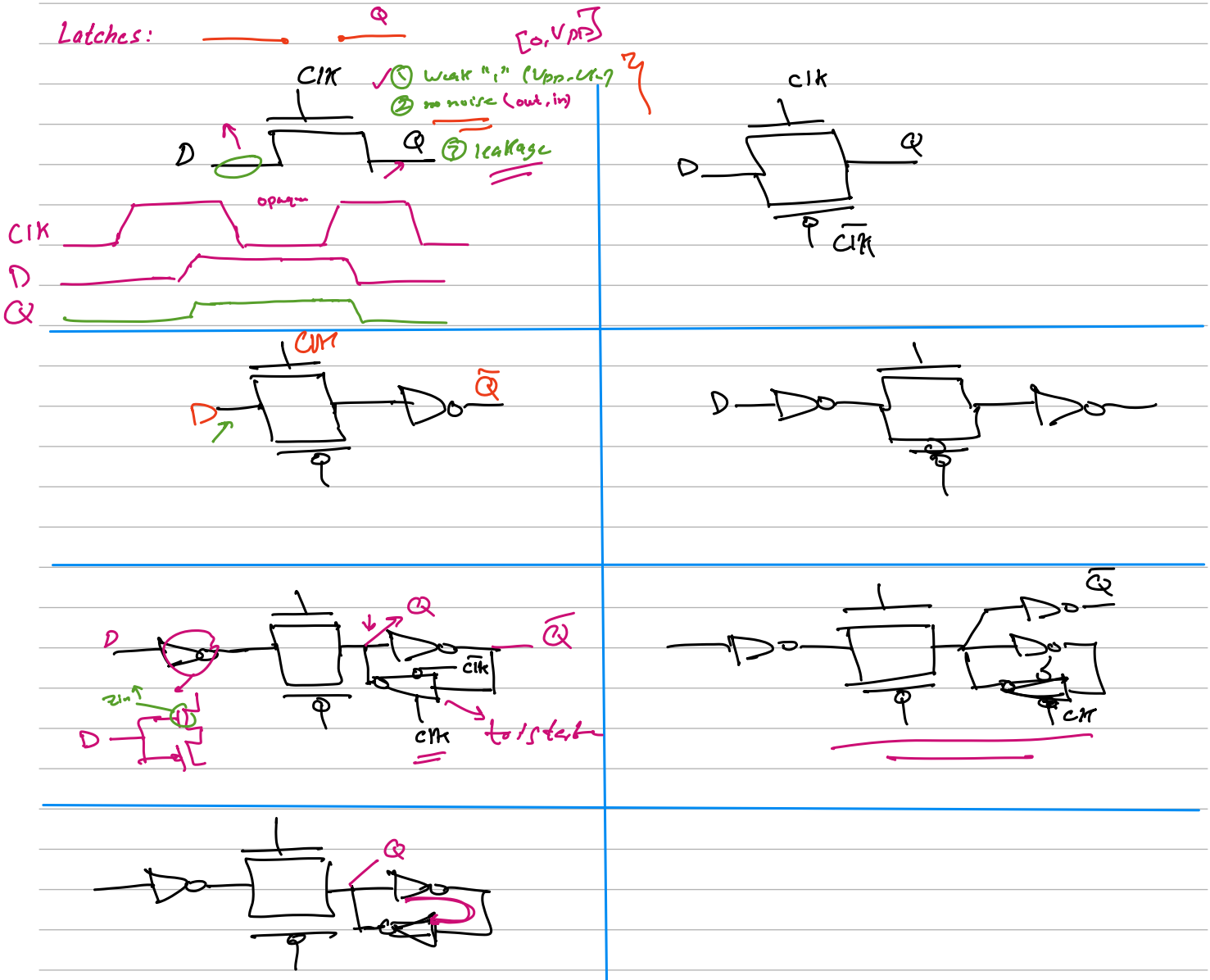


FIGURE 10.1 Latches and flip-flops

Latches:



Sequencing Element Timing Notation

TABLE 10.1 Sequencing element timing notation

Term	Name
t_{pd}	Logic Propagation Delay
t_{cd}	Logic Contamination Delay
t_{pcq}	Latch/Flop Clock-to-Q Propagation Delay
t_{ccq}	Latch/Flop Clock-to-Q Contamination Delay
t_{pdq}	Latch D-to-Q Propagation Delay
t_{cdq}	Latch D-to-Q Contamination Delay
t_{setup}	Latch/Flop Setup Time
t_{hold}	Latch/Flop Hold Time

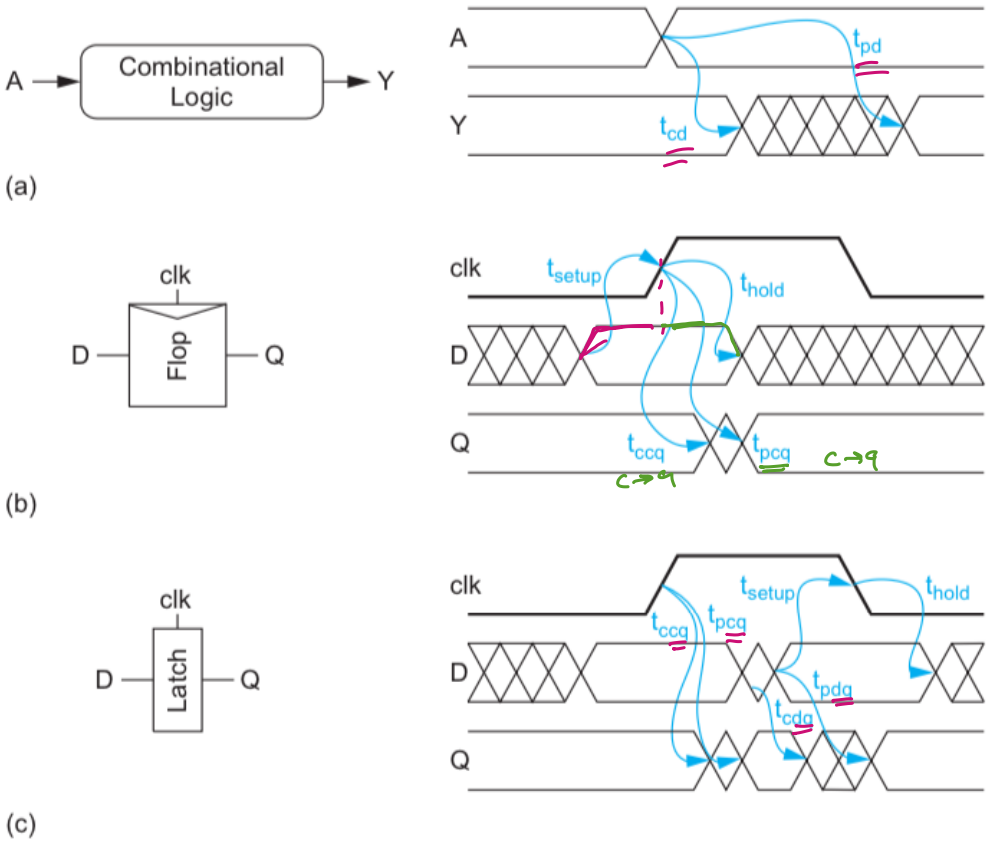


FIGURE 10.4 Timing diagrams

Max-Delay Constraints

$$T_c \geq t_{pcq} + t_{pd} + t_{setup} + t_{skew}$$

$$t_{pd} \leq T_c - (t_{pcq} + t_{setup} + t_{skew})$$

sequencing overhead

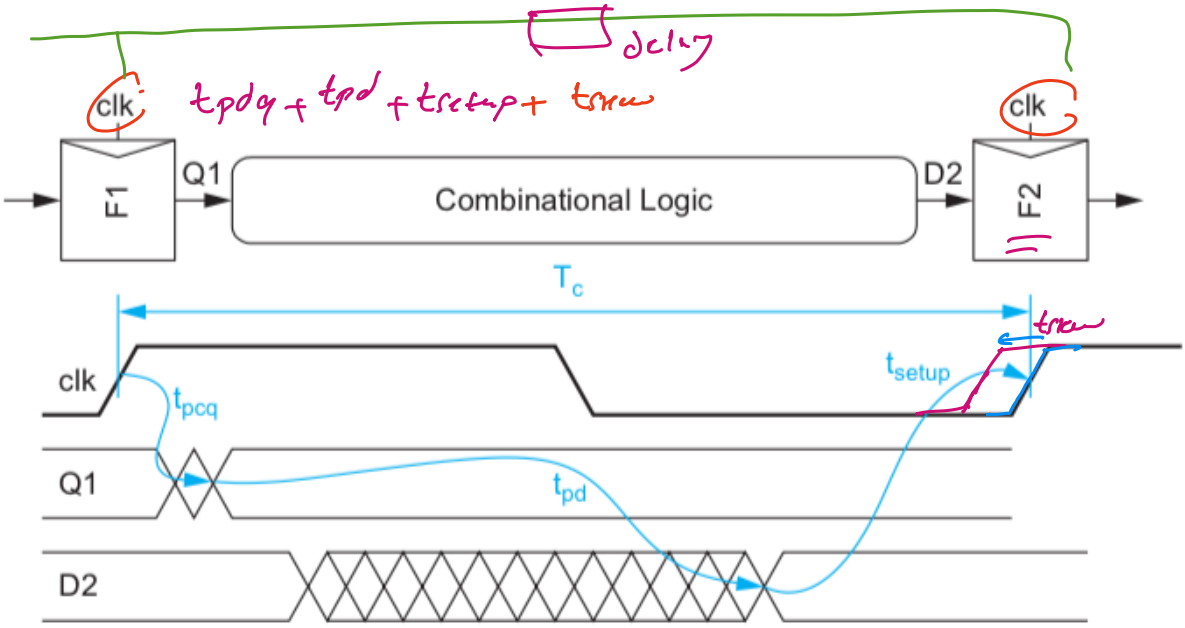


FIGURE 10.5 Flip-flop max-delay constraint

Min-Delay Constraints

$$t_{cd} \geq t_{hold} + t_{skew} - t_{ccq}$$

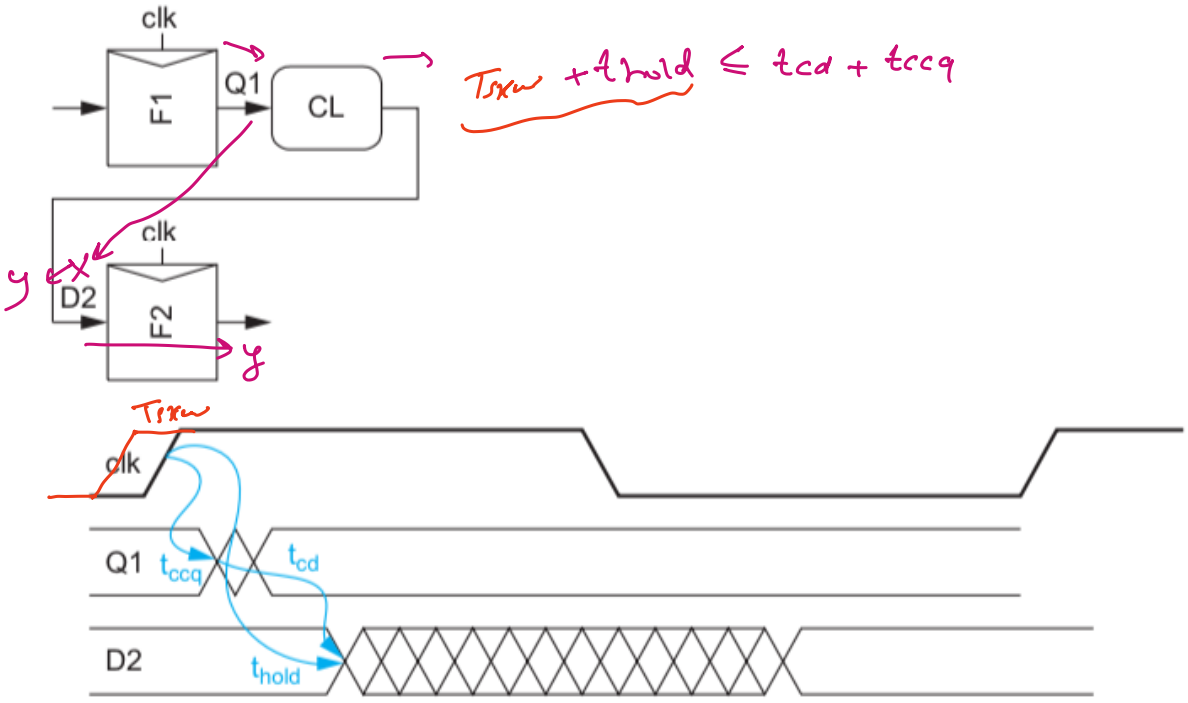


FIGURE 10.9 Flip-flop latch min-delay constraint

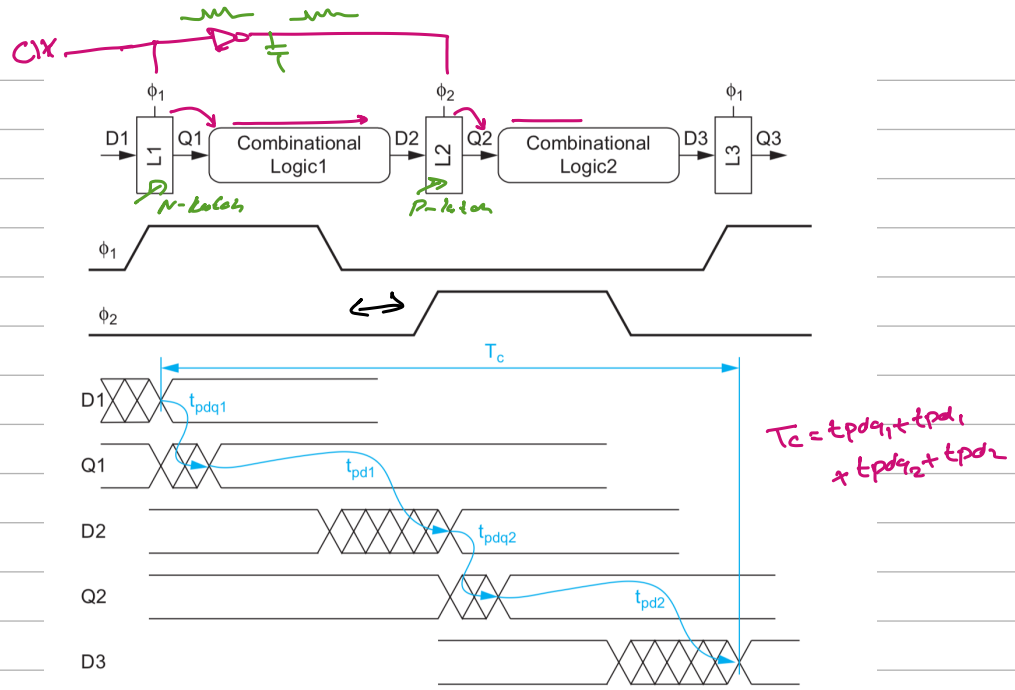


FIGURE 10.7 Two-phase latch max-delay constraint

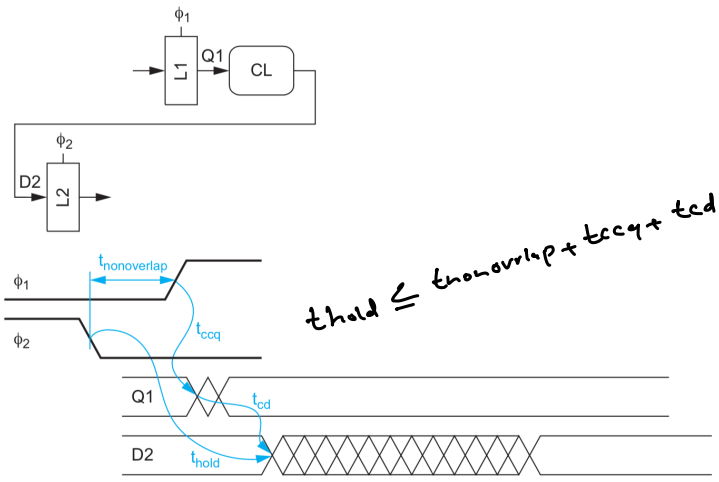


FIGURE 10.10 Two-phase latch min-delay constraint

Time Borrowing

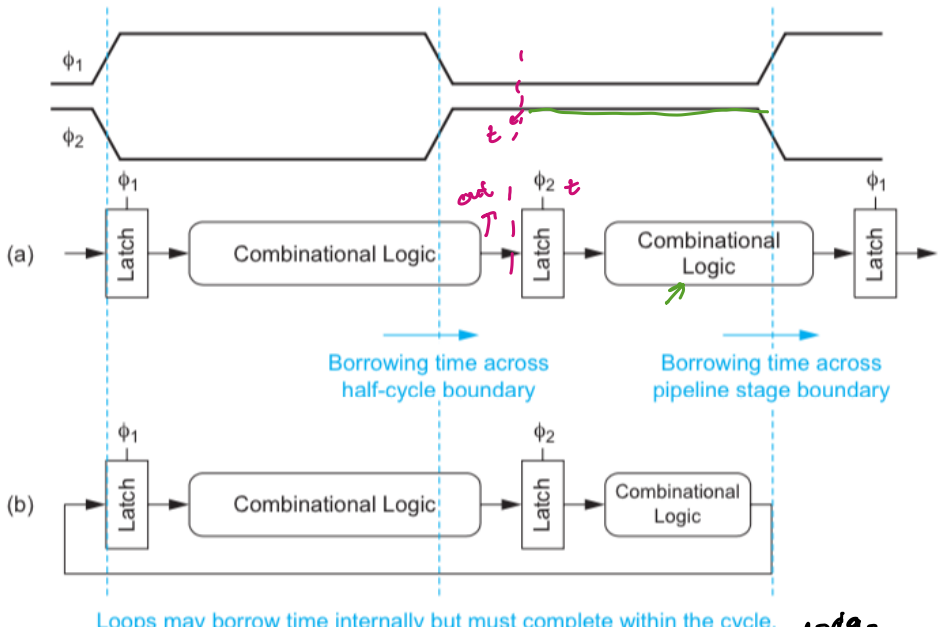


FIGURE 10.12 Time borrowing

$T_{borrow} = \frac{T_c}{2} - t_{pd_2} - t_{pdq_2}$

Example: Assume rise/fall times are zero.

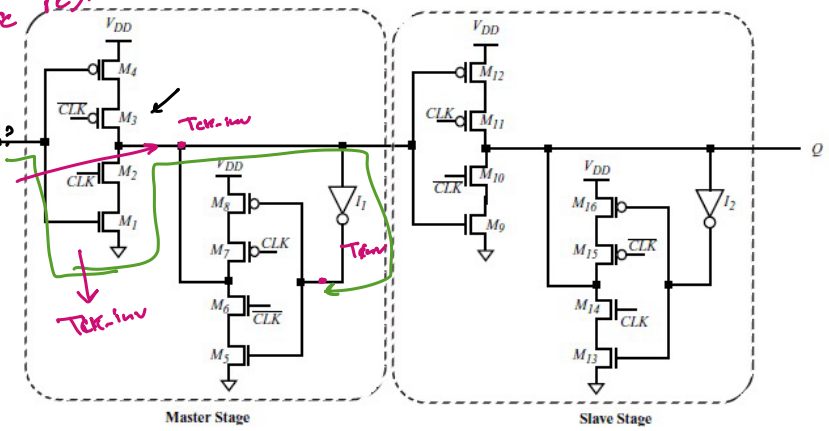
a) What kind of register is this? Neg-edge static register

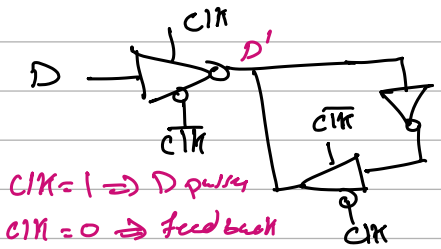
b) Assume prop delay of each clocked inverter is T_{ck_inv}, and I_1, I_2 is T_{inv}. Derive the expression for t_{su}, t_{cq}, t_h?

$T_{su} = T_{ck\_inv} + T_{inv}$

$T_{cq} = T_{ck\_inv}$

$T_h = 0$





W- latch

Example: $t_{su} = 62$ ps, $t_h = -10$ ps, $t_{pcq} = 90$ ps, $t_{ccq} = 75$ ps

① Minimum cycle time T_c.

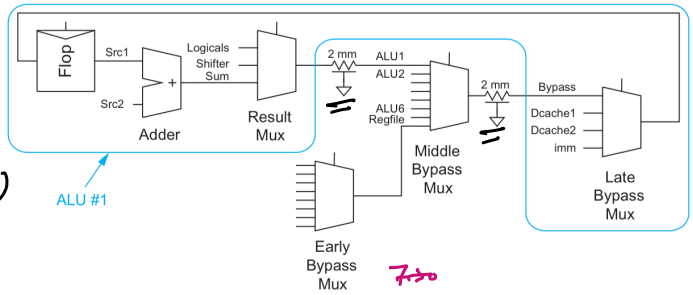
② Will the path with the least delay fail?

③ Assume latches are used instead of flip flops as in fig. (2). ($t_{su} = 40$ps, $t_h = 5$ps, $t_{ccq} = 52$ps, $t_{pcq} = 82$ps, $t_{pdq} = 82$ps)

a) Compute minimum cycle time T_c?

b) How much time is borrowed at $CT = T_c$?

c) If $T_c = 2000$ps, how much time is borrowed?



(b)

FIGURE 10.6 Itanium 2 ALU self-bypass path ((a) © IEEE 2002.)

① $T_c = t_{pcq} + t_{pd} + T_{setup} + T_{wire}$

$= 90ps + 100 + 62ps + 0 = 1152$ ps

② $t_{hold} \leq t_{ccq} + t_{cd} \Rightarrow$ no failure

$-10 \leq 75 + 45 = 120$ ps

③ a) $T_c = t_{pcq_1} + t_{pd_1} + t_{pcq_2} + t_{pd_2}$, $t_{pdq} \rightarrow \max(t_{pdq_1}, t_{pcq_1})$

$= 82ps + 590ps + 82ps + 410$

$= 1164$ ps

b) $T_{borrow} = t_{pcq_1} + t_{pd_1} - \frac{T_c}{2}$

$= 82 + 590 - 582 = 90$ ps

c) $872 < \frac{T_c}{2} = 1000$ps → no time is borrowed

$t_{pd} = 590ps + 60ps + 80ps + 70ps + 2 \times 100ps$

TABLE 10.2 Combinational logic delays

Element	Propagation Delay	Contamination Delay
Adder	590 ps	100 ps
Result Mux	60 ps	35 ps
Early Bypass Mux	110 ps	95 ps
Middle Bypass Mux	80 ps	55 ps
Late Bypass Mux	70 ps	45 ps
2-mm Wire	100 ps	65 ps

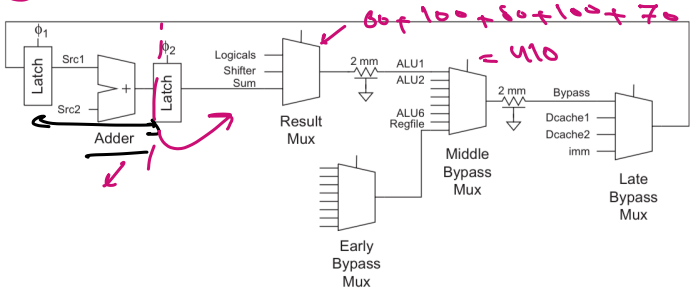


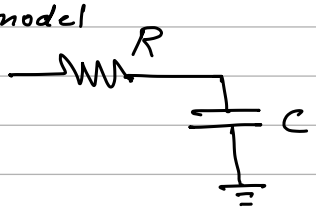
FIGURE 10.14 ALU self-bypass path with two-phase latches

Interconnect

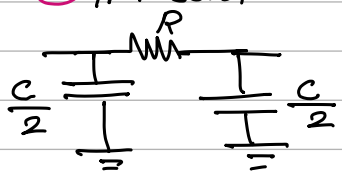
Interconnect Modelling

lumped approximations:

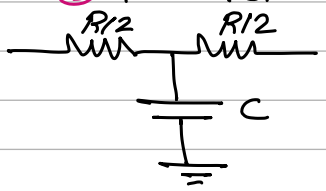
① L-model



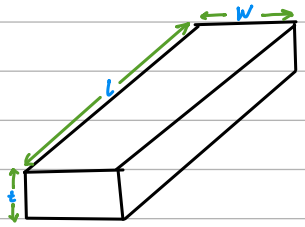
② π-model



③ T-model



Wire Resistance



$$R = \frac{\rho L}{A} = \frac{\rho L}{t W} = R_{\square} \frac{L}{W}$$

($R_{\square}$: sheet resistance ($\Omega/\square$))

Example: Compute the sheet resistance of a 0.22 μm thick Cu wire in a 65 nm process. Find the total resistance if the wire 0.125 μm wide and 1 mm long.

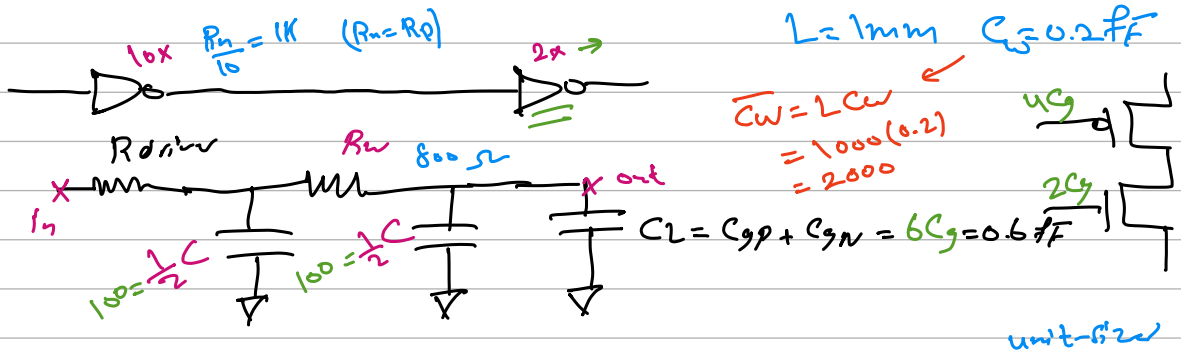
($t = 0.22\mu m$, $\rho = 2.2 \times 10^{-8}$)

Solution:

$$R_{\square} = \frac{\rho}{t} = \frac{2.2 \times 10^{-8}}{2.2 \times 10^{-7}} = 0.1\ \Omega/\square \qquad R = R_{\square} \frac{L}{W} = 0.1 \times \frac{1000}{0.125} = 800\ \Omega$$

Example: A 10x unit-sized inverter drives a 2x inverter at the end of the 1mm wire from the previous example. Suppose wire capacitance is 0.2 fF/μm and that a unit-sized nMOS transistor has $R = 10\ k\Omega$ and $C = 0.1$ fF. Estimate the propagation delay using Elmore delay model, ignoring diffusion capacitance

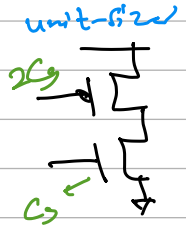
Solution:



$$\tau = R_{driver}\left(\frac{1}{2}C_w\right) + (R_{driver} + R_w)\left(\frac{1}{2}C_w + C_L\right)$$

(100, 0.6)

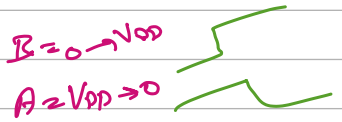
$$= 1000 \times 100\ fF + (1000 + 80\Omega)(0.7\ fF) \approx \ldots$$

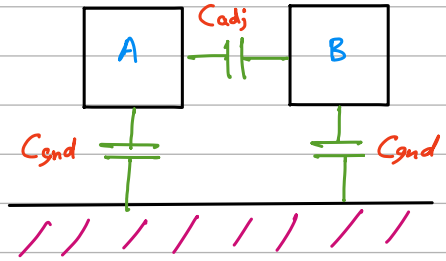


Crosstalk

① Crosstalk Delay Effects

B	ΔV	Ceff (A)
Constant	V_{DD}	$C_{gnd}+C_{adj}$
Switching in the same direction as A	0	C_{gnd}
Switching opposite to A	$2V_{DD}$	$C_{gnd}+2C_{adj}$

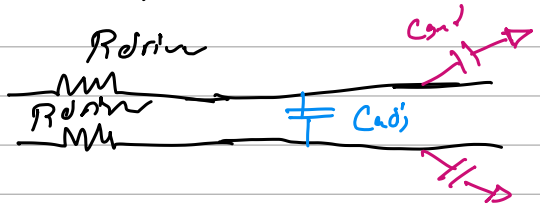




C_{gnd} (fF/μm)

Example: Each wire in a pair of 1mm lines has capacitance 0.08 fF/μm to ground and 0.12 fF/μm to its neighbour (C_{adj} (fF/μm)). Each line is driven by an inverter with 1kΩ effective resistance. Estimate the contamination and propagation delays of the path. Neglect parasitic capacitance of the inverter and resistance of the wires.

Solution:



Contamination: min. delay

propagation: max. delay

$C_{adj} = 1mm(0.12fF)$

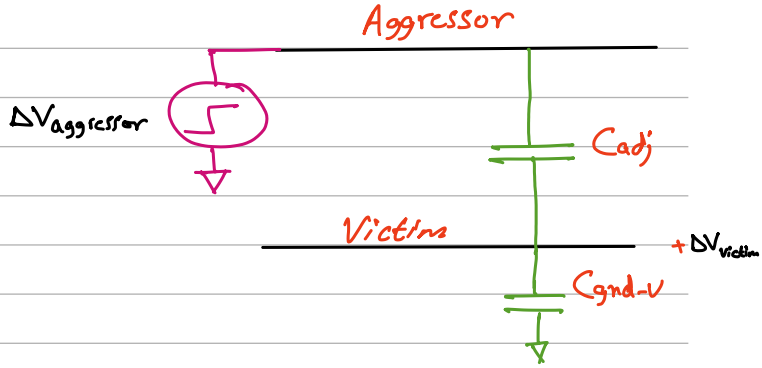
$C_{gnd} = 1mm(0.08fF)$

$t_c = R_{driver}.[C_{gnd}]$ $\quad t_p = R_{driver}[2C_{adj}+C_{gnd}]$

② Crosstalk Noise Effects

a. Floating Victim (high impedance)

$$\Delta V_{victim} = \frac{C_{adj}}{C_{gnd-v}+C_{adj}} \Delta V_{aggressor}$$



b. driven Victim

$$\Delta V_{victim} = \frac{C_{adj}}{C_{gnd-v}+C_{adj}} \frac{1}{1+K} \Delta V_{aggressor}$$

$$K = \frac{\tau_{aggressor}}{\tau_{victim}} = \frac{R_{aggressor}(C_{gnd-a}+C_{adj})}{R_{victim}(C_{gnd-v}+C_{adj})}$$