



DEPARTMENT OF COMPUTER SYSTEM ENGINEERING

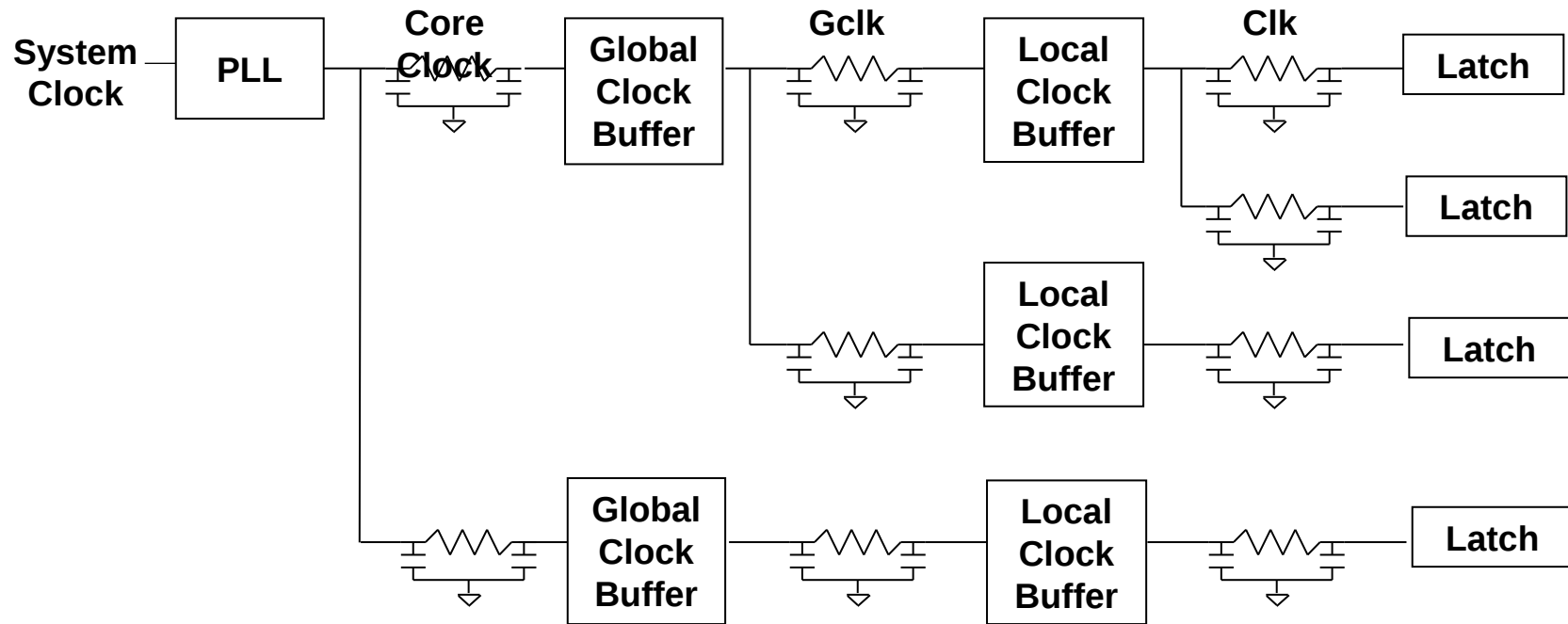
Digital Integrated Circuits - ENCS333

Dr. Khader Mohammad

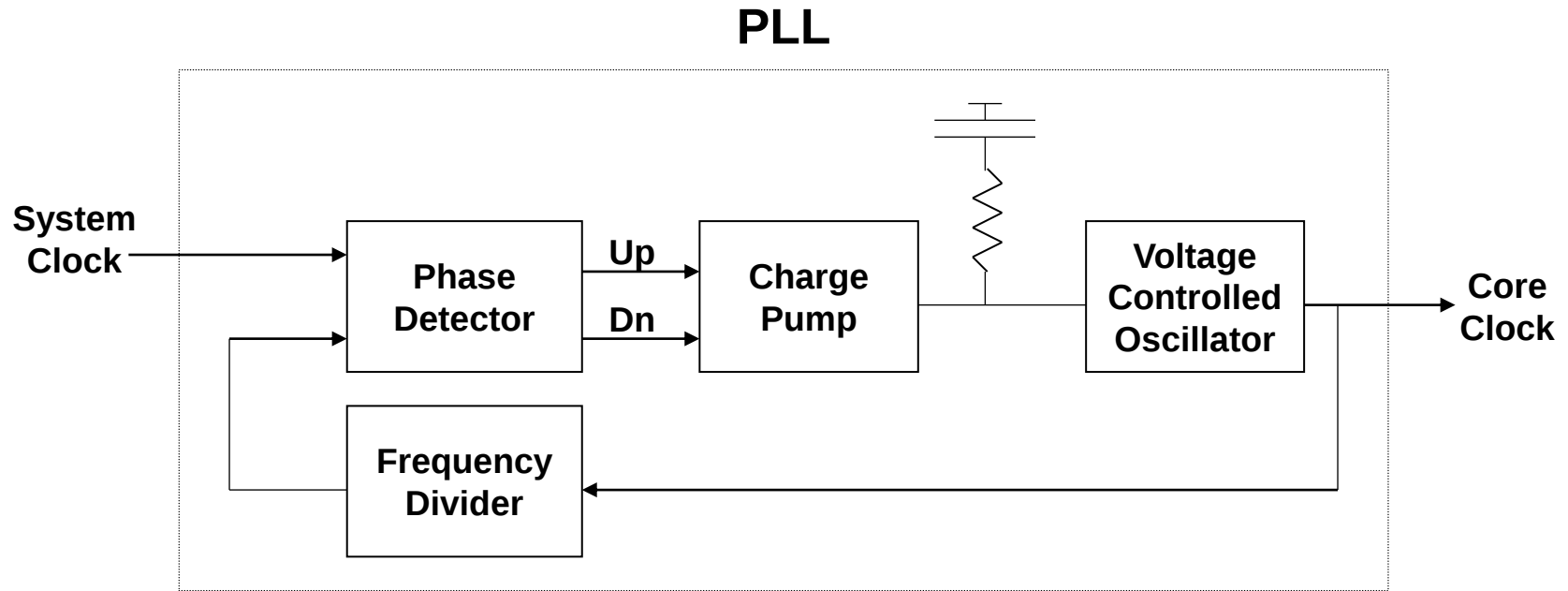
Lecture #11 clock-wire-interconnect

Integrated-Circuit Devices and Modeling

Clock Distribution Tree



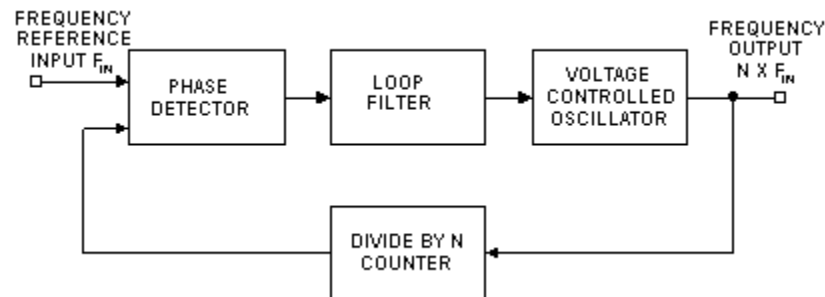
Phase Locked Loop (PLL)



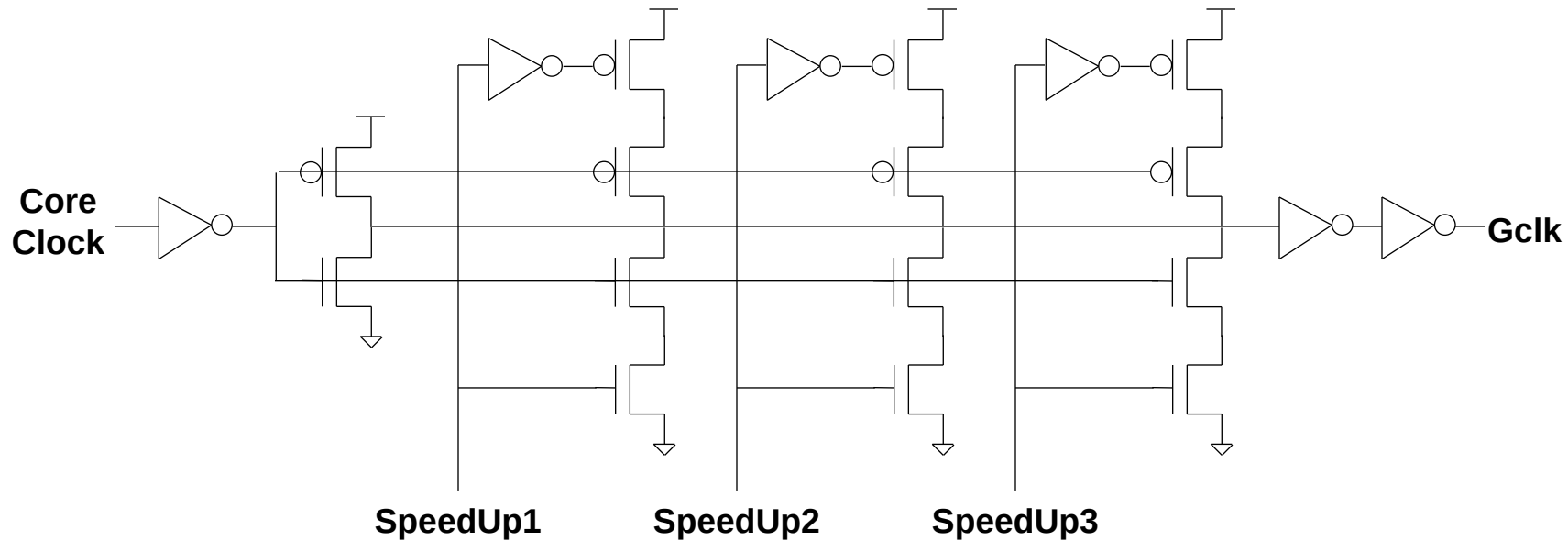
- PLLs produce an on-chip core clock at a multiple of the off-chip system clock.

PLL Overview

- PLLs
 - Typically there are two PLLs on a chip
 - IOPLL and COREPLL
 - IOPLL gets an external “xxbclk” and generates the address clock (2x) and data clock (4x)
 - These clocks are only used in the PADs
 - COREPLL takes the IOPLL output as reference and generates the core clock for entire chip

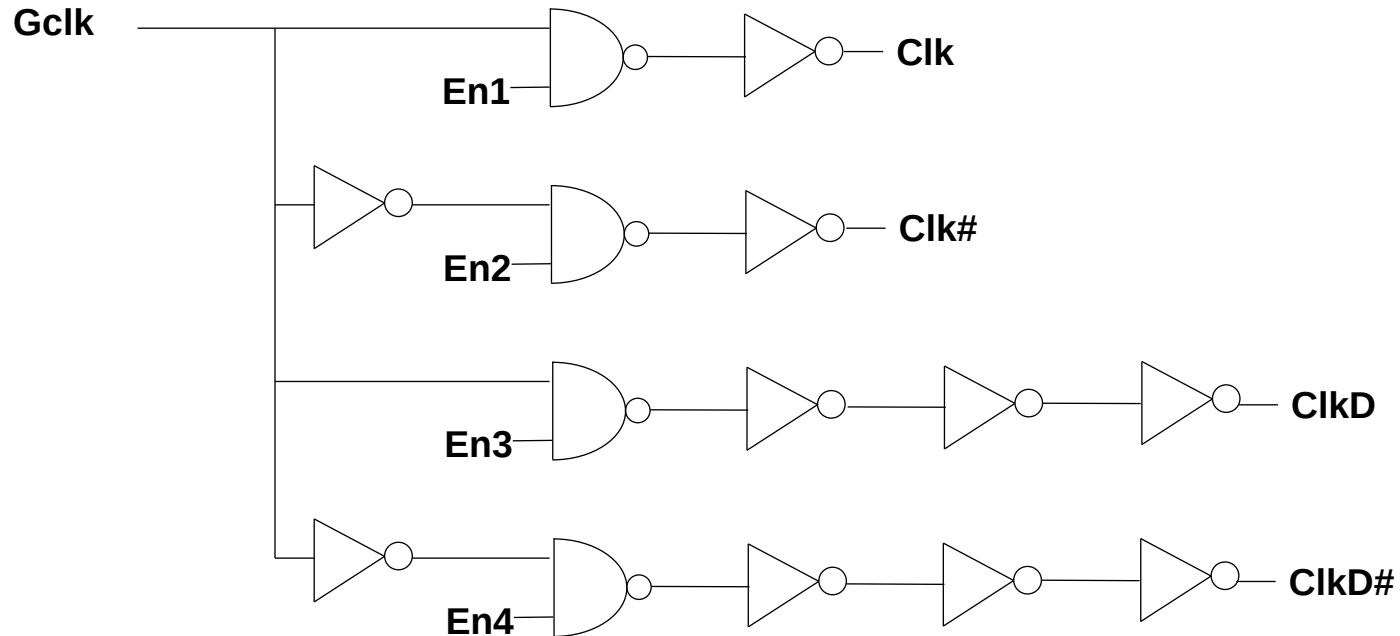


Global Clock Buffer



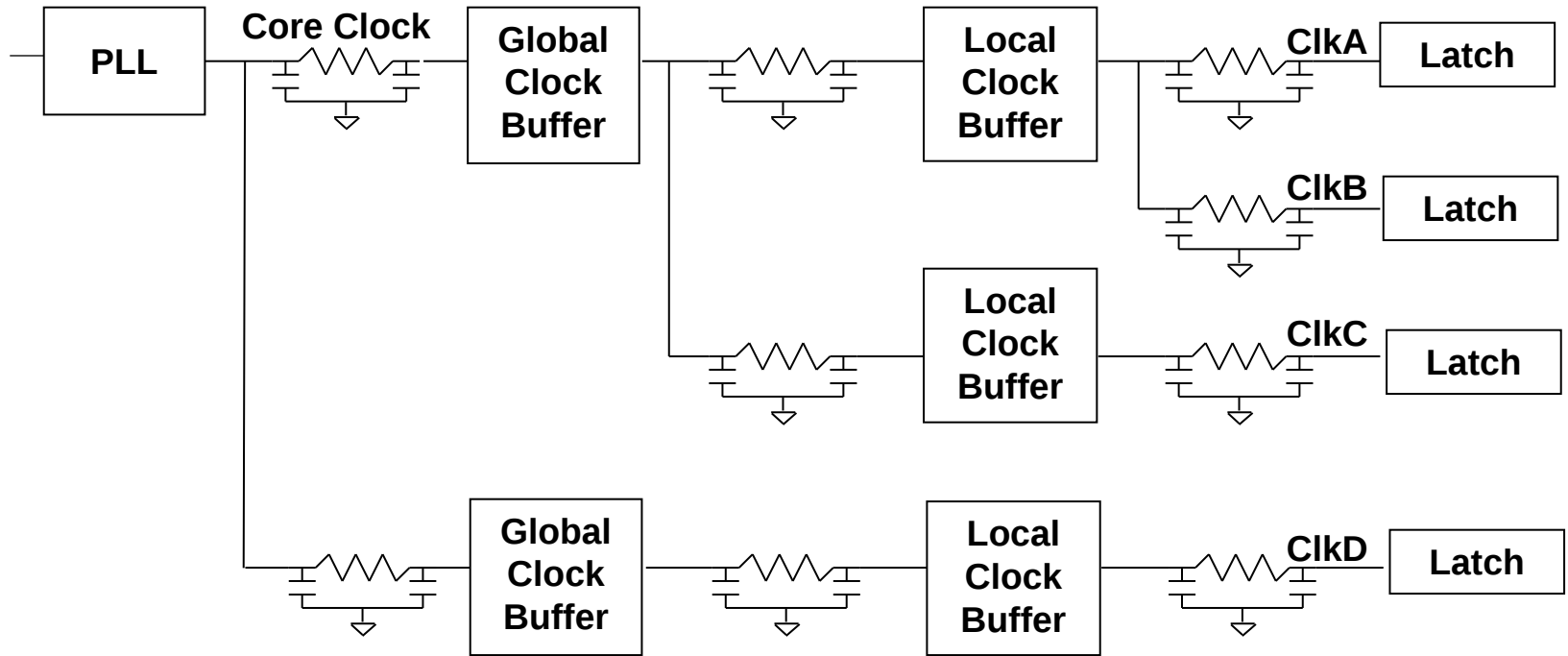
- Global clock buffers can use variable delay to compensate for RC mismatches across a die

Local Clock Buffers (LCBs)

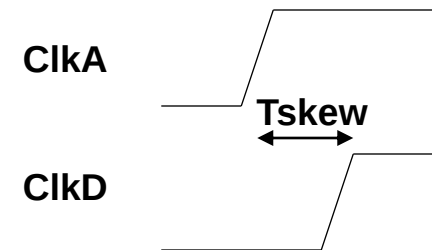


- Local Clock Buffers Support:
 - Clock gating for power reduction
 - Intentional clock skew insertion for timing optimization

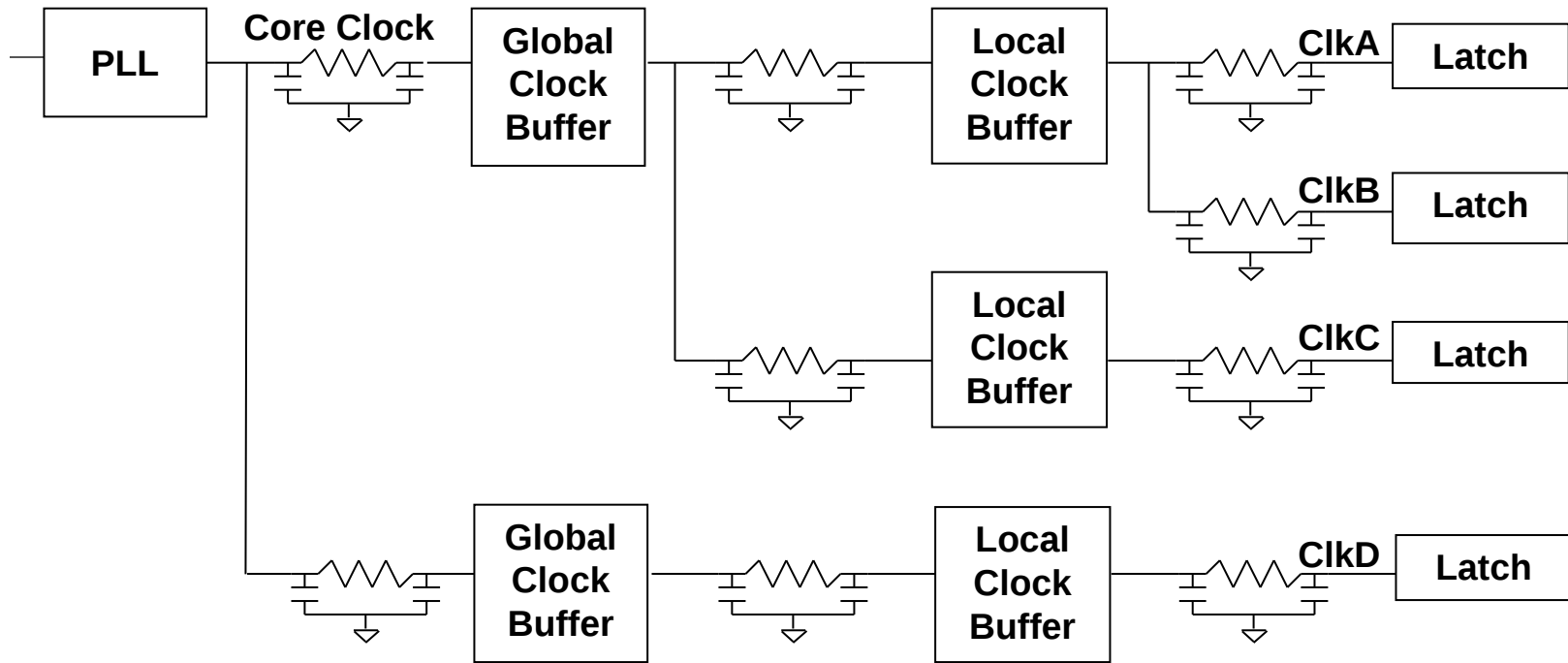
Clock Skew



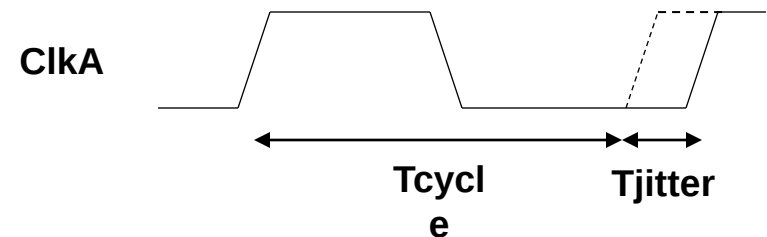
- A single transition of the core clock does not arrive at all sequentials at the same time.



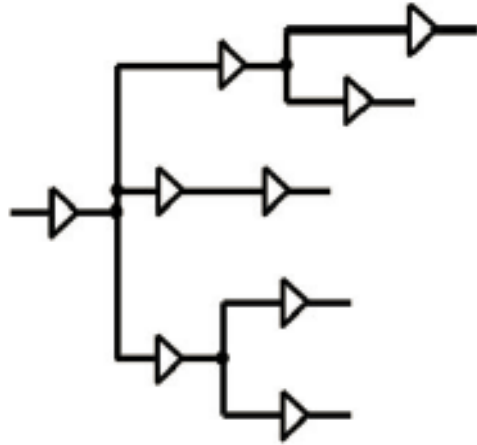
Clock Jitter



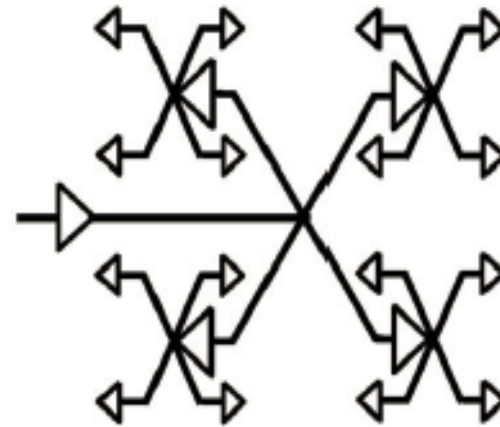
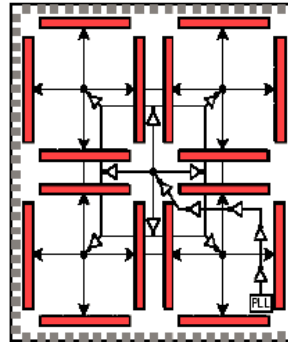
- Clock frequency at any point in the clock tree is not constant.



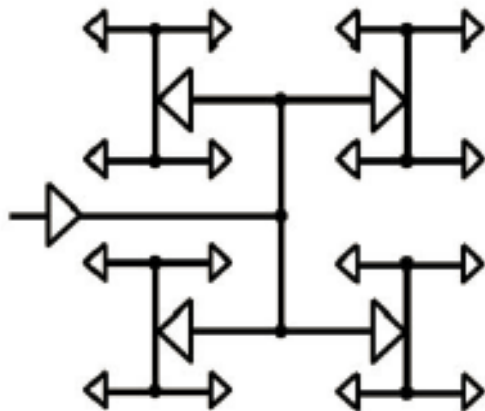
Variations of tree distribution networks



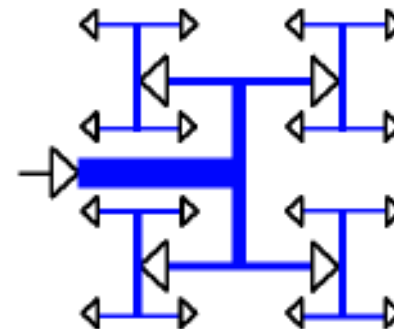
Tree



X-Tree

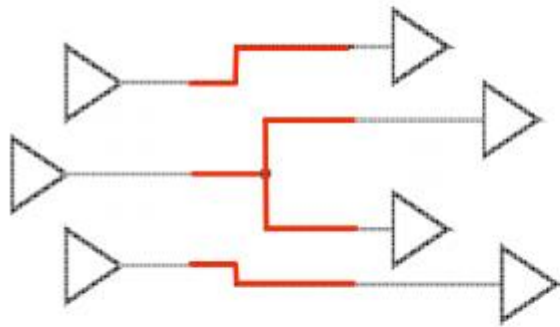


H-Tree



Tapered H-Tree

The Wire



Schematic



Physical

Agenda

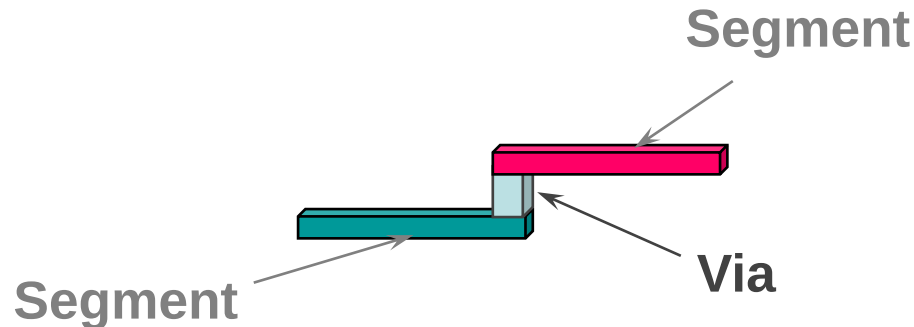
- Interconnect Definition
- RC Equation of a Line
- Interconnect Resistivity
- Interconnect Capacitance
- Cross Capacitance & Miller Effect
- Interconnect Modeling
- Repeaters
- Interconnect DO's and DON'Ts

Interconnect Definition

- Interconnect is any net used to connect two different pins on the layout, commonly referred to as metal layer.
- Each process has a different number of metal layers.
- Each metal layer has specific electrical parameters defined by process file.
- The minimum width and minimum spacing provided by process process file.
- .

Interconnect Definition – Cont'd

- An interconnect net includes segments and Vias.
- Segment: Is a polygon of metal layer.
- Vias: Is the connection between segments from different metal layer.



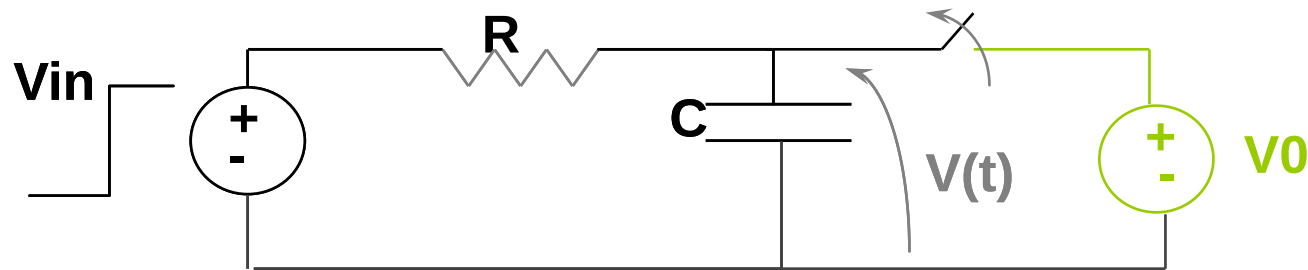
Process example Layer's Properties

Layer	RC	Where to use it.
M1	Very High	Local interconnect.
M2	Very High	Local interconnect.
M3	High	Some internal buses
M4	Medium	Critical signals & buses in fub
M5	Medium_low	Clk, critical signals & buses
M6	Low	Clk, Full chip signals & buses
M7	Low	Clk, Full chip signals &buses

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First Order Line model (RC Model)



Current law

$$I_R + I_C = 0$$

$$V/R + C \, dv/dt = 0$$

$$dv/V = -1/RC \, dt$$

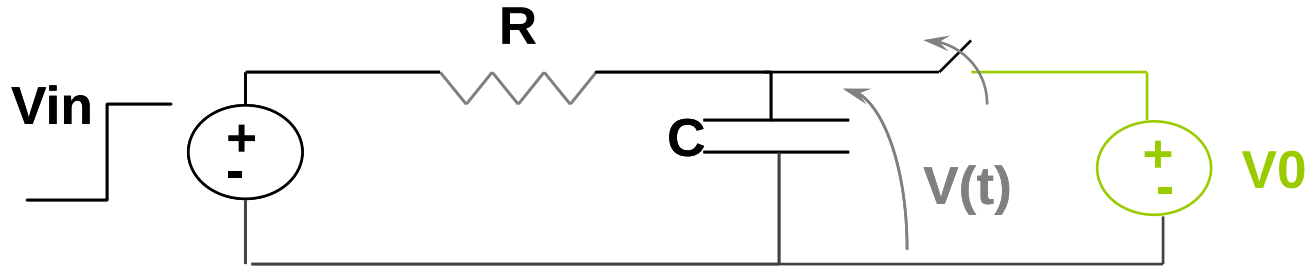
$$\int dv/V = \int -1/RC \, dt$$

$$\ln V = -1/RC \, t + \text{CON}$$

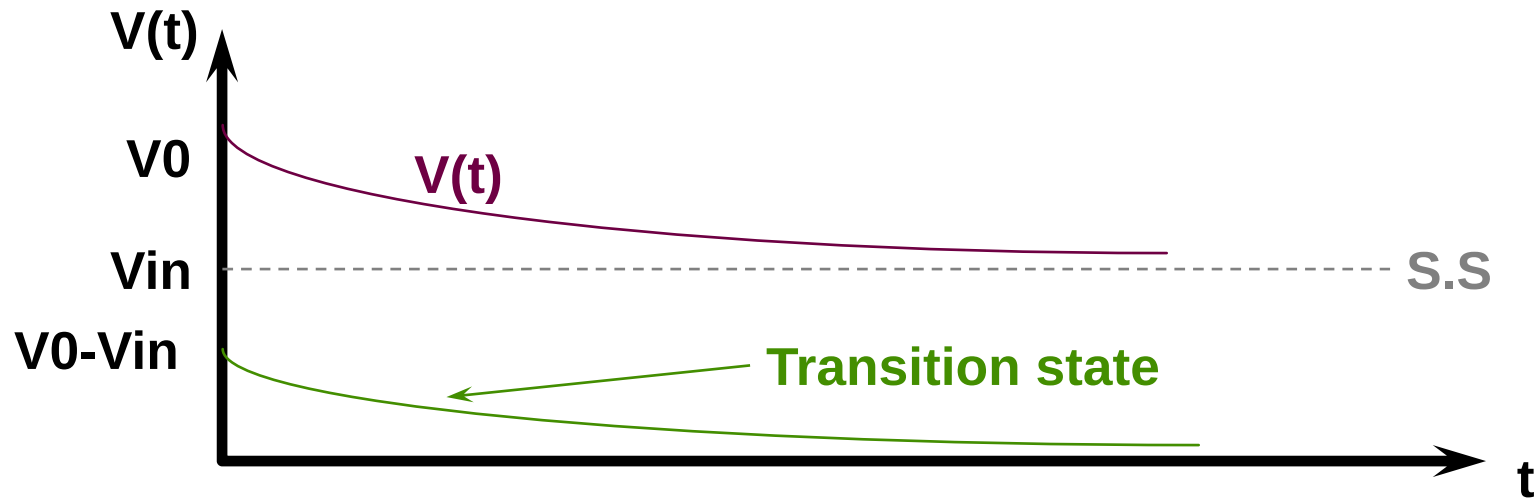
$$V(t) = A e^{-1/RC \, t}$$

$$V(t) = V_0 e^{-t/RC}$$

First Order Line model (RC Model)



- $$V(t) = V_0 e^{-t/rc} + V_{in} (1 - e^{-t/rc})$$



Resistance, Capacitance & Inductance

RESISTOR

$$V(t) = R * i(t) , \quad R = V / I = V / A = \Omega$$

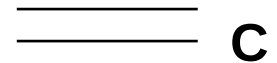


$$P(t) = I^2 R = V^2 / R , \quad W(t_0, t_1) = R \int_{t_0}^t I^2 \partial \tau = \frac{1}{R} \int_{t_0}^t V^2 \partial \tau$$

CAPACITOR

$$Q(t) = CV , \quad C = Q / V = A * Sec / V = FARAD$$

$$I(t) = \partial Q / \partial \tau = \partial (CV(t)) / \partial \tau = C \partial V / \partial \tau$$



$$V(t) = V(t_0) + 1/c * \int_{t_0}^t I(t) \partial \tau \quad P(t) = CV(t) \partial V / \partial \tau$$

INDUCTOR

$$\Phi(t) = L * I(t) , \quad L = \Phi / I = \text{weber} / A = V * Sec / A = \text{Henry}$$

$$V(t) = \partial \Phi / \partial \tau = \partial (LI) / \partial \tau = L * \partial I / \partial \tau$$

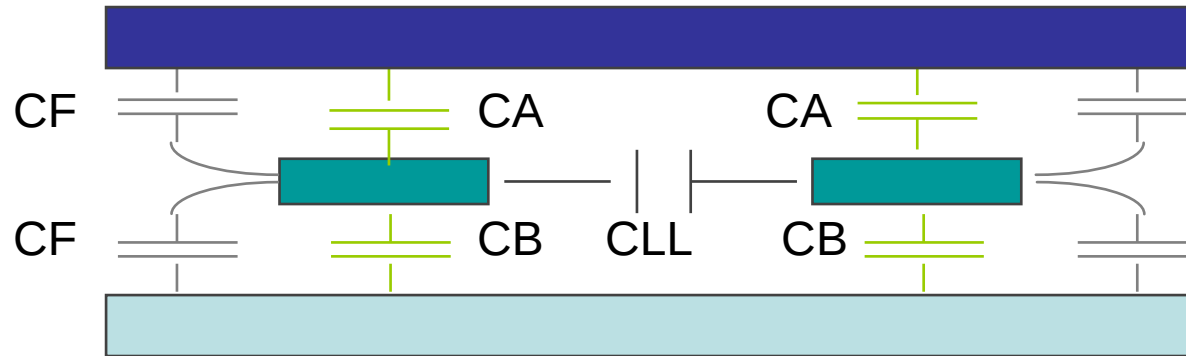


$$I(t) = I(t_0) + \frac{1}{L} \int_{t_0}^t V(t) \partial \tau , \quad P(t) = L * I * \partial I / \partial \tau$$

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- Interconnect Resistivity
- Interconnect Capacitance
- Cross Capacitance & Miller Effect
- Interconnect Modeling
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Interconnect Capacitance

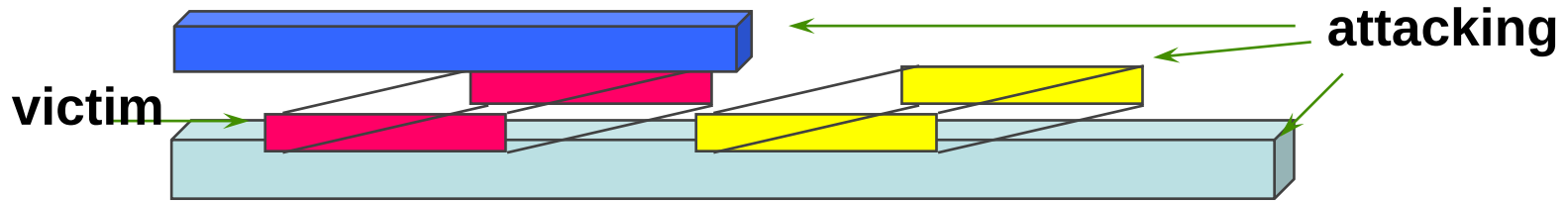


CLL Line to Line Capacitance.

CA, CB Capacitance to Other Plane.

CF Fringing Capacitance.

Cross Capacitance

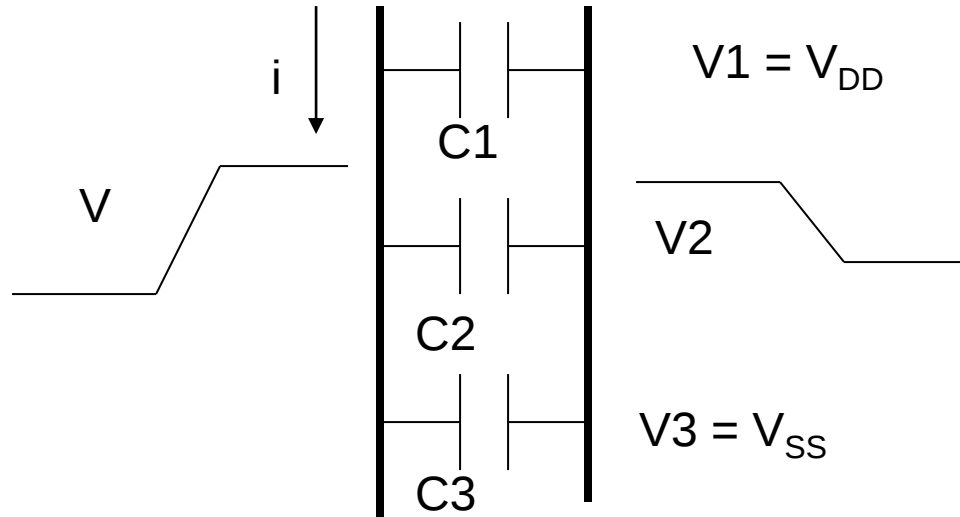


- Cross Capacitance is any capacitance between nets, which are non DC nets.
- In the worst case all the capacitance between nets can be cross capacitance.
- We call the signal that we are analyzing the **victim**, and all the signals that have cross capacitance to it we will call them **attacking** signals.

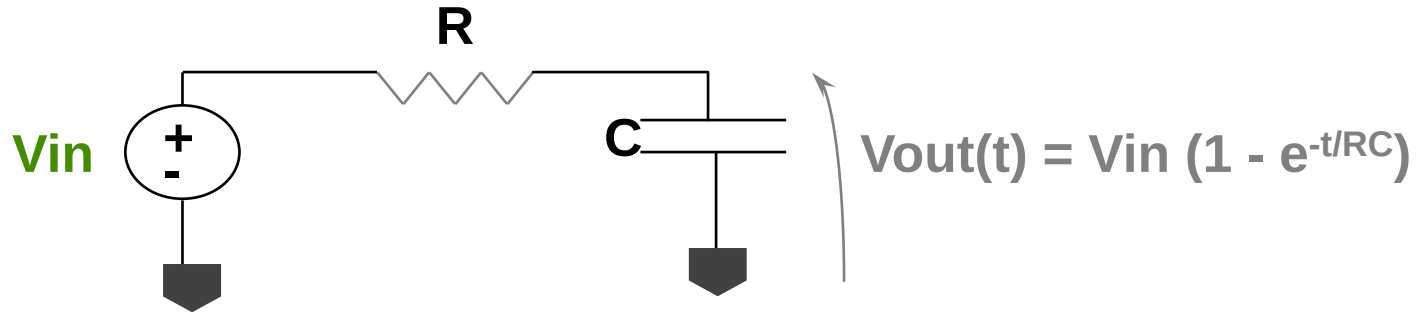
Cross Capacitance & Miller Effect

- Remembering the current-voltage equation for a capacitor
 $i(t) = C * dv(t)/dt$
- In case that the **attacking signal** is also switching, then the $dv(t)/dt$ is actually bigger or smaller than the DC case, depending on the switching directions of the victim and attacking signals.
- In verification tools we always calculate the voltage referenced to the Ground “Vss” which is a DC signal.
- We can see this effect as if the effective capacitance between the line and the Ground changes, this is called the **Miller Effect**.
- Miller Coefficient is the factor that we use to multiply the Xcap in order to model the Miller Effect.

Miller Coupling Mathematics

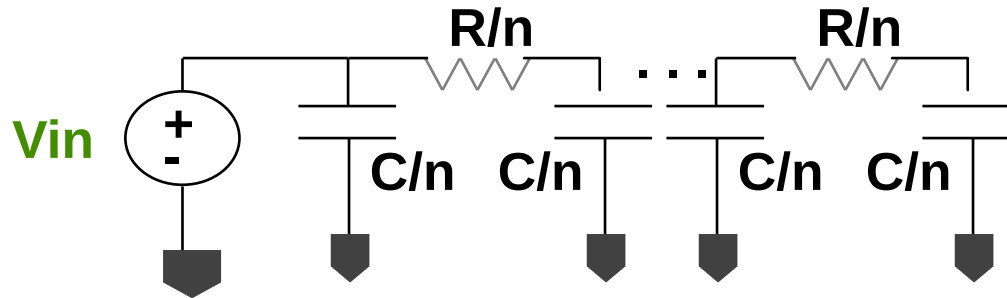


Lumped Line Model

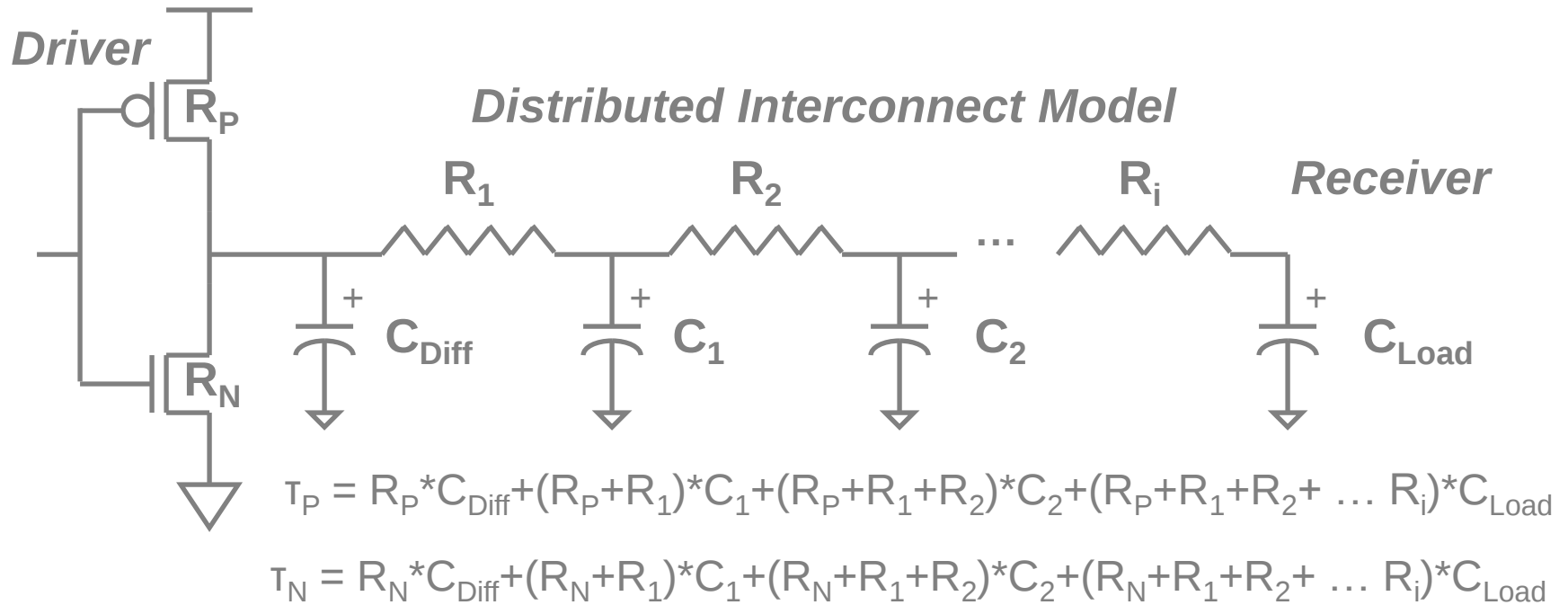


- A lumped model is a pessimistic one, which assumes that all the capacitance, line and load, is located at the end of the line, in other words that the driver “sees” the total load through the total line resistance.
- As the RC delay increases the lumped RC model is less and less accurate.

Distributed Line Model

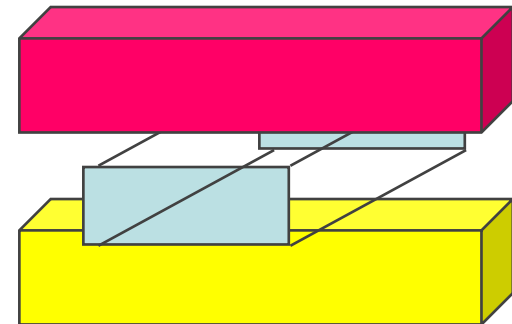
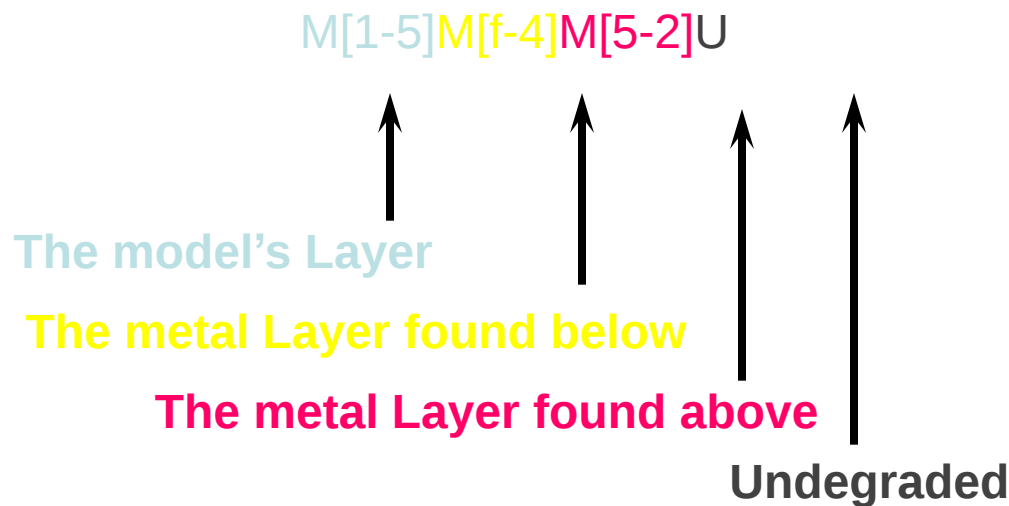


- The distributed line model is a more accurate model which assumes that the line is built out of many segments, when each segment is modeled as a lumped RC model.
- For calculating the RC delay using the distributed model a simulation is needed



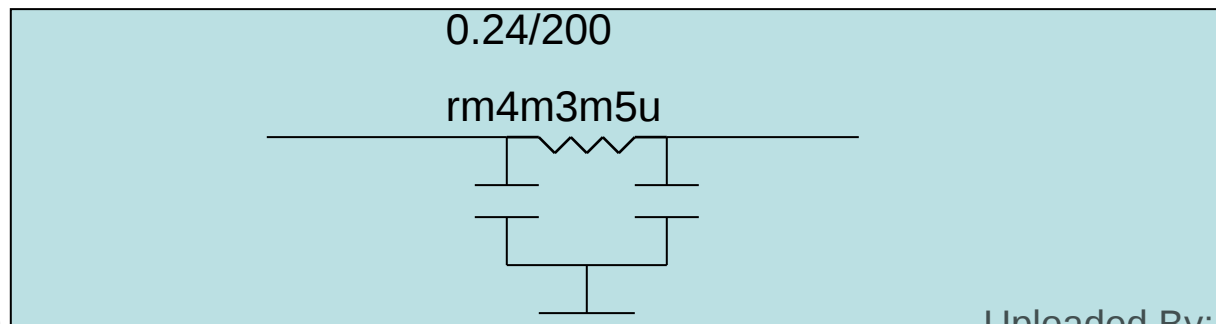
Line Capacitance Models

- Unlike the Line resistance, its capacitance is dependent not only on the line topography, but also on its neighbors from all directions.
- In order to model the Line capacitance we define the parameters for all the possible configurations, and then map each line segment to one of these configurations.
- The naming convention of the models is:

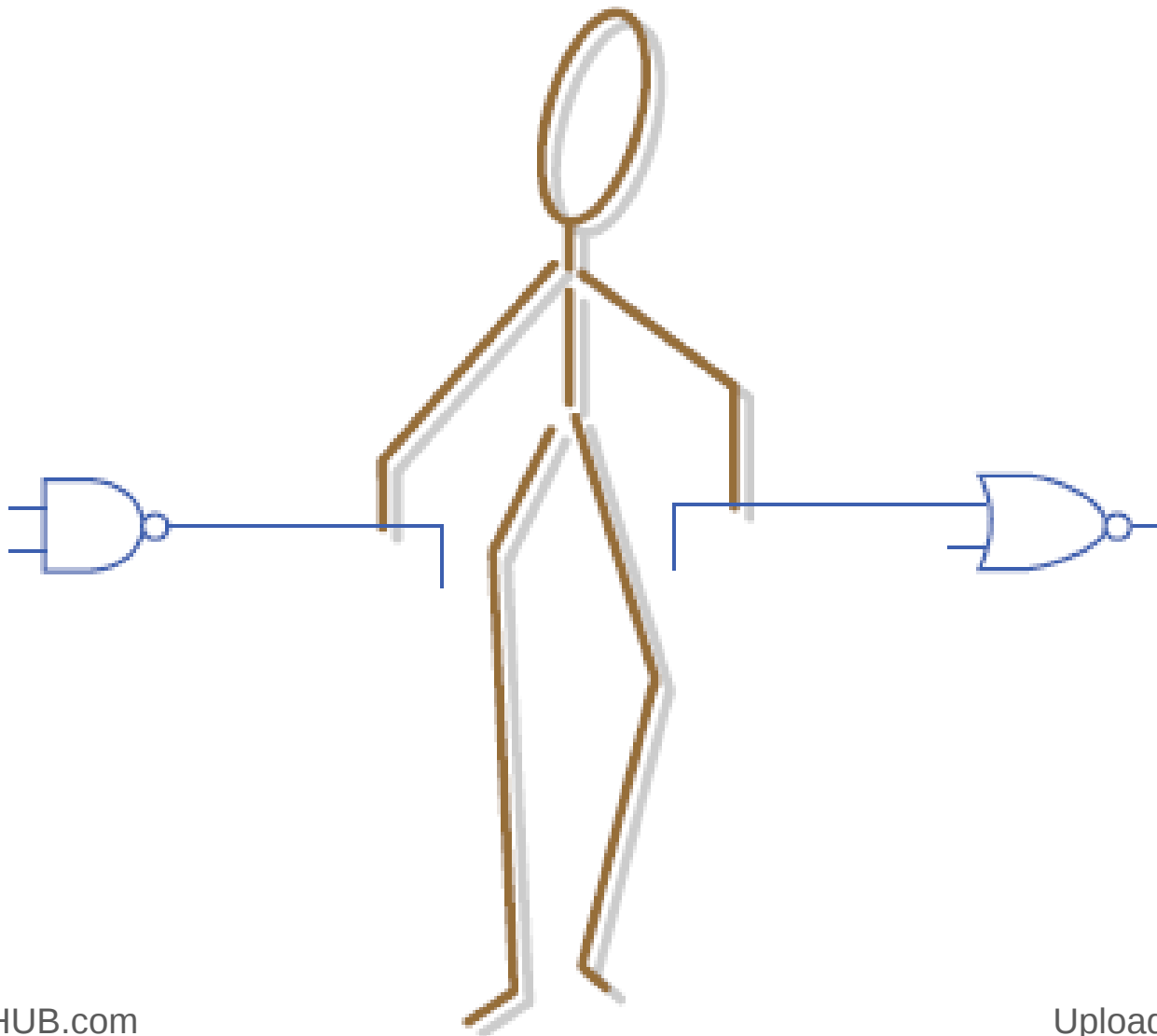


FTRC Elements

- The **FTRC** element is a library cell which enables the user to build a line simulation model using the lumped approximation for the distributed line.
- The FTRC element has the following parameters
 - **MODEL**: define the segment's capacitance and resistance model the model should be one of the process file defined models (m2m1m3u, m1fm4, ...)
 - **wid**: The segment width
 - **Spc**: The segment spacing
 - **Length**: The length of the segment



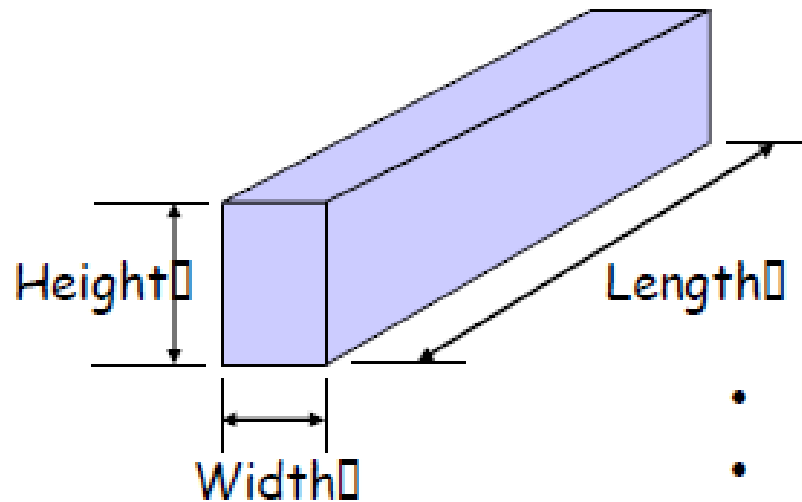
Wires



Interconnect Problems

- A lot of circuit designers are very worried about what's happening with wires in CMOS technology
- Device technology **has been scaling well, with gate performance increasing linearly with decreasing feature size**
- Wires **scale differently, and long wires have been getting relatively slower over time**
- delay is a function of **wire resistance and capacitance**

Wire Resistance



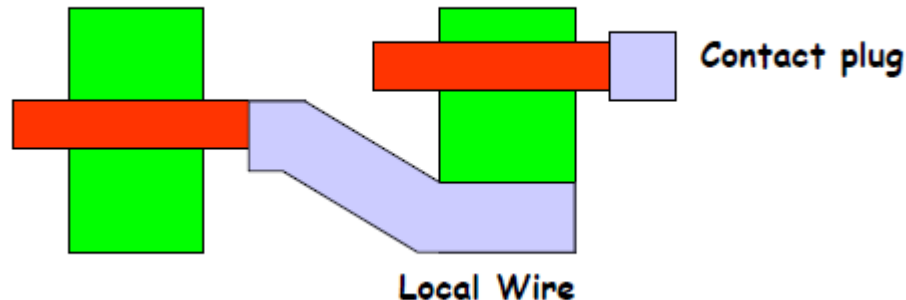
$$\text{resistance} = \frac{(\text{length} \times \text{resistivity})}{(\text{height} \times \text{width})}$$

- bulk aluminum $2.8 \times 10^{-8} \Omega\text{-m}$
- bulk copper $1.7 \times 10^{-8} \Omega\text{-m}$
- bulk silver $1.6 \times 10^{-8} \Omega\text{-m}$

- Height (Thickness) fixed in given manufacturing process
- Resistances quoted as Ω/square
- TSMC 0.18 μm 6 Aluminum metal layers
 - M1-5 0.08 Ω/square (0.5 μm $\times$ 1mm wire = 160 Ω)
 - M6 0.03 Ω/square (0.5 μm $\times$ 1mm wire = 60 Ω)

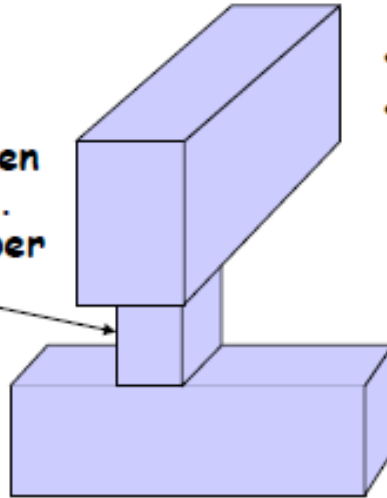
Local Interconnect

- Use contact material (tungsten) to provide extra layer of connectivity below metal 1
- Can also play same trick with silicided poly to connect gates to diffusion directly in RAMs
- Typically used to shrink memory cells or standard cells
- Contacts directly to poly gate or diffusion



Via Resistance

Vias made from Tungsten
in Aluminum processes.
Vias are Copper in Copper
processes



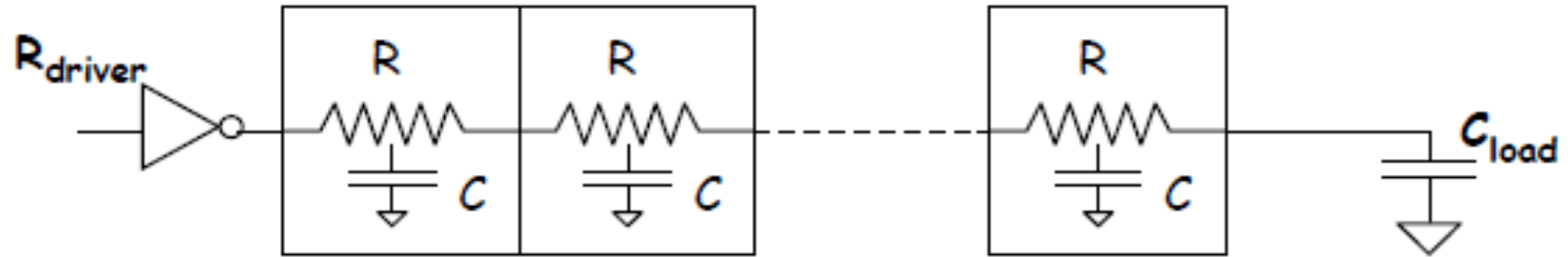
- Via resistance significant

- TSMC 0.18 μ m 6-Al

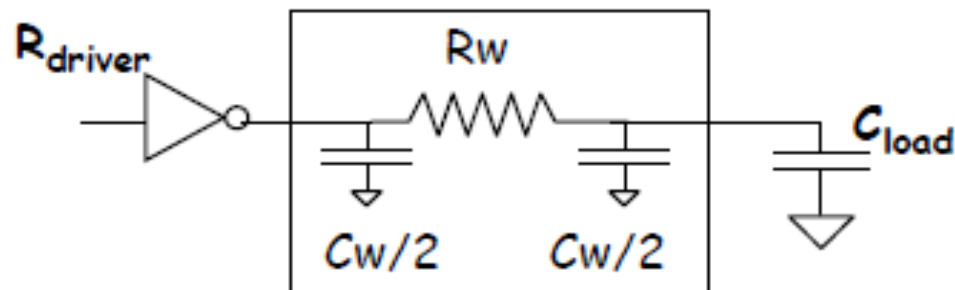
Diff-M1	11.0 Ω
Poly-M1	10.4 Ω
M2-M1	4.5 Ω
M3-M1	9.5 Ω
M4-M1	15.0 Ω
M5-M1	19.6 Ω
M6-M1	21.8 Ω

- Resistance of two via stacks at each end of M1 wire equivalent to about 0.1 mm wire ($\sim 20 \Omega$)
- Resistance of two via stacks at each end of M6 wire about the same as 1 mm narrow M6 wire ($\sim 60 \Omega$)!!!
- Use multiple vias in parallel to reduce effective contact resistance
- Copper processes have lower via resistance

RC Delay Estimates

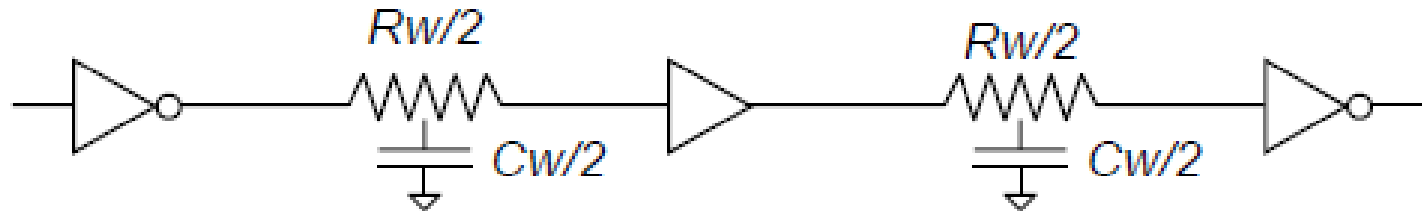
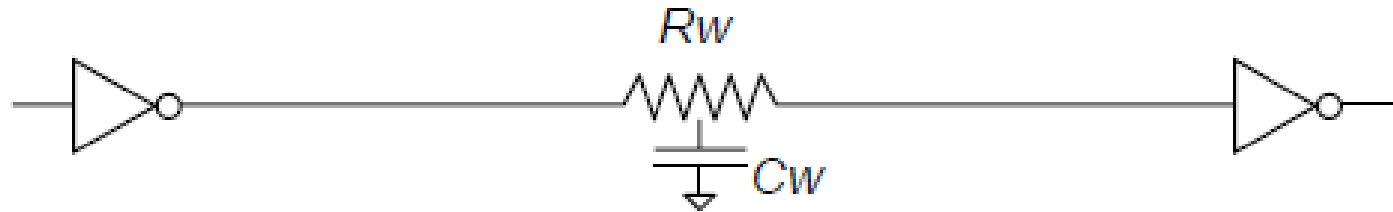


- Wire has distributed R and C per unit length
 - wire delay increases quadratically with length
 - edge rate also degrades quadratically with length
- Simple lumped Π model gives reasonable approximation
 - R_w is lumped resistance of wire
 - C_w is lumped capacitance (put half at each end)



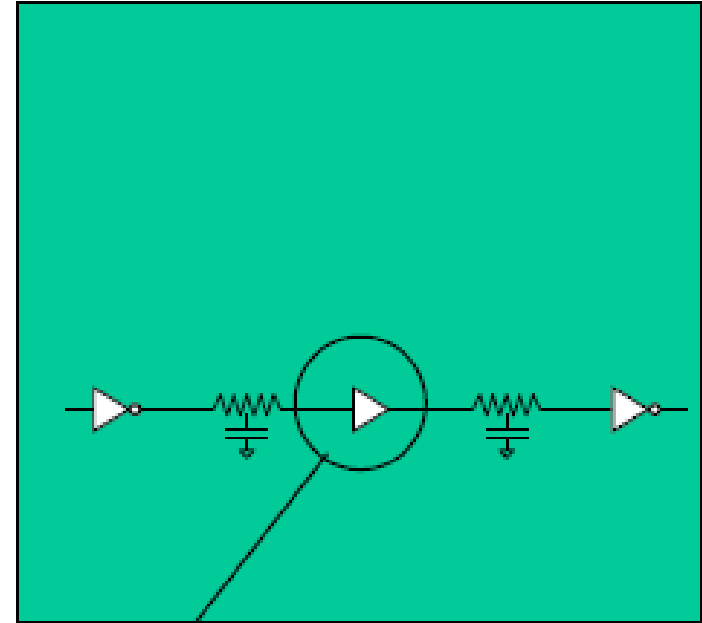
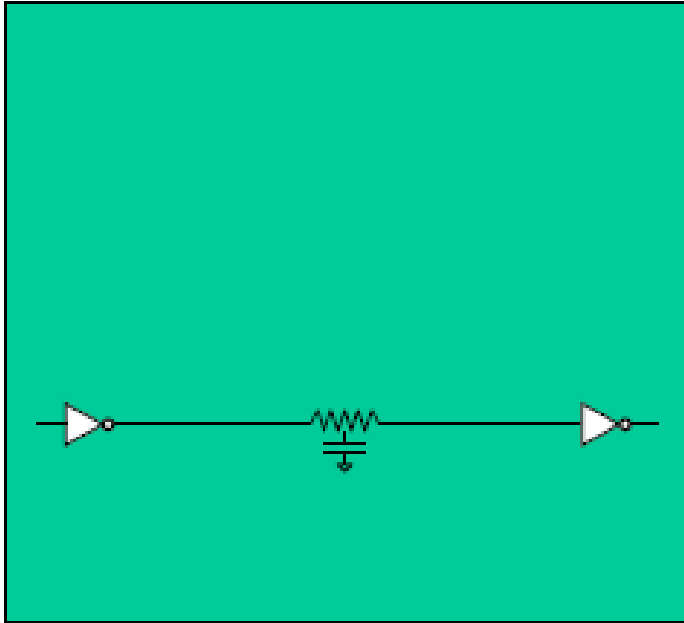
$$\text{Delay} = R_{\text{driver}} \times \frac{C_w}{2} + (R_{\text{driver}} + R_w) \times \left(\frac{C_w}{2} + C_{\text{load}} \right)$$

Circuit Fixes - Repeaters



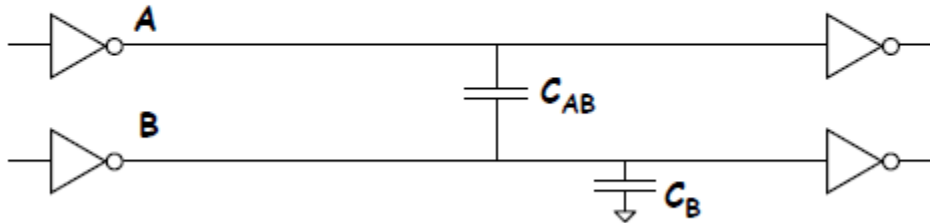
- Use repeaters
- Converts quadratic dependence into linear dependence on length (but watch the constants)
- Can determine optimal repeater sizing for minimum delay

Repeater Issues



- Repeater must connect to transistor layers
- Blocks other routes with vias that connect down
- Requires space on active layers for buffer transistors and power connections
- Repeaters often grouped in preallocated repeater boxes spread around chip
 - repeater location might not give ideal spacing

Fixing Coupling Problems

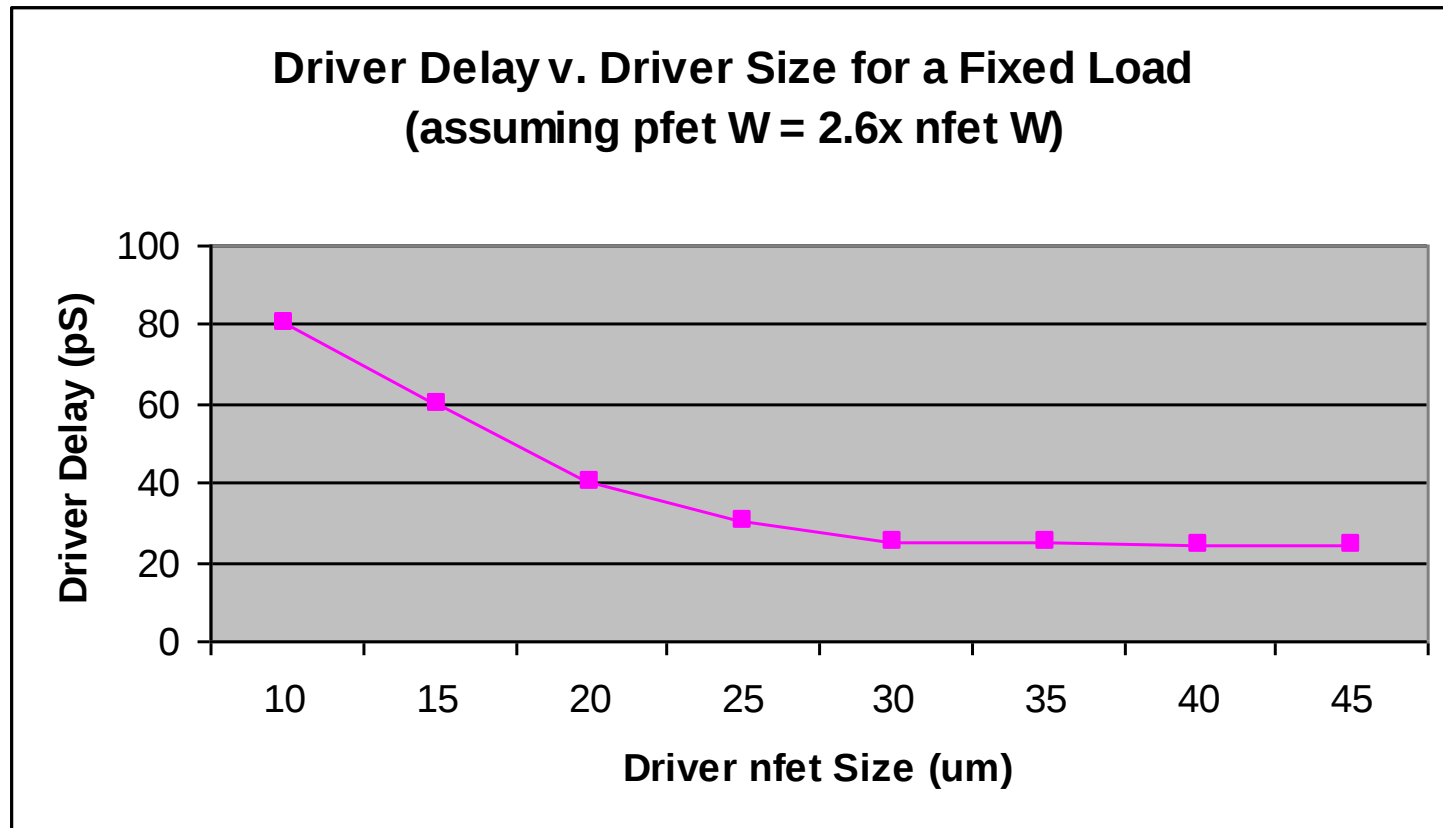


- Avoid placing simultaneously switching signals next to each other for long parallel runs
- Reroute signals which will be quiet during switching inbetween simultaneous switching signals
- Route signals close to power rails to provide capacitance ballast
- Tough problem to solve - moving one wire can introduce new problems
 - "timing closure" causes many real-world schedule slips



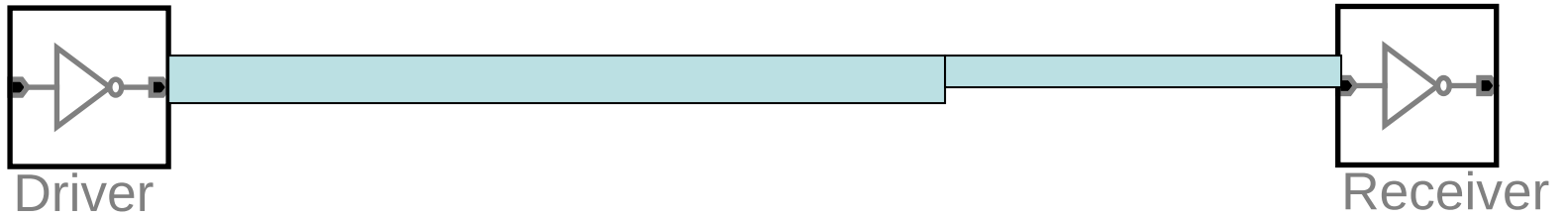
Repeaters

- Use repeaters to break lengthy high-metal routes into segments
- It also assists in preventing your routes from running into slope and noise issues
- Bigger repeaters don't always translate into faster paths; use the right sized device for the job
- Don't try to squeeze too much out of the interconnect/repeater design solution by over-sizing repeaters just to gain a few pS... often the path can be solved in the driver or receiver fub at a lower total W cost

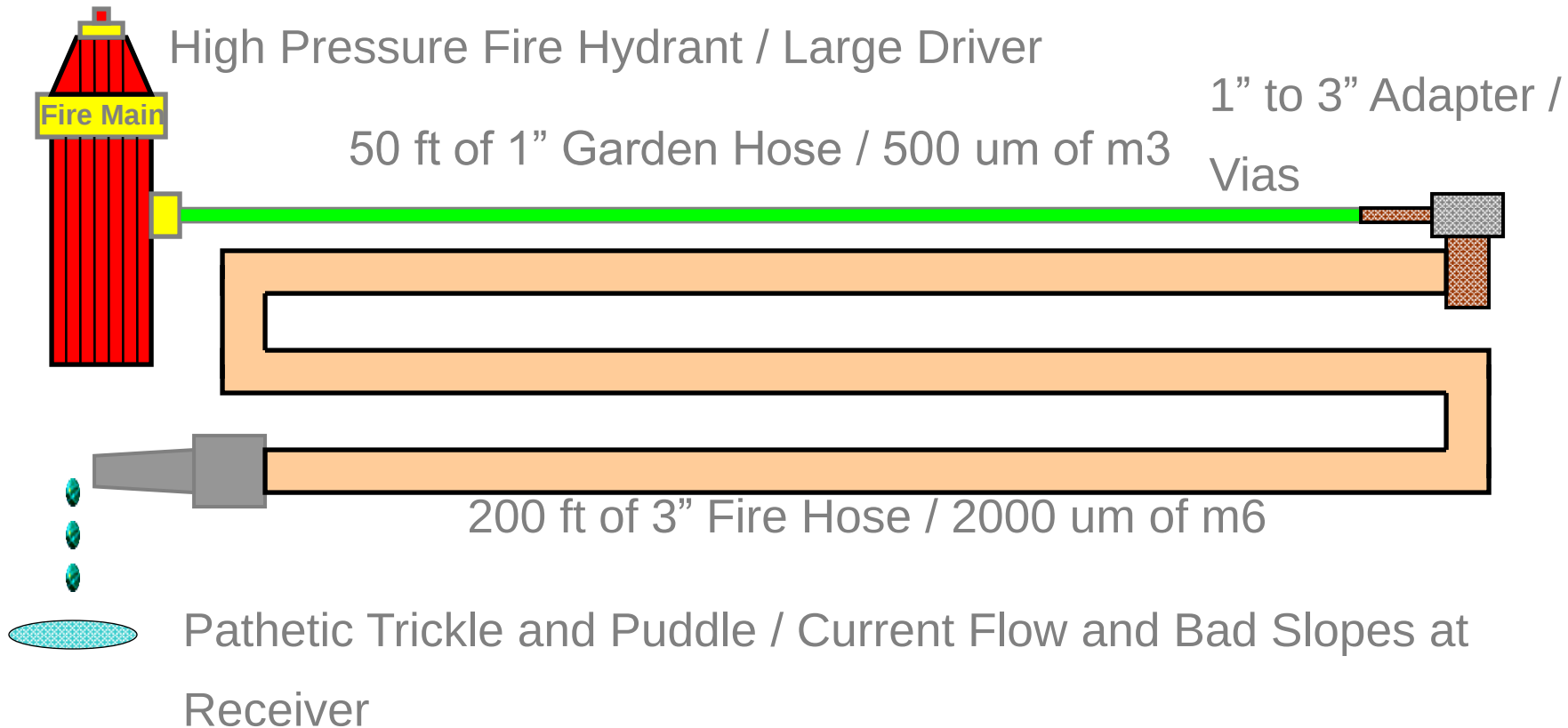


- **Note:** for this example, improvement in driver delay starts tapering off at nfet W = 25 um; this is the knee of the curve after which ROI for further W increases declines rapidly

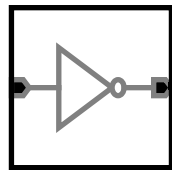
Tapering



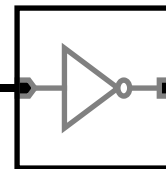
Do Not Do : Example



- Lengthy high metal routes initiating in lengthy m3 routes (> a few hundred microns) fall victim to a large amount of R-shielding of the downstream C. This typically leads to undersized drivers, and even if the drivers are intentionally oversized, the driver is choked off by the lengthy and highly resistive m3.

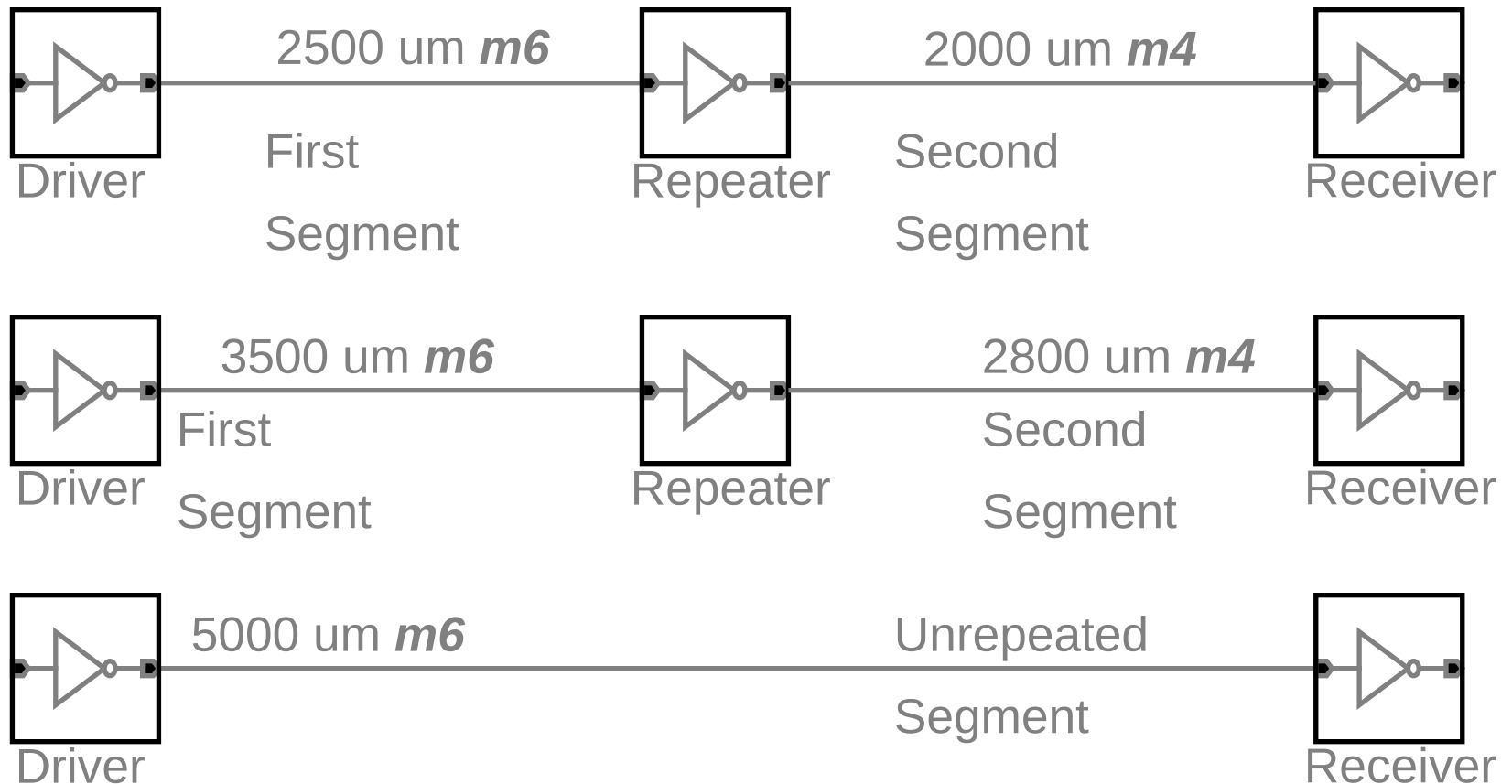


Driver

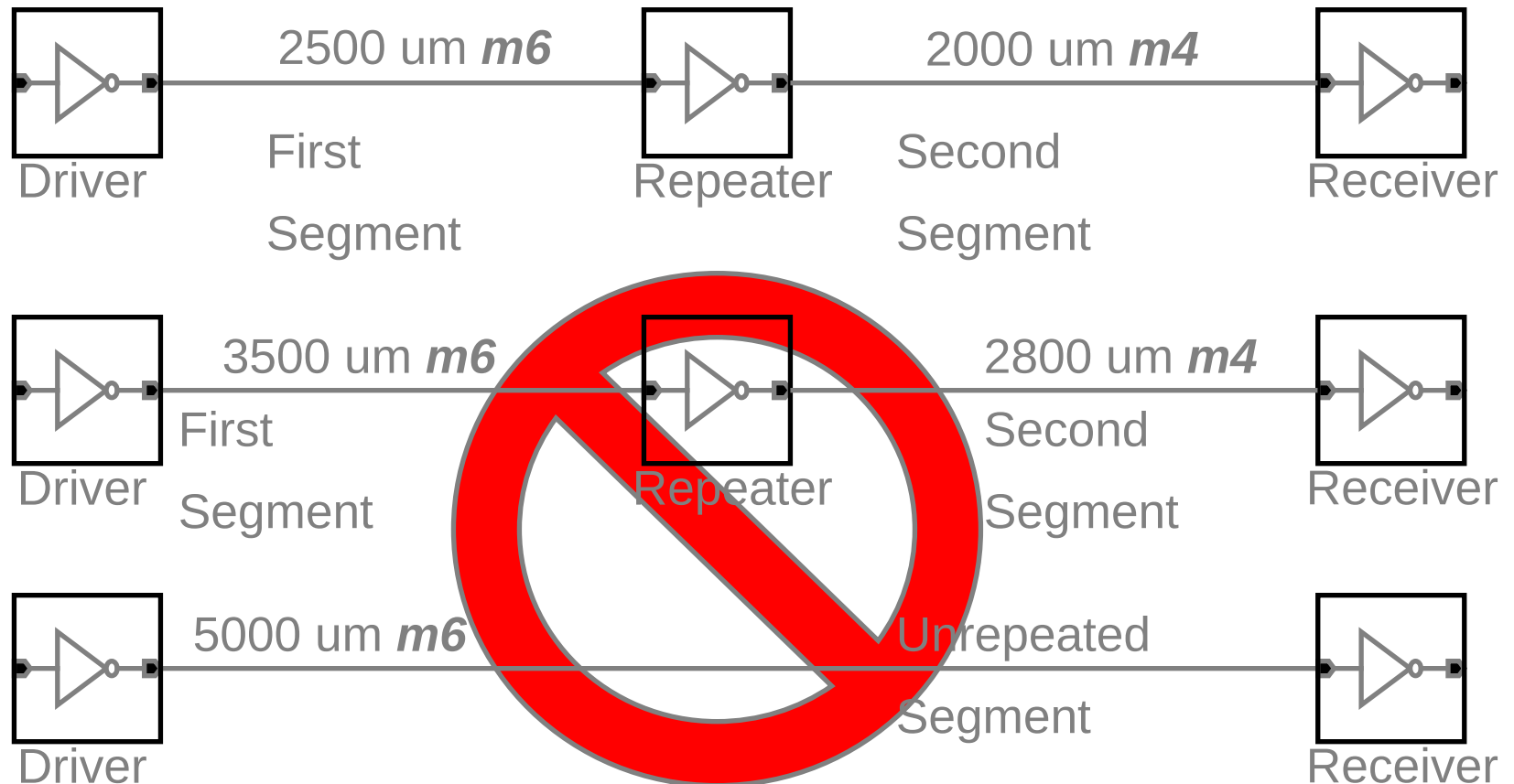


Receiver

Device Rule 1: Example



Device Rule 1: Example



- **Reduce Robustness**
- **Affect Performance**

Classes of Parasitics

- **Capacitive**
- **Resistive**
- **Inductive**

Methods For Improving RC Delay

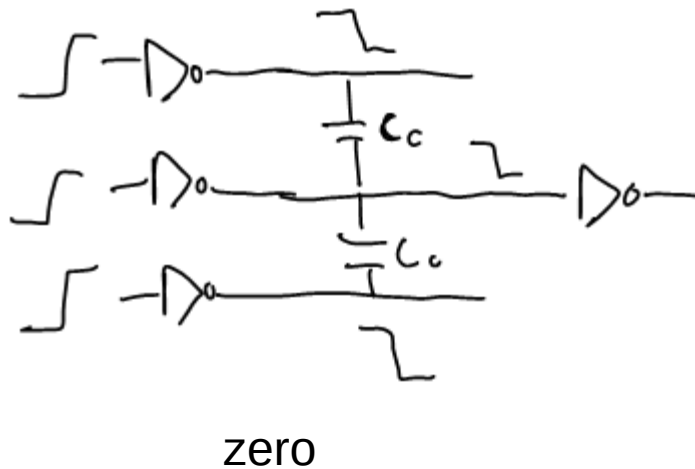
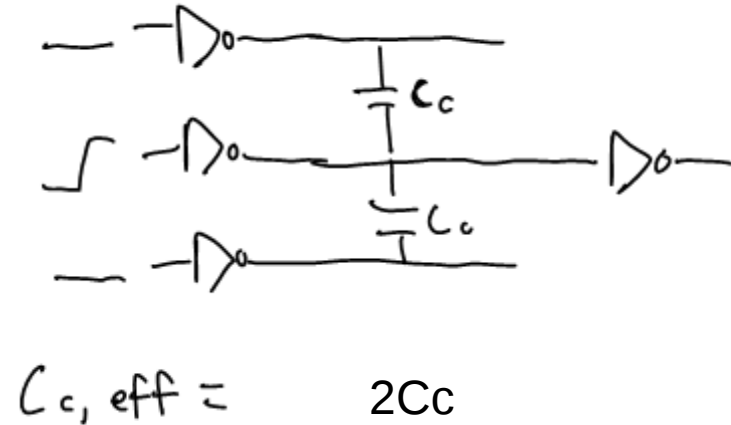
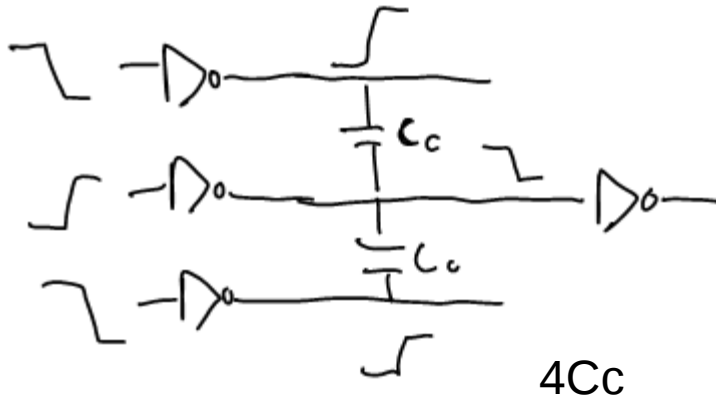
- Optimizing the Routing Path Length
- Tapering & Optimizing the Width Across the Net
- Reducing The Line Cap (Spacing, ...)
- Optimizing the Driver Size
- Reducing The Receivers Load
- Adding Repeaters

Impact of Interconnect Parasitics

- ❑ Interconnect and its parasitics can affect all of the metrics we care about
 - Cost, reliability, performance, power consumption

- ❑ Parasitics associated with interconnect:
 - Capacitance
 - Resistance
 - Inductance

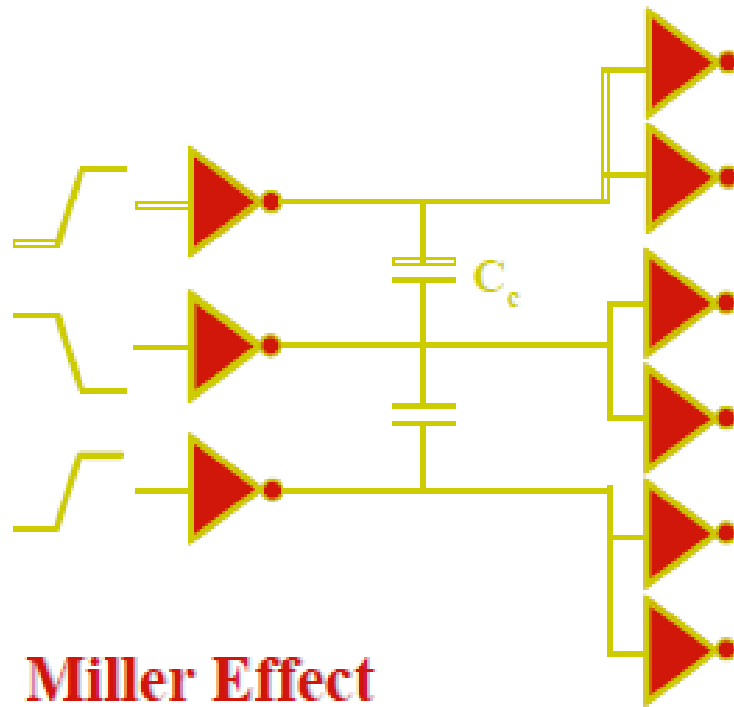
Coupling Capacitance and Delay



Dealing with Capacitive Cross Talk

- Avoid floating nodes
- Protect sensitive nodes
- Make rise and fall times as large as possible
- Differential signaling
- Do not run wires together for a long distance
- Use shielding wires
- Use shielding layers

Delay Degradation



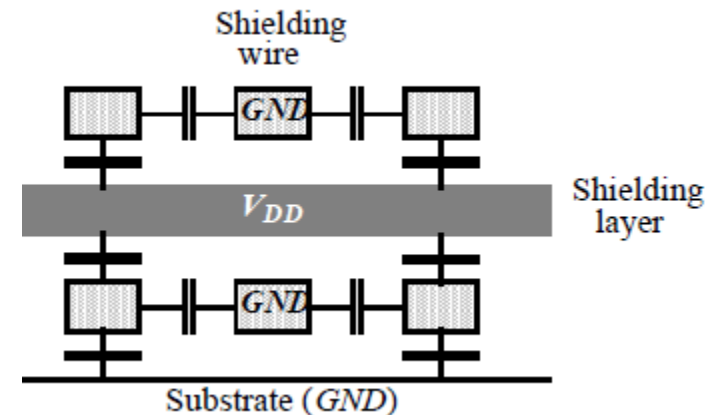
Miller Effect

- Impact of neighboring signal activity on switching delay
- When neighboring lines switch in opposite direction of victim line, delay increases

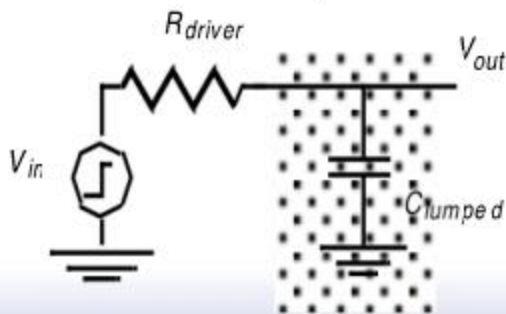
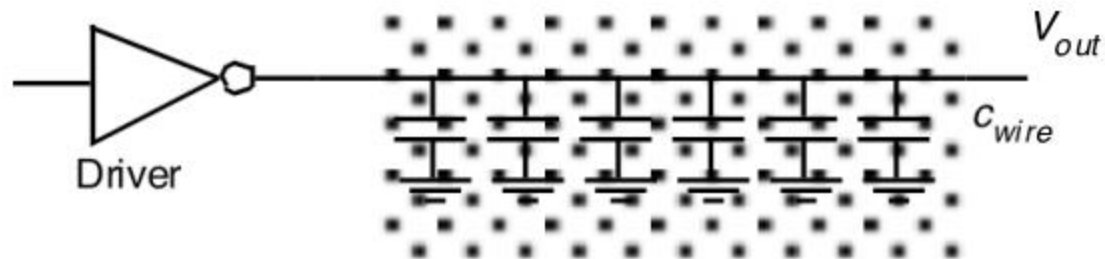
- Both terminals of capacitor are switched in opposite directions
($0 \rightarrow V_{dd}$, $V_{dd} \rightarrow 0$)
- Effective voltage is doubled and additional charge is needed
(from $Q=CV$)

How to Battle Capacitive Crosstalk

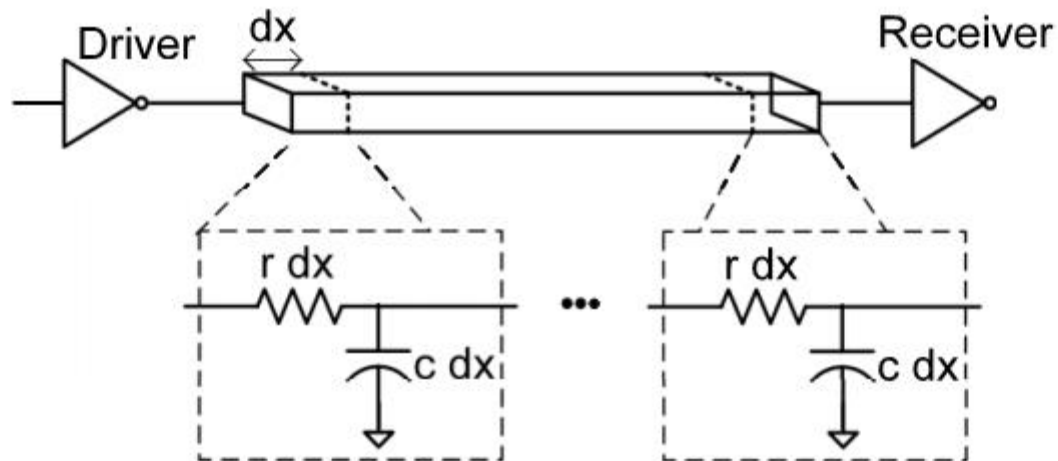
- Avoid large crosstalk cap's
- Avoid floating nodes
- Isolate sensitive nodes
- Control rise/fall times
- Shield!
- Differential signaling



The Lumped Model

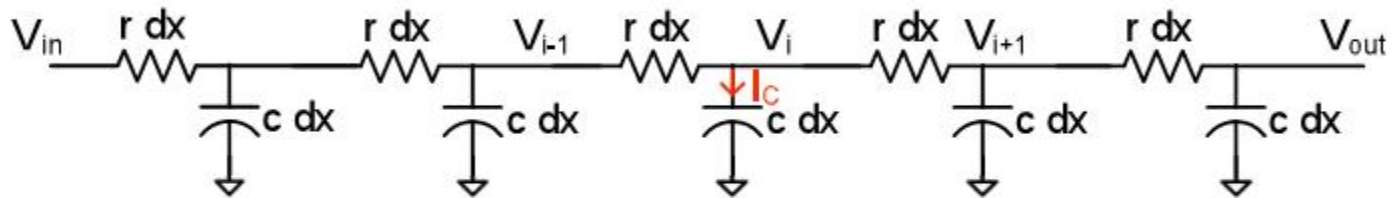


The Distributed RC-line



- Analysis method:
 - Break the wire up into segments of length dx
 - Each segment has resistance ($r dx$) and capacitance ($c dx$)

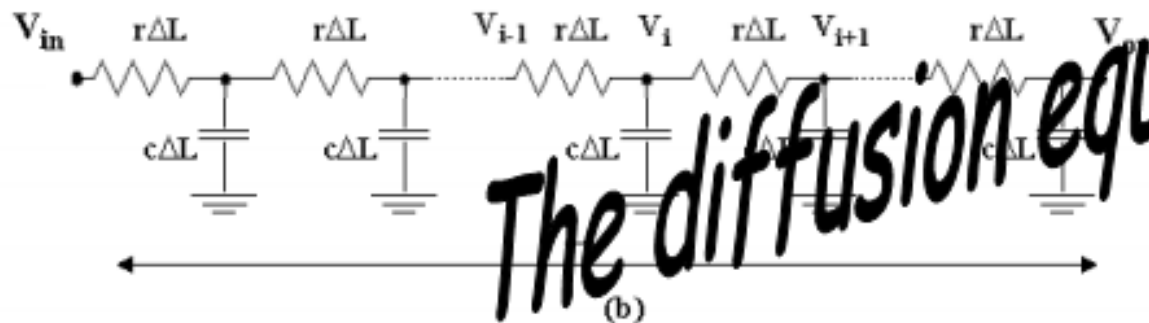
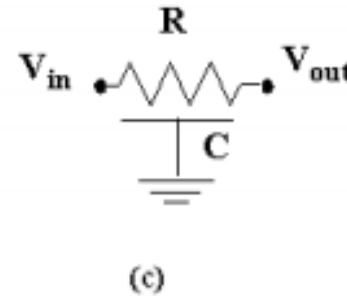
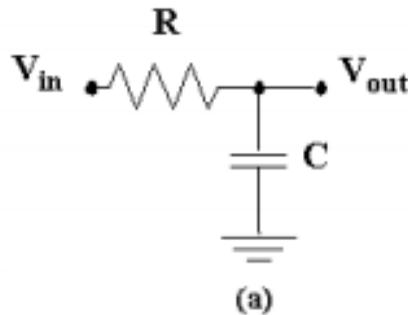
The Distributed RC-line



$$I_c = c \Delta L \frac{\partial V}{\partial t} = \frac{(V_{i-1} - V_i) - (V_i - V_{i+1})}{r \Delta L} \longrightarrow \boxed{rc \frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}}$$

$$\boxed{\tau = \frac{L^2}{2} rc}$$

The Distributed RC Line

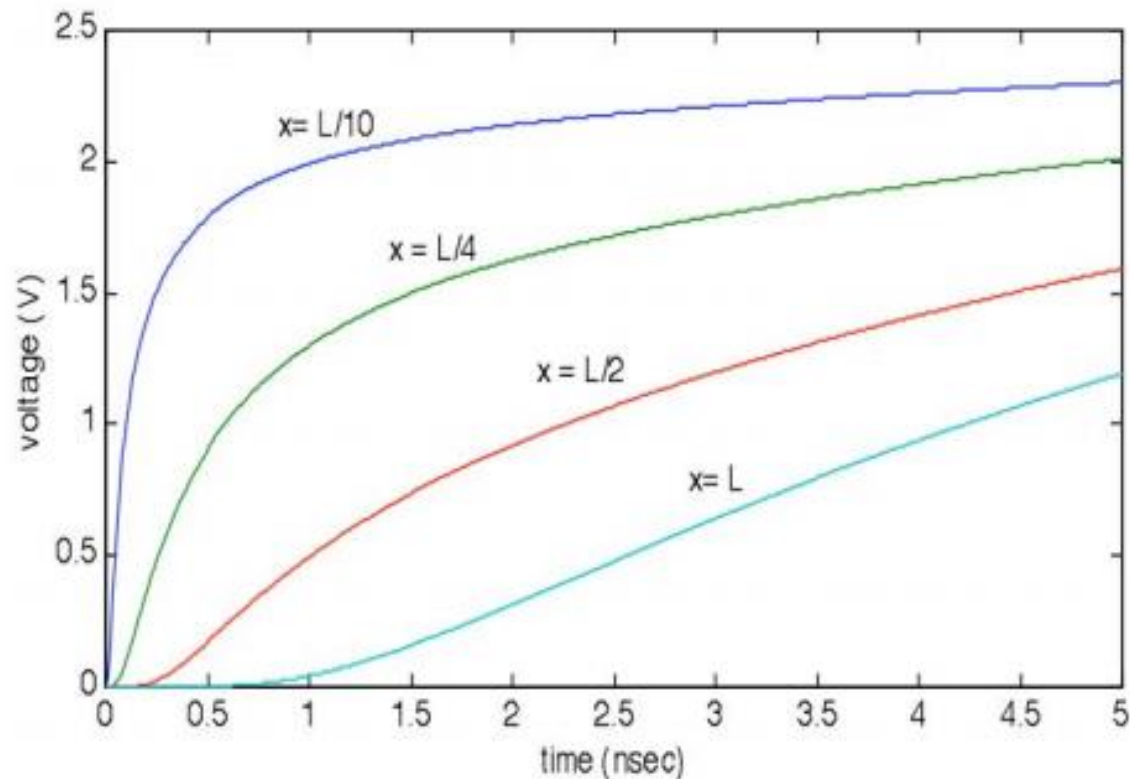


The diffusion equation

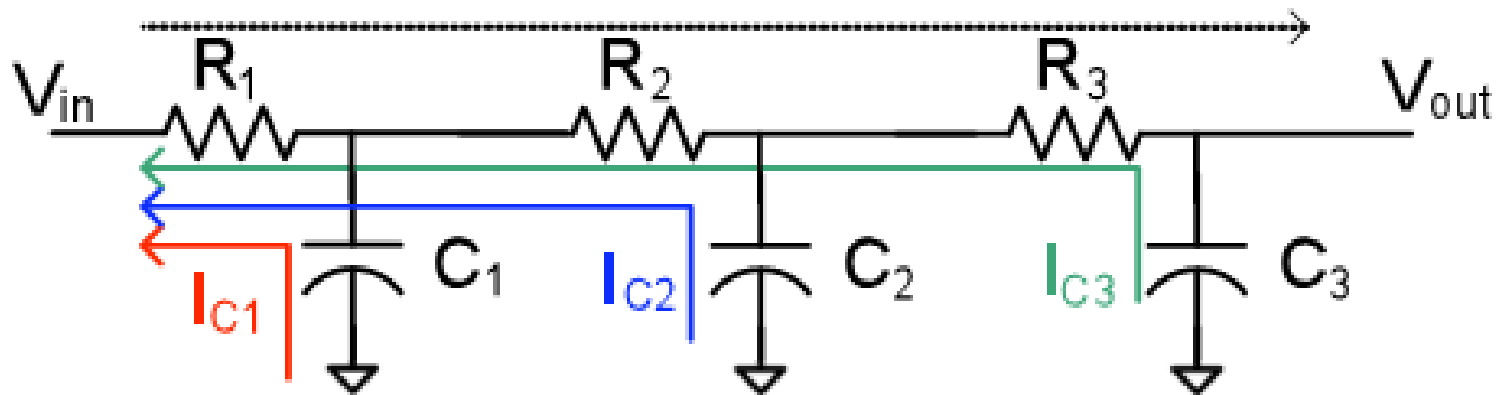
$$rc \frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}$$

$$\tau(V_{out}) = \frac{rc L^2}{2}$$

Step-response of RC wire as a function of time and space



Simplified Model: Elmore Delay



$$\tau_{Elmore} = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2 + R_3) C_3$$

Wire Model

Model the wire with N equal-length segments:

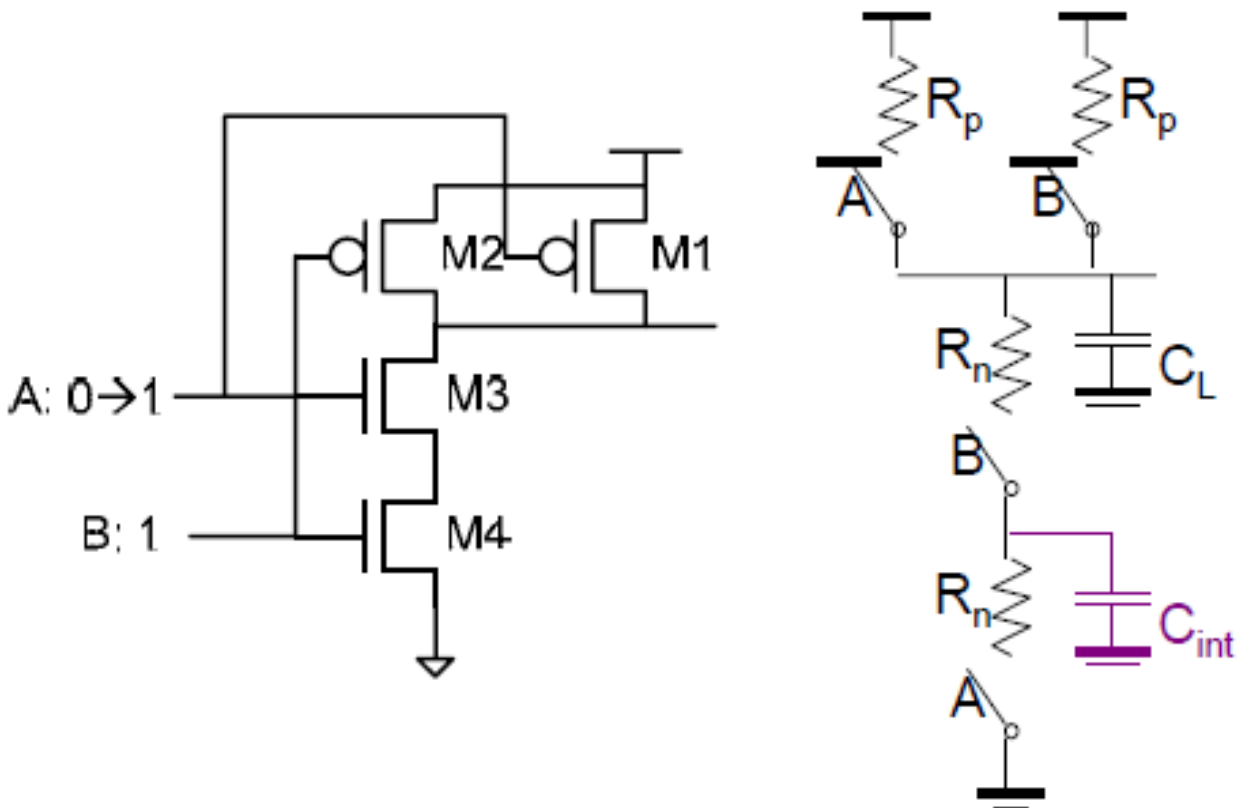
$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \dots + Nrc) = (rcL^2) \frac{N(N+1)}{2N^2} = RC \frac{N+1}{2N}$$

For large values of N:

$$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}$$

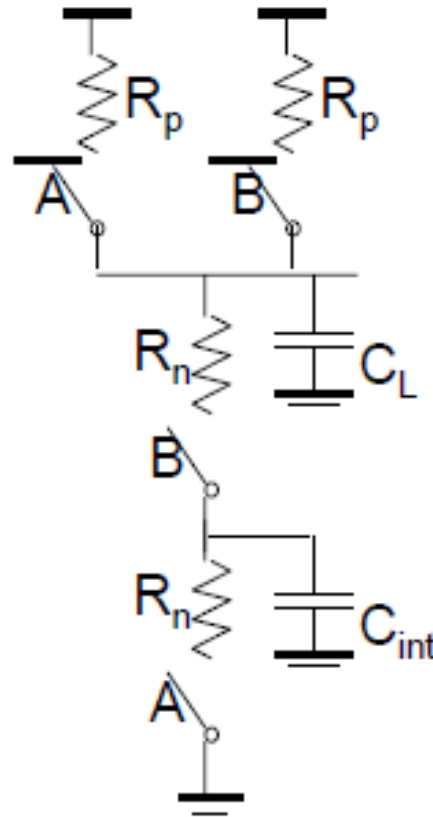
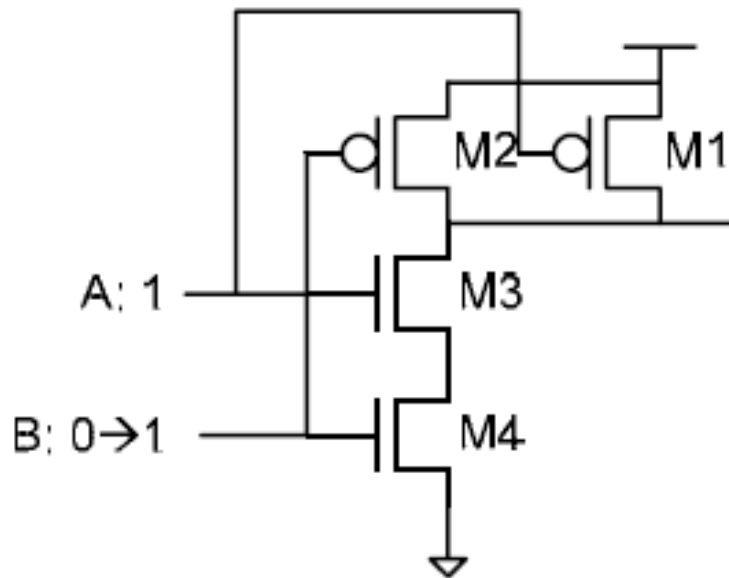
Complex Gate Delay

- ❑ Use RC model to estimate delay:



Complex Gate Delay (2)

□ What is the delay in this case?



PROBLEM.....

PROBLEM 2: Complex Gate Delay

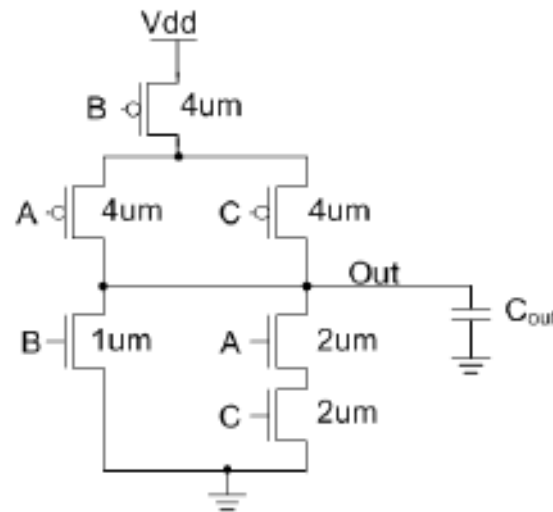
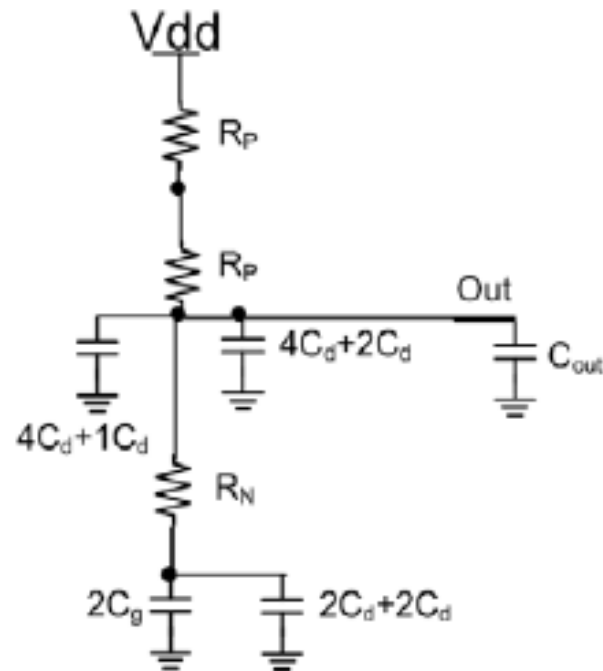


Figure 3.

For this problem you should assume that $L_{\text{min}} = 100\text{nm}$, $C_g = 2\text{ fF}/\mu\text{m}$, $C_d = 1.6\text{ fF}/\mu\text{m}$, $R_p = 20\text{ k}\Omega/\square$, and $R_n = 10\text{ k}\Omega/\square$, $C_{\text{out}} = 12\text{ fF}$.

- a) If $A = 1$ and $B = 0$, draw the switch model you would use to calculate the delay of the gate when C transitions from 1 to zero (i.e., the output going high).

Using the switch model, the equivalent RC circuit we would use to calculate the delay when $A = 1$, $B = 0$, and C transitions from 1 to zero is shown below.



b) What is the delay of the gate in this case?

Solution:

Using Elmore delay, the time constant for this circuit is:

$$\tau_{LH} = 2R_P(5C_d + 6C_d + 2C_g + 4C_d + C_{out})$$

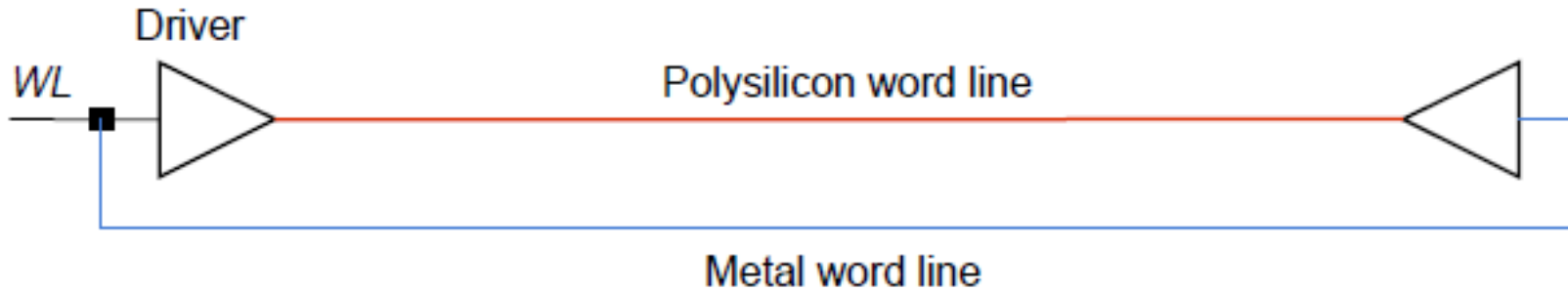
Where the resistance of each PMOS transistor is:

$$R_P = R_p \frac{L}{W} = 20k\Omega \frac{0.1\mu m}{4\mu m} = 500\Omega$$

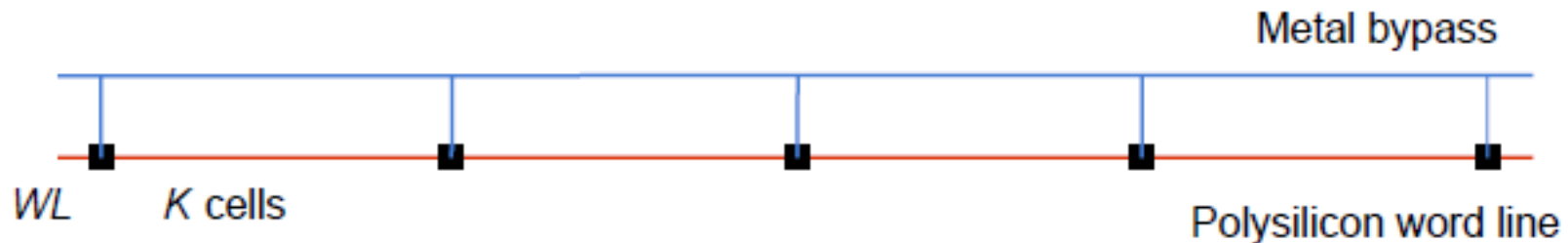
Therefore, t_{pLH} for the gate will be:

$$t_{pLH} = \ln 2 \times \tau_{LH} = \ln 2 \times 2 \times 500\Omega \times (5 \times 1.6fF + 6 \times 1.6fF + 2 \times 2fF + 4 \times 1.6fF + 12fF) \approx 27.73ps$$

Using Bypasses

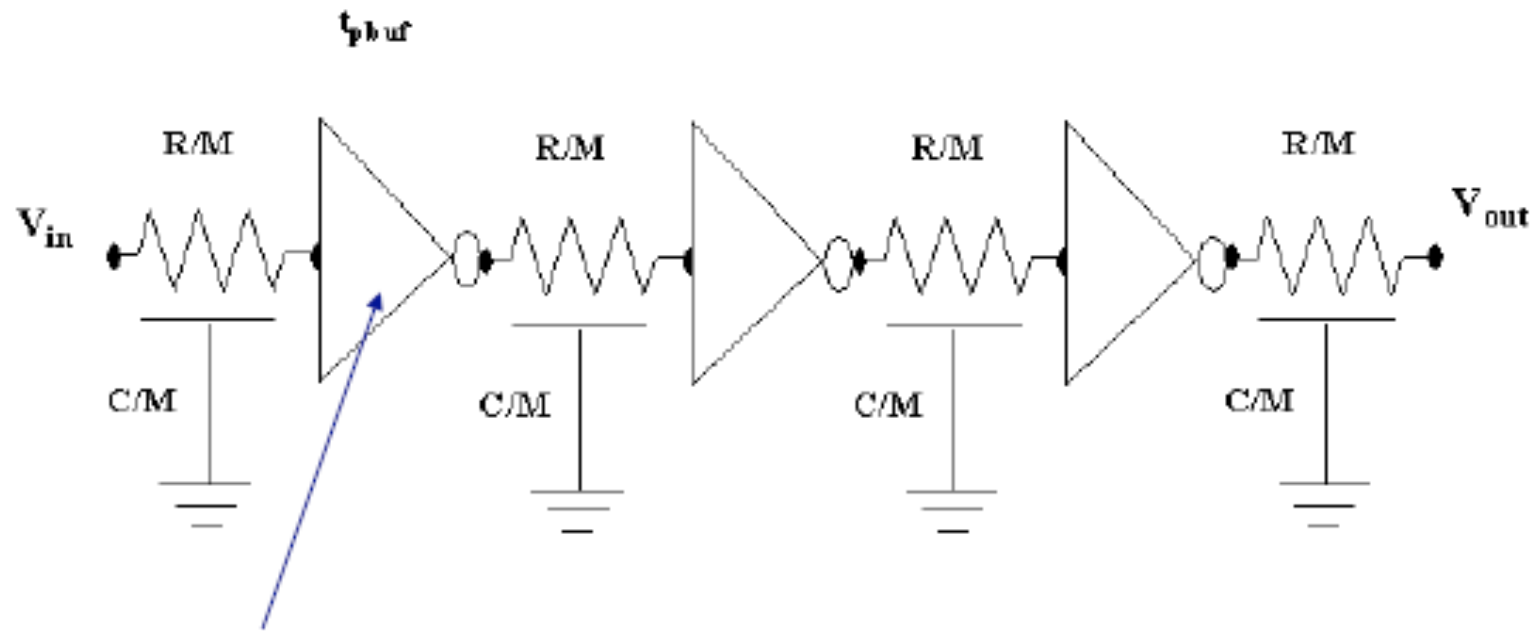


Driving a word line from both sides



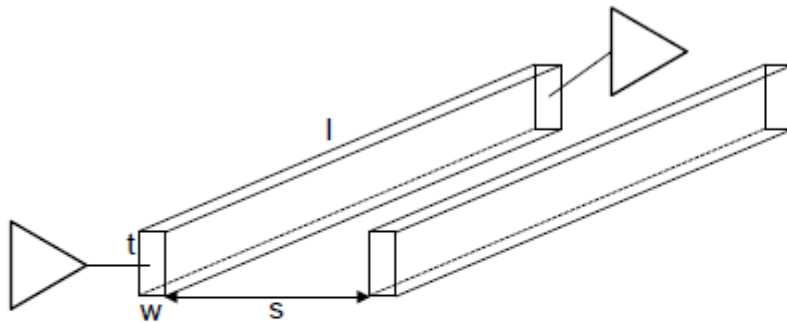
Using a metal bypass

Reducing RC-delay Using Repeaters

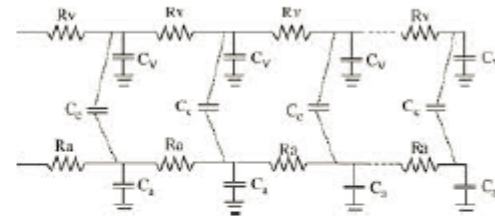


Repeater

Interconnect delay



modeling



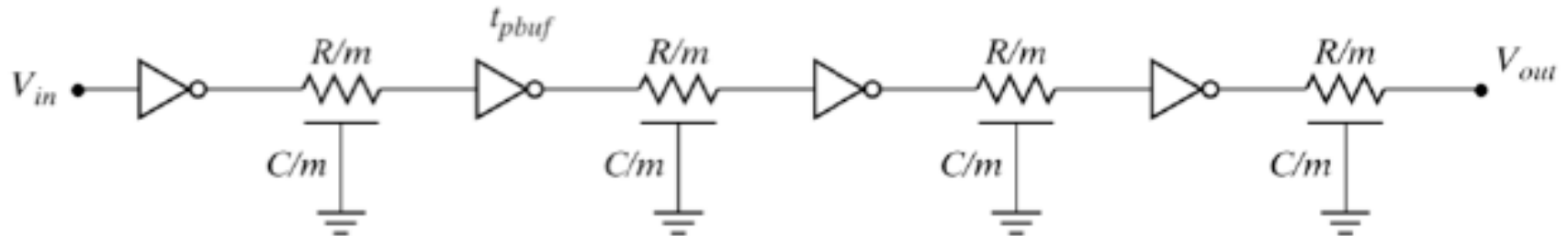
$$R = \rho \frac{l}{t \cdot w}$$

$$C = \epsilon \frac{t \cdot l}{s}$$

$$\text{Delay} \propto RC \propto l^2$$

- Extra

Repeaters



$$t_p = m \left(0.69 \frac{R_d}{s} \left(s\gamma C_d + \frac{cL}{m} + sC_d \right) + 0.69 \left(\frac{rL}{m} \right) (sC_d) + 0.38rc \left(\frac{L}{m} \right)^2 \right)$$

$$m_{opt} = L \sqrt{\frac{0.38rc}{0.69R_dC_d(\gamma + 1)}} = \sqrt{\frac{t_{pwire(unbuffered)}}{t_{p1}}}$$

$$s_{opt} = \sqrt{\frac{R_dc}{rC_d}}$$

Repeater Insertion (Revisited)

Taking the repeater loading into account

$$m_{opt} = L \sqrt{\frac{0.38rc}{0.69R_dC_d(\gamma + 1)}} = \sqrt{\frac{t_{pwire(unbuffered)}}{t_{p1}}}$$

$$s_{opt} = \sqrt{\frac{R_dc}{rC_d}}$$

For a given technology and a given interconnect layer, there exists an optimal length of the wire segments between repeaters. The delay of these wire segments is independent of the routing layer!

$$L_{crit} = \frac{L}{m_{opt}} = \sqrt{\frac{t_{p1}}{0.38rc}} \quad t_{p,crit} = \frac{t_{p,min}}{m_{opt}} = 2 \left(1 + \sqrt{\frac{0.69}{0.38(1 + \gamma)}} \right) t_{p1}$$