BIRZEIT UNIVERSITY

Faculty of Engineering and Technology
Department of Electrical and Computer Engineering

Course Information	
Course Title	**Computer Architecture**
Course Number	ENCS4370
Prerequisites	ENCS2380 | Computer Organization and Microprocessor ENCS336 | Computer Organization and Assembly Language ENCS238 | Computer Organization ENCS2308 | Computer Structure and Organization
Semester	Second Semester 2023 – 2024
Instructors	Ayman Hroub, Aziz Qaroush

Text Book	
Title	**Computer Organization and Design: The Hardware/Software Interface**
Author(s)	John L. Hennessy and David A. Patterson
Publisher	Morgan Kaufmann
Edition	6th Edition (2021)
References	• **Computer Architecture: A Quantitative Approach** John L. Hennessy and David A. Patterson, Morgan Kaufmann,6th Edition, 2019 • Modern Processor Design: Fundamentals of Superscalar Processors. John Paul Shen and Mikko H. Lipasti, McGraw-Hill, 2012.

Course Objectives

- To understand performance measures used in computer design, technology and cost trends in computer design, quantitative principles of computer performance measures designers use.
- To understand the principles of instruction set design, recent instruction set architecture, study the statistics of the use of memory addressing modes in programs executing on a recent instruction set architecture, statistics of the types and sizes of operands used by programs executing on a recent instruction set architecture.
- To understand basic and advanced pipelining techniques, basic methods for handling data, control, and resource hazards in single-pipeline processors, analyze instruction-level parallelism (e.g., loop unrolling and detailed aspects of instruction dependence), dynamic scheduling, dynamic branch prediction, performance of pipelines incorporating multiple-instruction issue, limitation of Instruction-Level Parallelism and multithreading.
- To understand the aspects of memory hierarchy and cache design, cache timing and use that information in analyzing overall computer performance, implementation details of advanced cache features (e.g., write buffers, prefetch buffers, out-of-order fetches). analyze cache and TLB interaction and timing
- To understand the aspects Storage and I/O Systems: Types of Storage Devices, Buses, I/O Performance Measures, Memory Interface, Designing an I/O System.
- Be able to analyze and use techniques that guarantee cache coherence and correct sequential memory access across multiprocessor systems.

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Assessment Policy		
Assessment Type	**Expected Due Date**	**Weight**
Quizzes	TBA	10%
Midterm Exam	TBA	25%
Final Exam	TBA	40%
Two Projects	TBA	25%

Course Schedule			
Topics		**#Lectures**	**Materials**
Introduction		1	T.B Ch. #1
Instructions Set Principles and Architecture	• Basic Concepts • MIPS Architecture	2	T.B Ch. #2
MIPS32 Assembly Language Programming	• Introduction to Assembly Language • Arithmetic Instructions • Control Flow Instructions • Load/Store Instructions • Floating Points Instructions	2	T.B Ch. #2
Performance	• Benchmarks • Analysis (CPU execution time) • Amdal's Law	2	T.B Ch. #4 + R.B Ch. #1
CPU Organization & Design	• CPU Organization – Data path and Control • Single cycle scheme • Multi-Cycle scheme • Pipelining scheme	7	T.B Ch. #5
Instruction-Level Parallelism & Superscalar Processors	• Dynamic scheduling • Hardware-Based Speculation • Dynamic Branch Prediction • Superscalar Processors • Multiple Issue Processors	6	R.B Ch. #2
Memory Hierarchy & Cache Design	• Basics of memory hierarchy and caches • Main Memory • Measuring and improving cache performance • Parallelisms and memory hierarchy • Virtual memory	7	T.B Ch. #5 + R.B Ch. #5
Storage & I/O Systems	Disk structure, Interfacing, RAID Systems Measuring I/O Performance	If time allows	T.B Ch. #6 R.B Ch #6

Teaching and Learning Methods
Lectures, assignments, projects, in-class activities and exams.

Additional Notes	
Assignments	No late assignments
Exams	Comprehensive exams
Makeup Exams	**No makeup exam**
Drop Date	TBA
Attendance	Your attendances is very important
Key to a good grade	Reading the **TEXTBOOK and HANDOUT + DOING the PROJECTS**

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