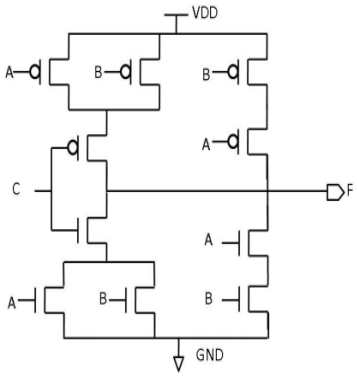
B. What is the logic function of the circuit shown below? Is this a static logic gate? Why or why not? (3 points)



Solution:

$$PDN = \overline{AB + C(B + A)}$$

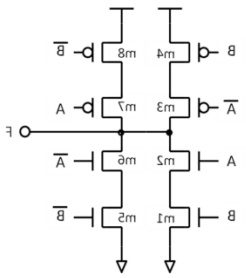
$$\left(PUN = \overline{AB} + \overline{C}(\overline{A} + \overline{B}) = \overline{A} + \overline{B} + \overline{C} + \overline{AB} = \overline{(A + B)C(AB)} = \overline{AB + C(B + A)}\right)$$

$$F = \overline{AB + C(B + A)}$$
$$= \overline{AB + BC + CA}$$
$$= \overline{AB + C(B + A)}$$
$$= \overline{AB} + \overline{C}(\overline{A} + \overline{B})$$

$$F = \overline{AB + BC + CA} = \overline{AB + C(B + A)}$$

Yes. It is a static gate because the output is always connected to a low impedance path to VDD or GND.

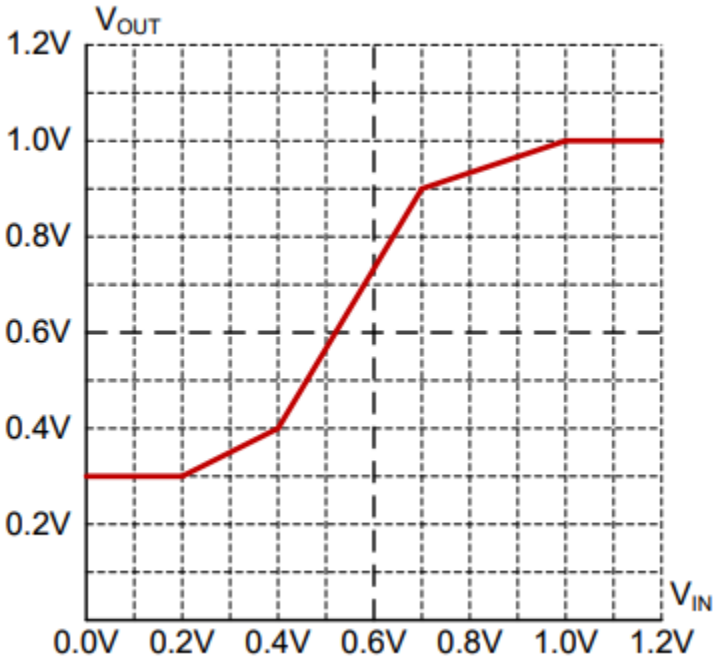
C. Draw the true table and determine the logic function of the complex gate shown below (3 points)



A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

This is an XOR gate

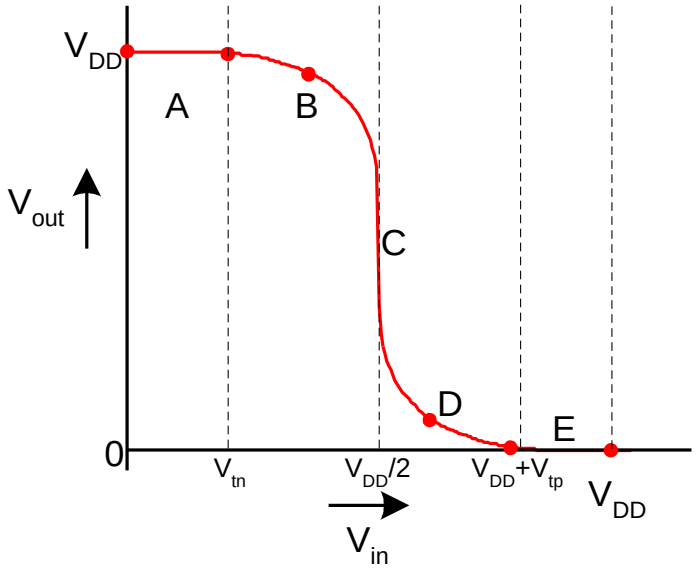
D. Simulation below is for Digital CMOS buffer VTC (3 points)



Compute V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, and NM_H.

(i) VIL = 0.4V (ii) VIH = 0.7V (iii)VOL = 0.3V (iv)VOH = 1.0V (v) NML = 0.1V (vi)NMH = 0.3V NML = VIL - VOL = 0.1V NMH = VOH - VIH = 0.3V

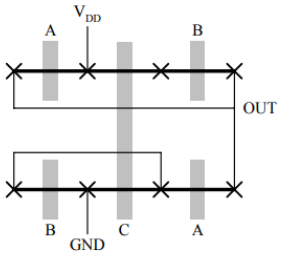
E. Transistor operating regions: Fill the table based on the figure below for each region (3 points)



Region	nMOS	pMOS
A	Cutoff	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff

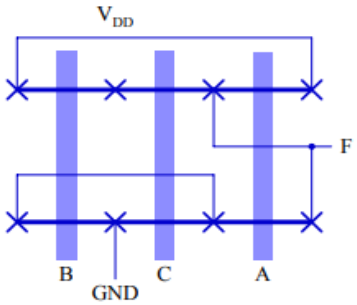
Question 3: (12 POINTS)

F. Write out the truth table that corresponds to the following stick diagram (3 Points)



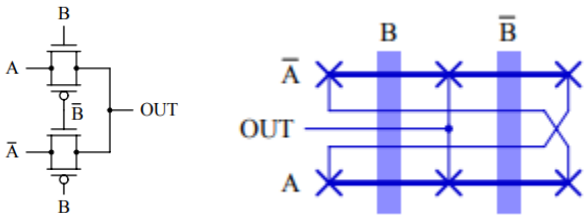
A	B	C	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

A. Implement F = $\overline{AB+AC}$ using stick diagram. Each gate must be used for both PMOS and NMOS. Use static CMOS. Clearly denote if crossing wires are connected or not. **Use the fewest number of transistors possible**. (4 pts)



$F = \overline{A(B+C)}$

B. Implement the following circuit in stick diagram. Assume all inputs are given and do not break the diffusion. (4 pts)



Question 4: (13 POINTS)

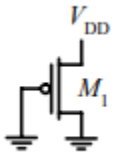
C. What is the effect of Increasing temperature on (4 Points)

A. Mobility → Reduces mobility
B. Vt → Reduces V_t

C. I_{ON} → **decrease**s with temperature
D. I_{OFF} → **increase**s with temperature

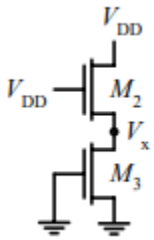
D. Determine the region of operation (Off, Linear, Saturation) in the following configurations. You may assume that all transistors are short-channel devices and have identical sizes, VDD = 2.5V. Assume following transistor parameters: Explain your reasoning and show your derivations if needed (6 Points)

NMOS: $V_{Tn} = 0.4V$, $k_n = 115\mu A/V^2$, $V_{DSATn} = 0.6V$, $\lambda = 0$, $\gamma = 0.4V^{1/2}$, $2\Phi_F = -0.6V$
PMOS: $V_{Tp} = -0.4V$, $kp = -30\mu A/V^2$, $V_{DSATp} = -1V$, $\lambda = 0$, $\gamma = -0.4V^{1/2}$, $2\Phi_F = 0.6V$



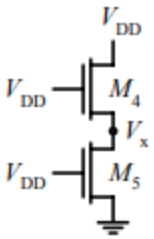
$V_{GS1} = V_{DS1} = -2.5V$

$|V_{DSAT1}| < |V_{GT1}| < |V_{DS1}| \Rightarrow$ **M_1 velocity saturation**



$V_{GS3} = 0 < V_{T3} \Rightarrow$ **M_3 off**

$V_x = V_{DD} - V_{T2} \Rightarrow$ **M_2 off**



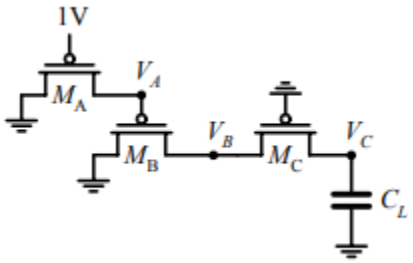
$V_{T4} > V_{T5}$ (body effect) $\Rightarrow V_{DS5} < V_{GT5} \Rightarrow$ **M_5 linear** (

Assume M_4 **vel sat** and ignore body effect in the first iteratio

$$(V_{DD} - V_{T4}) \cdot V_x - \frac{V_x^2}{2} = (V_{DD} - V_x - V_{T5}) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2}$$

$V_x = 0.435V \Rightarrow$ **M_4 velocity saturation** (

E. For the circuit in below determine the final value of VA, VB, VC, assuming initial condition at each of the nodes is 3V and VTP = −0.5V. (3 pts)



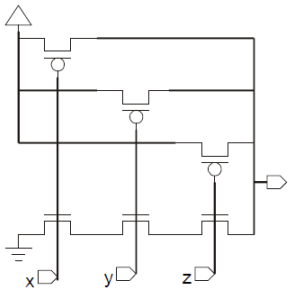
No current flows into the gate ⇒ IDA = 0 ⇒ VA = VGA – VTA = 1.5V

Since VA < initial VB, MB is also off ⇒ VB = VA – VTB = 2V

Finally, MC passes logic “1” to the output ⇒ VC = 2V

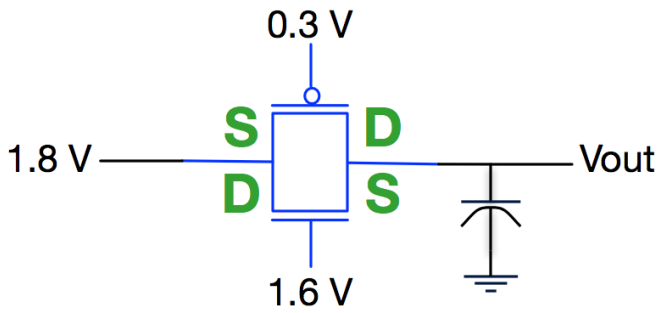
Question 2 (10 pts)

A. what function does this below circuit represent? **(2 pts)**



ANSWER: **3-INPUT -NAND**

B. In this transmission gate, Vout is initially discharged to 0 Volts. Given: V_{tN} = 0.5V, V_{tP} = -0.6V. Mark in the designated boxes the source and drain for each device **(2 pts)**



C. arrange the terms VOHmin, VIHmin, VILmax and VOLmax, and arrange them from lowest value to highest value. **(2 pts)**

$$V_{OLmax} \leq V_{ILmax} \leq V_{IHmin} \leq V_{OHmin}$$

D. Answer the following questions based on the circuit shown . **(4 pts)**

a) If Vx = 0V, what logic function is implemented?

ANSWER: **INV**

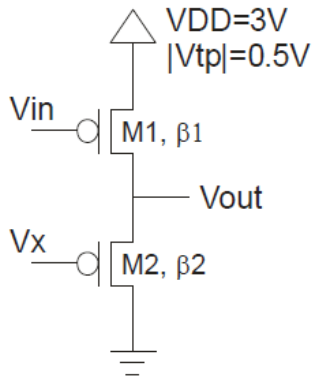
b) What is V_{OL} if Vx = 0V?

ANSWER: V_{OL} = **0.5 V**

C) How can this circuit be modified to maximize the output voltage swing (i.e., get V_{OH} close to 3V and V_{OL} close to ground)? Explain briefly
i) in terms of size parameter (W, L) for transistors M1 and/or M2?
V_{OL} = |Vtp|, can not be changed
V_{OH} can be raised by decreasing the W/L ratio of M2 or increasing W/L of M1

ii) Are there any other circuit parameters that can be modified to improve output voltage swing?

Increasing Vx (> 0V) will make current in M2 weaker and allow V_{OH} to go higher.



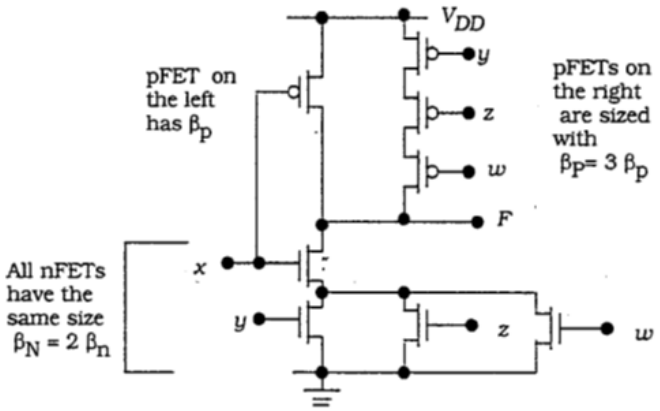
Question 3 (10 pts)

Transmission gates circuits used extensively in CMOS, good switch, can pass full range of voltage (VDD-ground)

A. How does the Pass gate Formed ? how do you connect the nMOS and pMOS to form a pass gate ? ***(1 pts)***

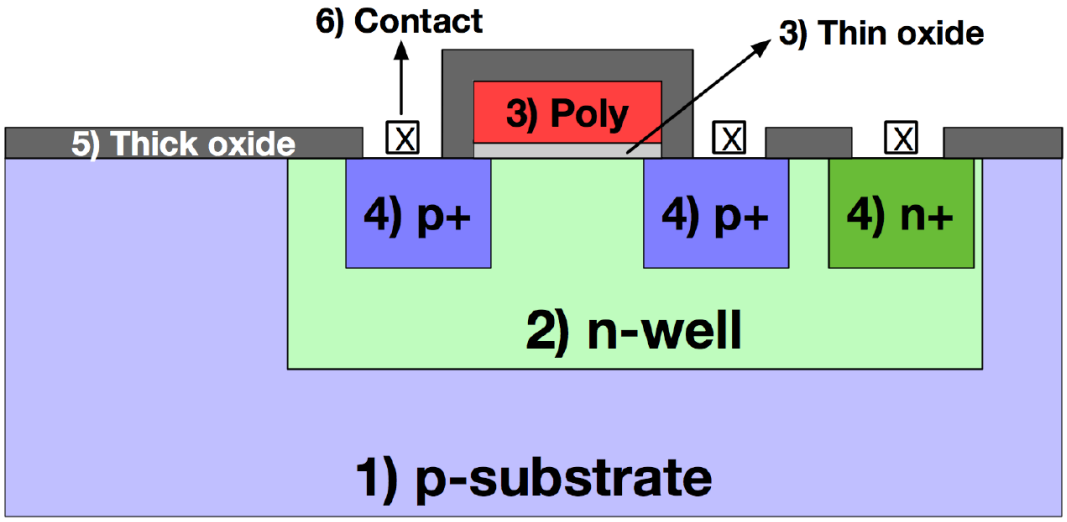
by a parallel nMOS and pMOS

B. Given the circuit as shown below, size the device assuming an inverter sizes are Bn for NMOS device size and Bp for PMOS size. ***(4 pts)***



C. List the steps required for creating a PMOS transistor, and draw a cross-section of the PMOS transistor, labeling each layer/feature in the order fabricated. **(5 pts)**

The steps below assume that a p-type substrate and positive photoresist is used.
1. Expose the substrate to oxygen (and hydrogen) at very high temperatures to form silicon dioxide
(SiO_2) layer. This is thick oxide.
2. Deposit photoresist.
3. Cover the photoresist with a mask which exposes those areas where n-well is to be created.
4. Expose to UV light.
5. Remove the exposed photoresist by dissolving.
6. Etch the surface to remove the portions of SiO_2 not covered by photoresist.
7. Strip off remaining photoresist.
8. Use *n* ion implantation to form n-wells in the areas without SiO_2.
9. Cover the whole surface with thin oxide and polysilicon.
10. Selectively remove thin oxide and poly from everywhere except for transistor gates.
11. Use *p+* ion implantation to form sources and drains of PMOS transistors.
12. Use *n+* ion implantation to form ntaps.
13. Cover the whole surface with thick oxide.
14. Selectively remove thick oxide from the source, drain and body (n-tap). This forms contact cuts.



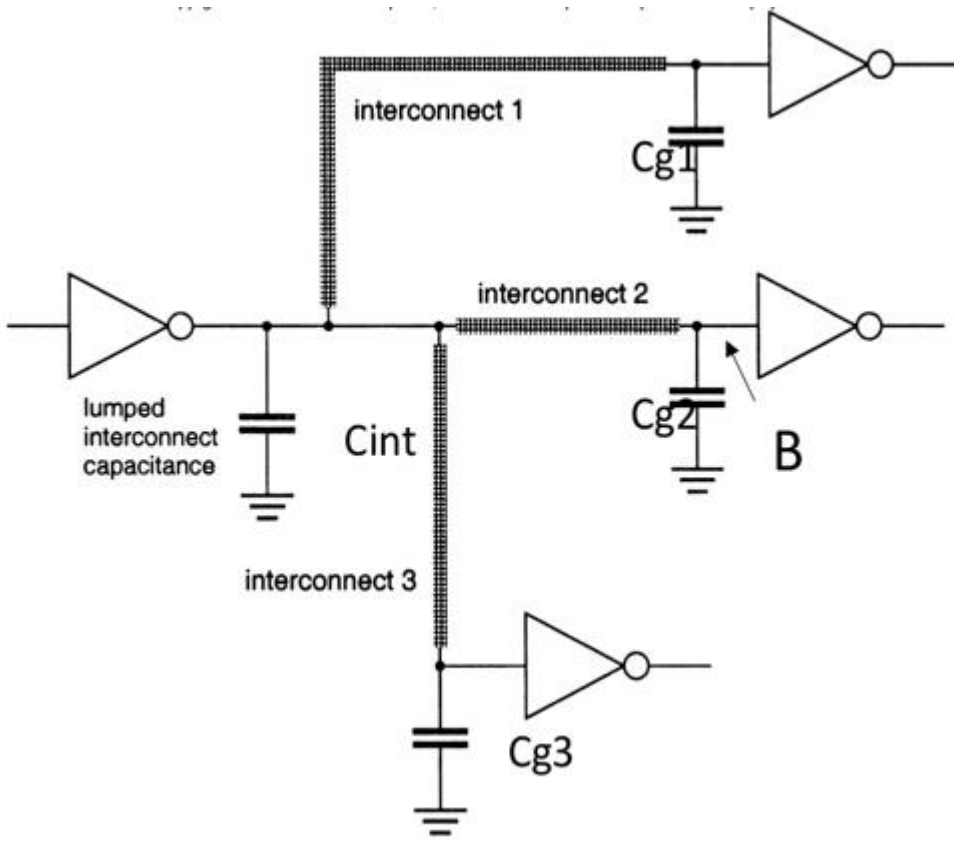
Question 4: ***(10 pts)***

A) Where do we find thin oxide in a CMOS circuit? Why don't we use thick oxide? ***(3 pts)***

Thin oxide is found under the polysilicon gate regions of any transistor.
Since its thickness is small, gate capacitance is higher. This allows better charge attraction to quickly form the inversion channel between source and drain.

B) Compute the worst-case rising and falling RC time constants at point B of the circuit below using the Elmore delay method. Assume all transistors **are unit sized** and wire **capacitance is lumped**. ***(7 pts)***

Assume **Rchn** = 2000 ohms. **Rchp** = 8604 ohms, Cg(n+p) = 20 ff, Cd(n+p) = 20ff, and Cint = 10 ff. Rint for interconnect1 is 10 ohms, interconnect2 is 5 ohms, and interconnect3 is 7 ohms.
Hint: Note that interconnect **capacitance is lumped at the beginning**, so we don't need to consider it separately for the 3 wires



Recall that channel resistance is inversely proportional to beta. So:

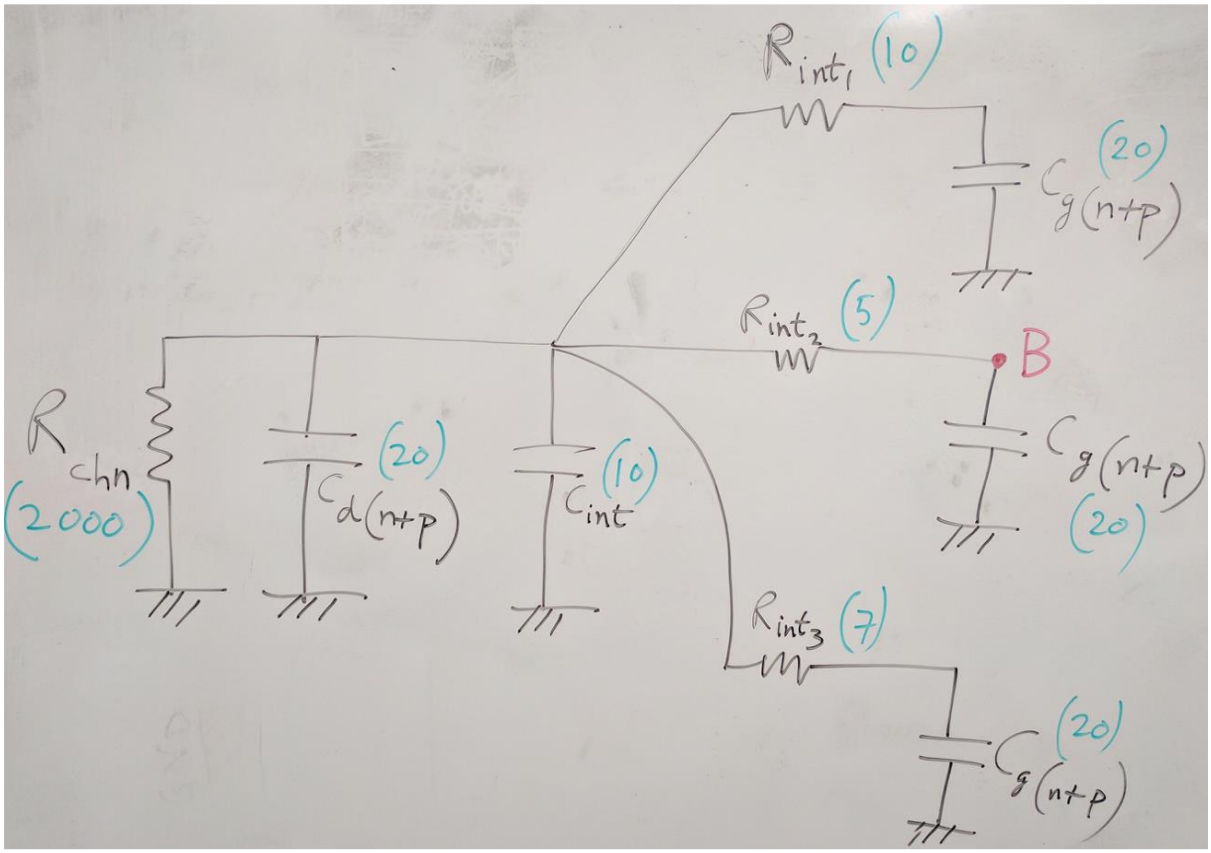
$$\frac{R_{chp}}{R_{chn}} = \frac{\beta_n}{\beta_p}$$

Note that interconnect **capacitance is lumped at the beginning**, so we don't need to consider it separately for the 3 wires.
Following is the circuit for falling delay at B:

Falling Elmore delay at B = $2000 \times 20 + 10 + 20 + 20 + 20 + 5 \times 20 = \mathbf{0.1801\ ns}$

For rising delay at B, the circuit is the same except that Rchn is replaced with Rchp and the leftmost Gnd
symbol is replaced with Vdd.

Rising Elmore delay at B = $8604 \times 20 + 10 + 20 + 20 + 20 + 5 \times 20 = \mathbf{0.77446\ ns}$

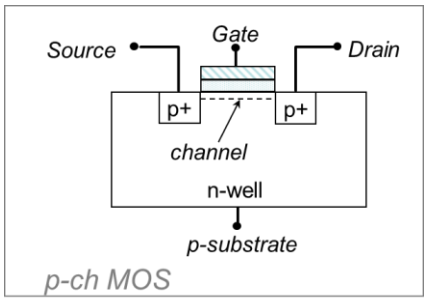


Question 1 [30 points]

1. **Select True or False for each point below** ALL T **[20 marks]**

- (T/F) Transmission gates are needed to pass both 0 and 1
- (T/F) nMOS pass transistors pull no higher than V_{DD}-V_{tn}
- (T/F) Process can be defined as – a sequence of steps used to form circuits on a wafer
- (T/F) Field Oxide used for Isolation between devices
- (T/F) We have Design Rules because the fabrication process has minimum/maximum feature sizes that can be produced for each layer
- (T/F) Poly or gate materials have a high-resistance conductor (can be used for short routing)
- (T/F) Nwell and Substrate must be connected to the power supply within each cell
- (T/F) If we now want to create an n-type channel below the Si-SiO_2 surface we need to increase V_{GS}. As V_{GS} is increased the Si close to the surface first becomes depleted of holes and only then (at higher V_{GS}) electrons start to build the channel.
- (T/F) We can define the 'threshold voltage' as the V_{GS} that below it the transistor's current (I_{DS}) effectively drops to zero
- (T/F) *Transistor's current saturates at high Vds values.*

2. **Draw the cross section of the PMOS Device** **[4 marks]**



3. **What are the major 4-steps in CMOS process technology? Briefly explain what each step function is?** **[6 marks]**

- Oxidation – build oxide layer for isolation or for gate
- Lithography – determine area for active, gate, .. etc
- Etch – etch away (remove) unwanted materials
- Implant – add doping to Si through CVD or by heat.

Question 2 [25 points]

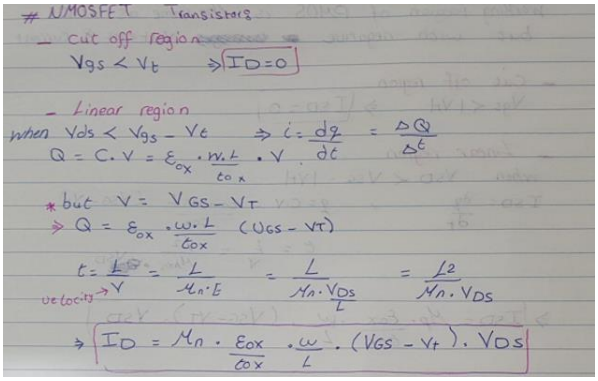
1. What are the main three modes of operation (region) of the transistor? And how can we model the transistor in each region? **[6 marks]**

   Cut off → open

   Linear → Ron

   Saturation → current source

2. Derive or find the Ron Equation for the NMOS transistor? **[6 marks]**



R = VDS/IDS = 1/ un …… etc

3. What is the effect of temperature on mobility, threshold voltage, and leakage current? **[4 marks]**

   Solution: Increase temp -> decrease mobility, increase vt, increase Vt

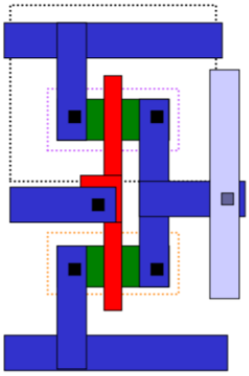
4. Hot-e degradation happens for which type of transistor OMOS/NMOS ? Why ? **[4 marks]**

NMOS

- When a MOS transistor is in saturation, the electric field across the pinch-off region may be high enough that carriers gain there enough energy to excite electron-hole pairs.

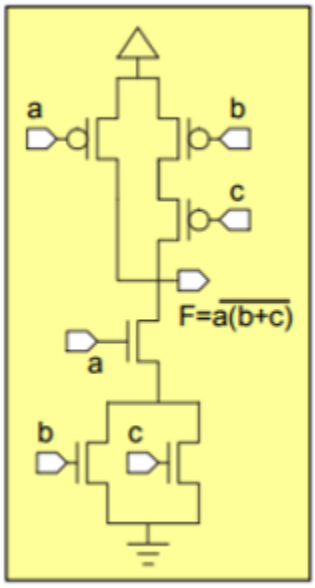
5. Given the layout shown below: **[10 marks]**

a. What function does this layout implement? Inverter [1 mark]
b. Draw the schematic view of the circuit. [3 marks]
c. Write/list all masks used in this layout.? Nwell/p+/n+/poly/metal1, metal2, via, metl1 contact/poly head(contact) [4 marks]

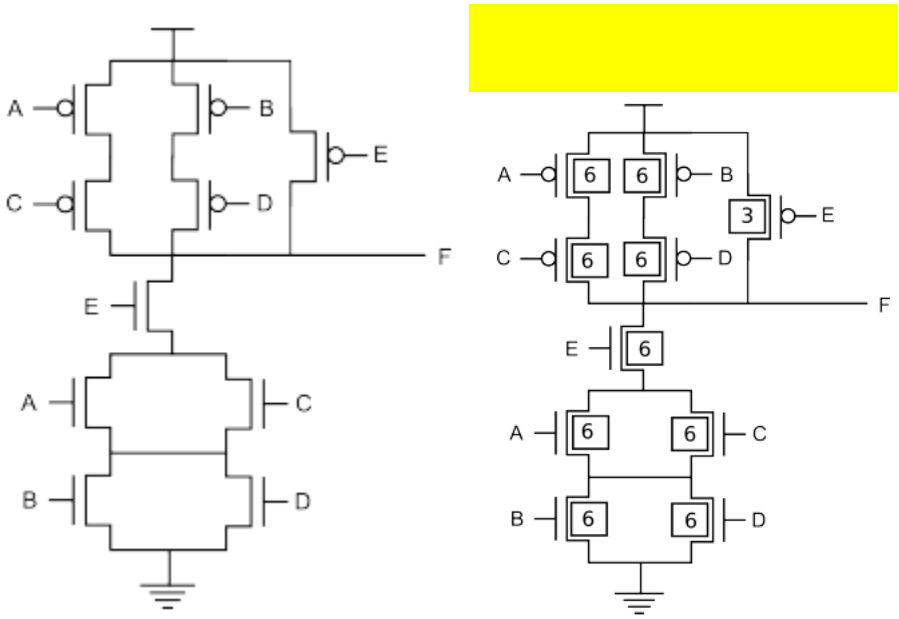


Question 3 [40 points]

1. **Draw the schematic with a minimum number of devices for** $F = \overline{a \cdot (b + c)}$ **[10 marks]**



2. **For the circuit shown below**
   a. **What is the function: F=[E.(A+C).(B+D)]'** **[2 marks]**
   b. **Size the transistors in the circuit on the right so that the current through any single path in the P and N network is the same as that of an inverter with widths of P=3, N=2.** **[10 marks]**



3. Given three differences ways to design inverter. Match the right VTC curve to the right figure for each one. **[8 marks]**

Fig. A

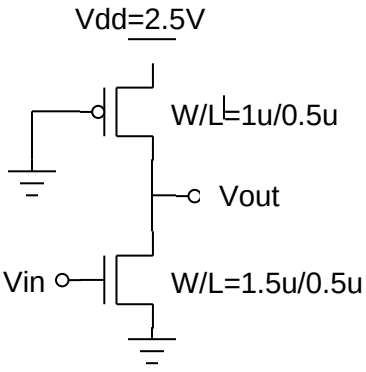


Fig. B

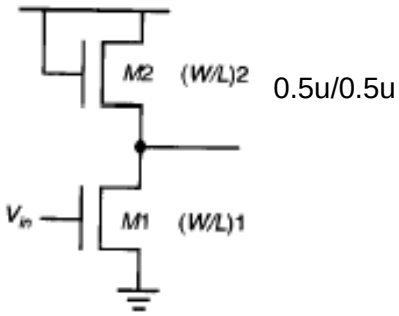
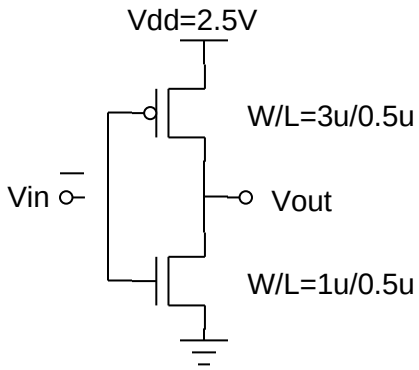
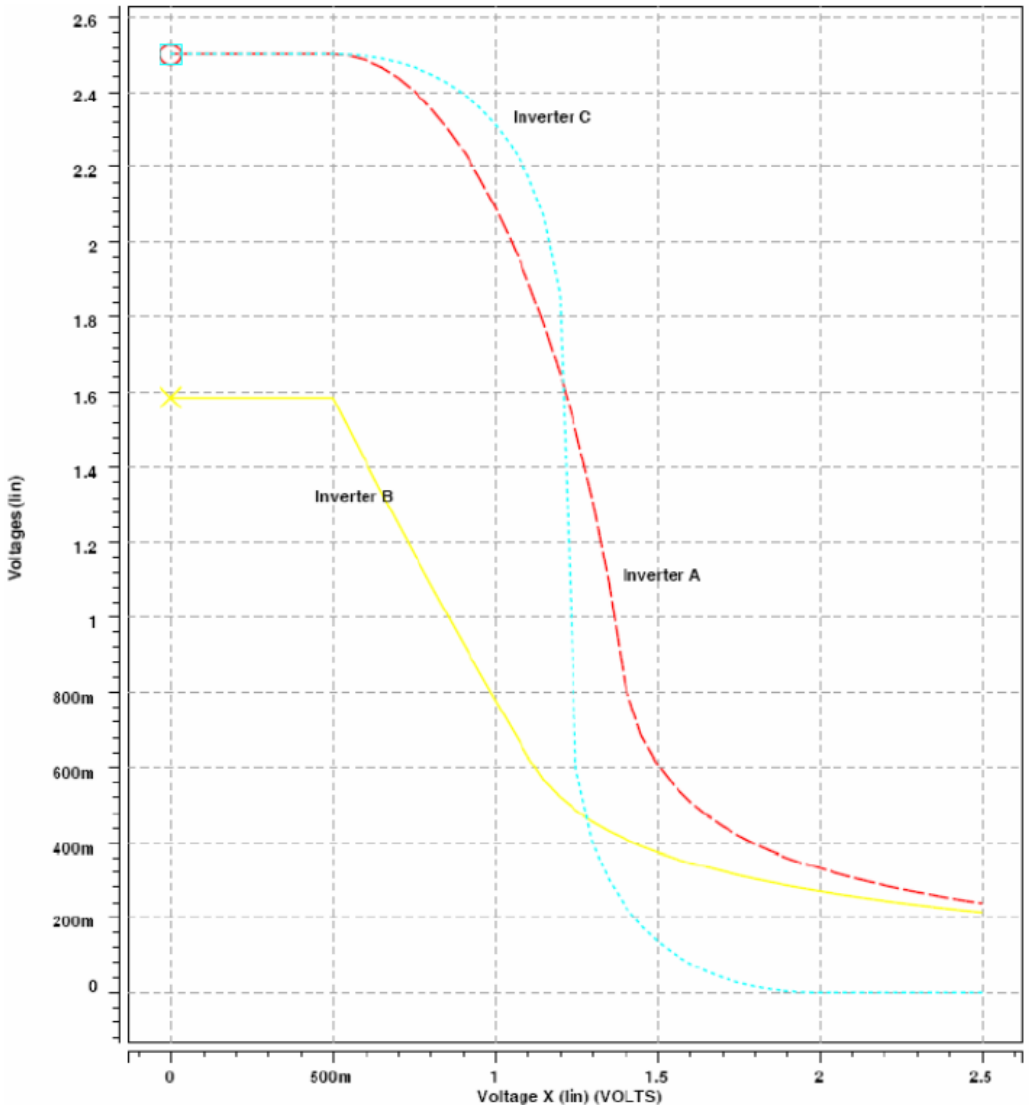
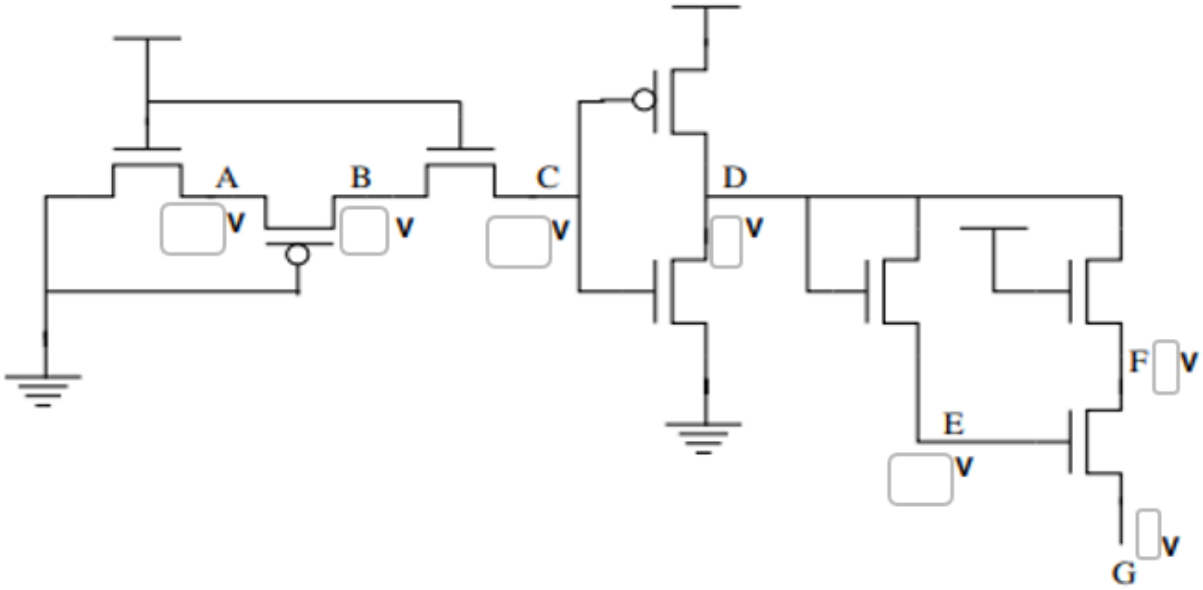


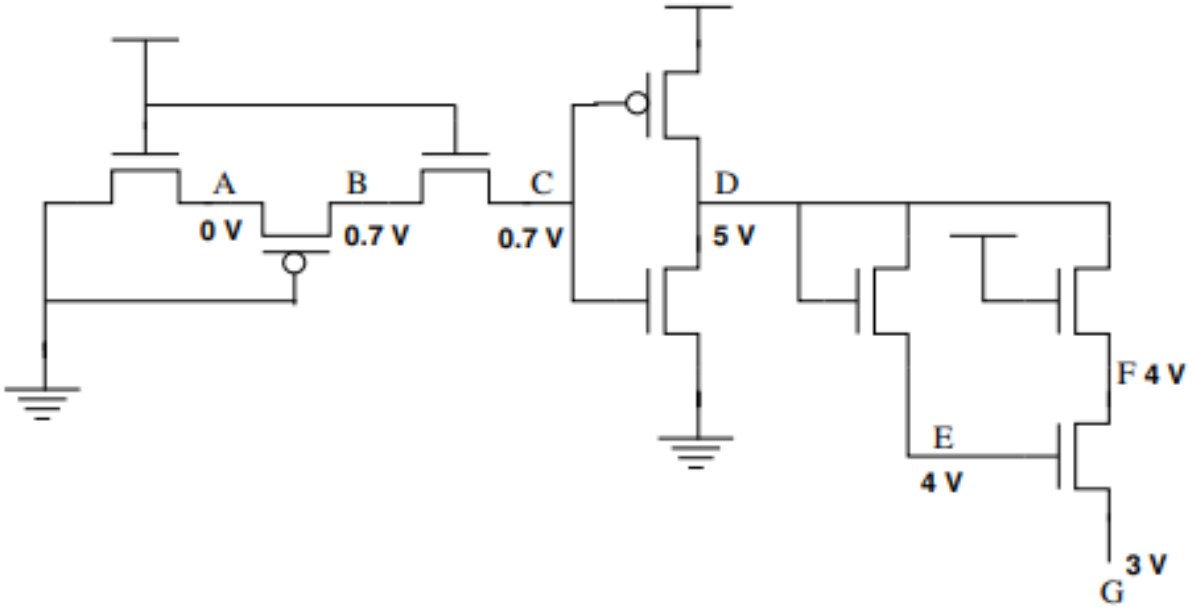
Fig. C





4. Write down the voltages at A, B, C, D, E, F, G in the following circuits, assuming that the initial voltage on each node is 2.5 volts. The relevant transistor parameters are, Vdd = 5V , Vtn = 1V and |Vtp| = 0.7V . **[10 marks]**





Problem 2: (20 pts)

A. Consider an N-channel MOSFET. You may assume that this MOSFET has no oxide charge. Fill in the blank cells in the table, using the following symbols: ↑ for increase, ↓ for decrease, and → for no change. If the cell has already been provided with an X it means that you are not responsible for filling that cell out. When moving along a row consider only the change brought on due to the parameter specified in the first cell of that row. **(7 pts)**

	V_t	V_{FB}	μ_s	I_{ds}
T_{ox} ↑	increase	No change	***Assume V_t is unchanged*** increase	***Assume μ_s remains unchanged*** decreas
Temperature ↑	**X**	decreas	decrease	**Assume V_t is constant and** decrease

B. Answer the following Questions about the figure shown below : **(13 pts)**

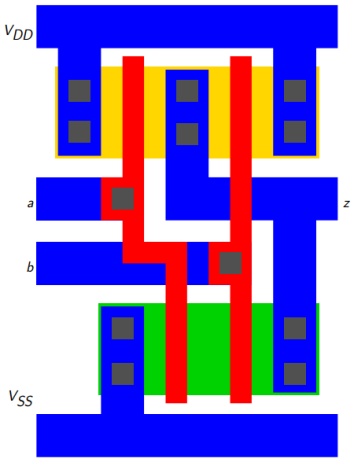
a. What does this layout represent ? _____

b. How many contacts does it Have ? _____

c. How Many Poly head/contact it has ? _____

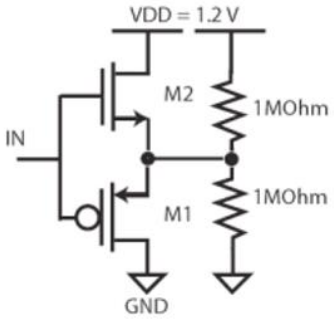
d. Mark the length(Ln) and the width (wp, wn) of devices on the figure

e. Sketch the equivalent detail schematic and the schematic symbol view.

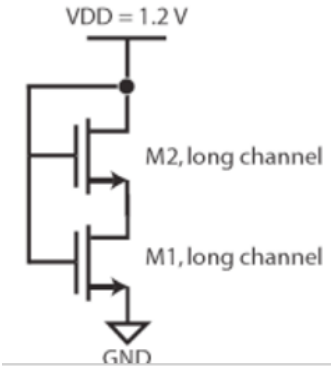


Problem 3: (20 pts)

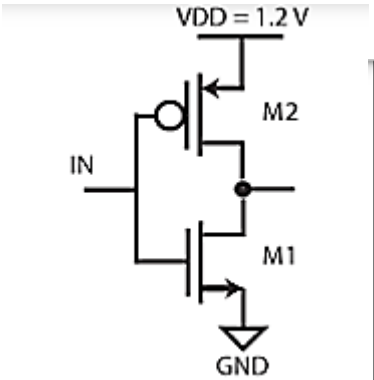
1. Indicate the regions of operation of the transistors shown in the circuits in the tables next to the circuits. Assume short channel devices unless otherwise stated VTn=VTp= 0.3 V, Vvsatn= 0.3 V, Vvsatp= 0.6 V and neglect the body effect. **(10 pts)**



Voltage	Region of Operation	
IN	M1	M2
GND (0 V)	◯cutoff ◯linear ◯saturation	◯cutoff ◯linear ◯saturation
VDD (1.2 V)	◯cutoff ◯linear ◯saturation	◯cutoff ◯linear ◯saturation

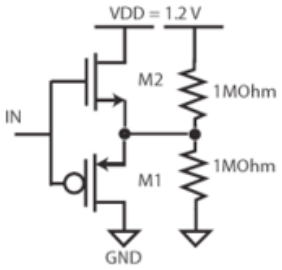


Region of Operation	
M1	M2
◯cutoff ◯linear ◯saturation	◯cutoff ◯linear ◯saturation

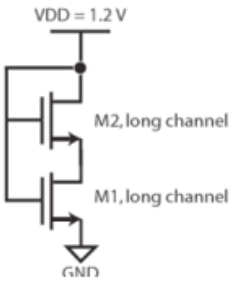


IN	M1	M2
GND (0 V)	◯cutoff ◯linear ◯saturation	◯cutoff ◯linear ◯saturation
VDD (1.2 V)	◯cutoff ◯linear ◯saturation	◯cutoff ◯linear ◯saturation

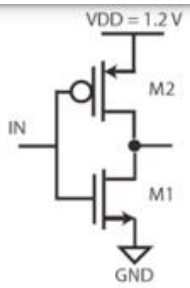
Solutions:



Voltage	Region of Operation	
IN	M1	M2
GND (0 V)	O cutoff O linear X saturation O vel. saturation	X cutoff O linear O saturation O vel. saturation
VDD (1.2 V)	X cutoff O linear O saturation O vel. saturation	O cutoff O linear X saturation O vel. saturation

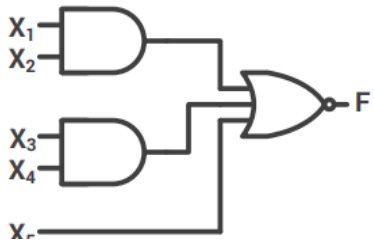


Region of Operation	
M1	M2
O cutoff X linear O saturation	O cutoff O linear X saturation

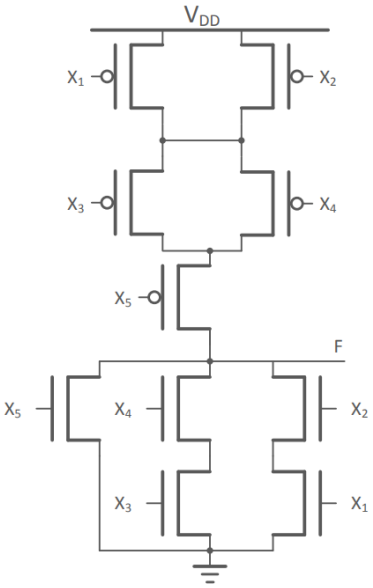


IN	M1	M2
GND (0 V)	X cutoff O linear O saturation O vel. saturation	O cutoff X linear O saturation O vel. saturation
VDD (1.2 V)	O cutoff X linear O saturation O vel. saturation	X cutoff O linear O saturation O vel. saturation

2. Consider the And-OR-Inverter (AOI) cell shown in Figure below. Derive the CMOS complex gate that implements this cell with minimum number of transistors. **(5 pts)**



Solutions:



T1 =$X_1.X_2$

T2 = $X_3.X_4$

Pull-Up Network

F = $(X_1.X_2 + X_3.X_4 + X_5)'$

F = $(X_1'+X_2')\ (X_3'+X_4').X_5'$

F =

$(X_1'X_3'+X_1'X_4'+X_2'X_3'+X_2'X_4')X_5'$

Pull-Down Network

F = $(X_1.X_2) +(X_3.X_4)+X_5'$

3. Consider the layout in Figure below **(5 pts)**

(a) What type of logic function does this layout implement?

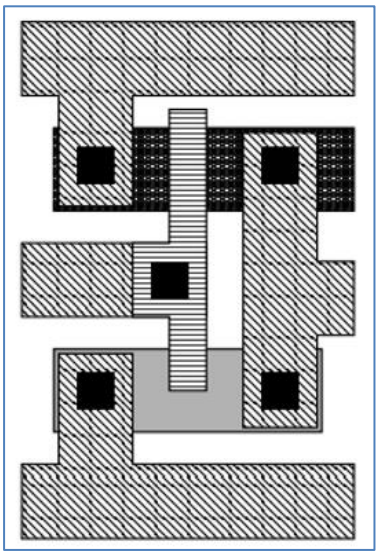
A messed up inverter.

(b) Point out the three largest problems with this layout. For each explain the impact on gate behavior. When possible, indicate the ways in which important parameters are influenced, e.g., k 0 .

i. The bottom half of the NMOSFET gate is missing.

ii. . The PMOSFET drain is bigger than it needs to be, increasing capacitance without benefit.

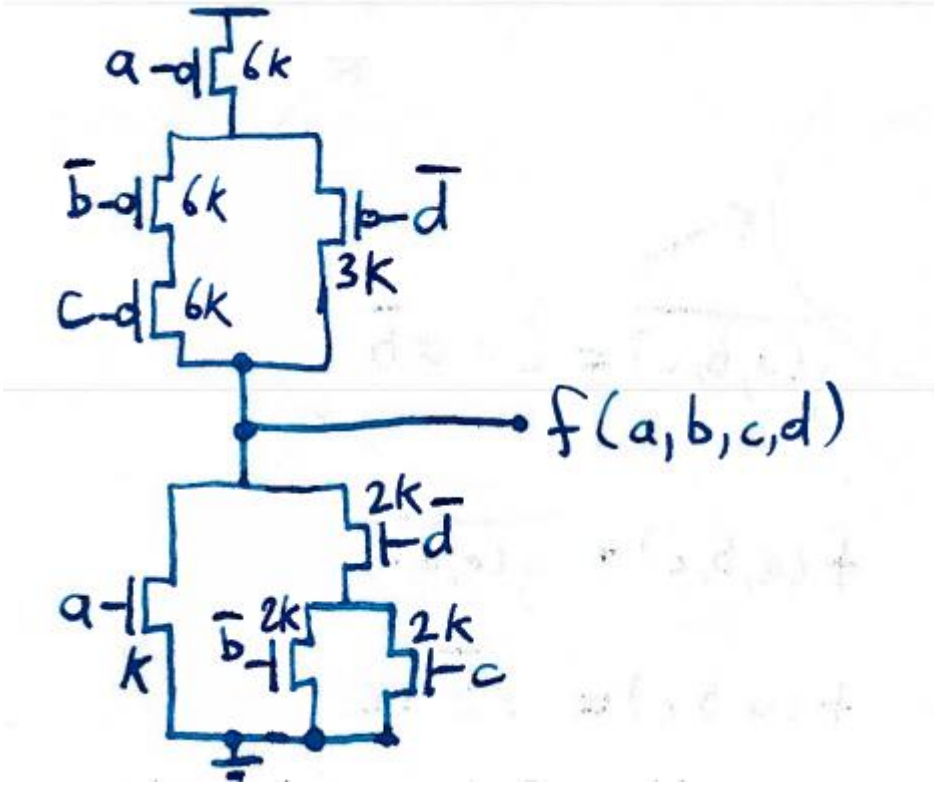
iii. The NMOSFET and PMOSFET active regions are the same width, which would result in asymmetric pull-up and pull-down resistances if the gates were designed correctly.



Problem 3: (15 pts)

1. **Implement the following function as a single logic gate. Indicate the widths of all gates in terms of k, the minimal gate width. Size the transistors to achieve the same worst-case resistance as a balanced, minimal width inverter (i.e., an inverter with a w-wide NMOSFET and a 2k-wide PMOSFET). (5 pts)**

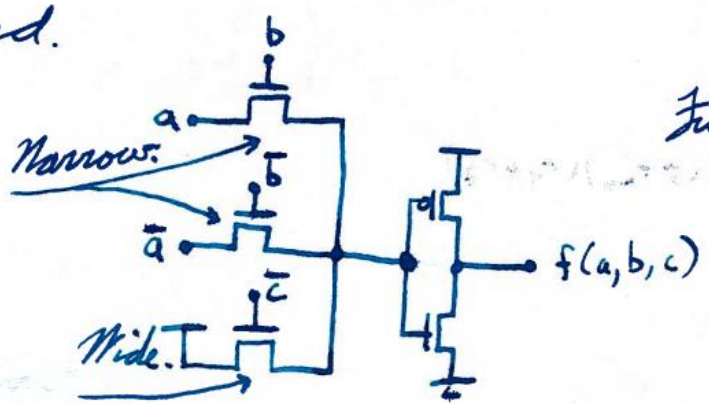
f(a, b, c, d) = a'(bc' + d)



2. **Implement the following function using the minimal number of transistors. The output of your implementation should have full output range, from VSS to VDD. However, it needn't be particularly fast or can have weak signal at some stages. You may use literals as direct inputs. (5 pts)**

f(a, b, c) = (ab' + a'b)c

Most or full credit was given for some designs w. ≤ 8 transistors. However, I wanted to see how far this could be pushed.



Fun, huh?

Question 1 (15)

1- Describe PMOS, NMOS Explain how they work? I am not looking for ON/OFF answers. A discussion of the Vgs.Id curve and region of operation should ensue. **(5points)**

```
If Vds = 0,
  Accumulation   Vgs << Vt
  Depletion      Vgs ~ Vt
  Inversion      Vgs > Vt

If Vds >0,
  Unsaturated    Vgs - Vt > Vds
  Saturation     Vgs - Vt < Vds
  Cutt-off       Current flow is essentially zero.
```

2- How do you evaluate performance of a digital circuit, please name at least three? (3 points)

a. Area/Cost
b. Reliability
c. Scalability
d. Speed (delay, operating frequency)
e. Power dissipation
f. Energy to perform a function

2. ***Yield & Defects : What is the yield and how do we calculated ?*** **(2 points)**

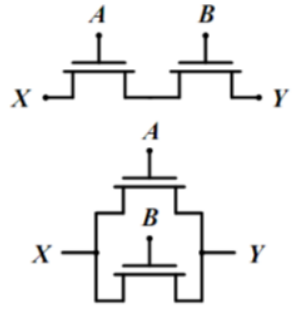
$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

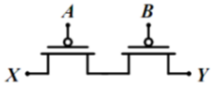
3. What are the three types of power? **(5 points)**

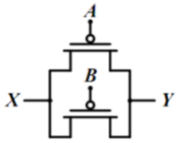
- ***p(t) = v(t)i(t) = Vsupplyi(t)***
- ***Peak power:***
- ***Ppeak = Vsupplyipeak***
- ***Average power:***
- $$P_{ave} = \frac{1}{T}\int_t^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_t^{t+T} i_{supply}(t)dt$$

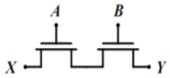
Question 2 (25)

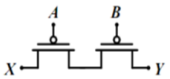
1. ***What type of logic function does these circuit do?*** **(12 points)**

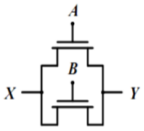


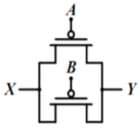




AND  $Y = X$ if A AND B

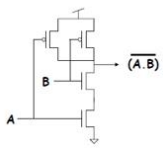
NOR  $Y = X$ if $\overline{A}$ AND $\overline{B} = \overline{A + B}$

OR  $Y = X$ if A OR B

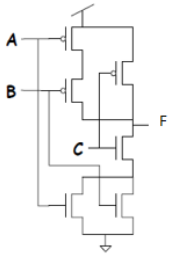
NAND  $Y = X$ if $\overline{A}$ OR $\overline{B} = \overline{AB}$

2. ***Given the truth table below, (8 points)***
   - ***1- Draw the CMOS circuit in transistor level***
   - ***2- Draw the layout stick diagram***

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0



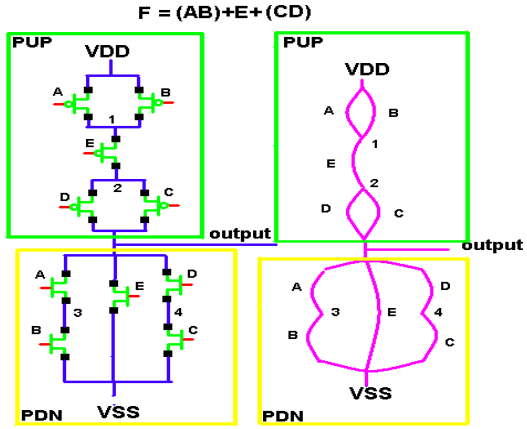
   - ***3- Given a complex gate as shown below, what the function of the circuit?*** **(5 points)**

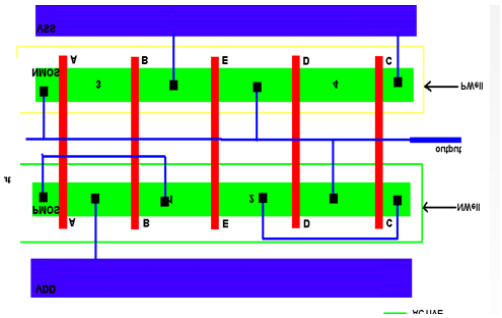


F=((A+B).C}'

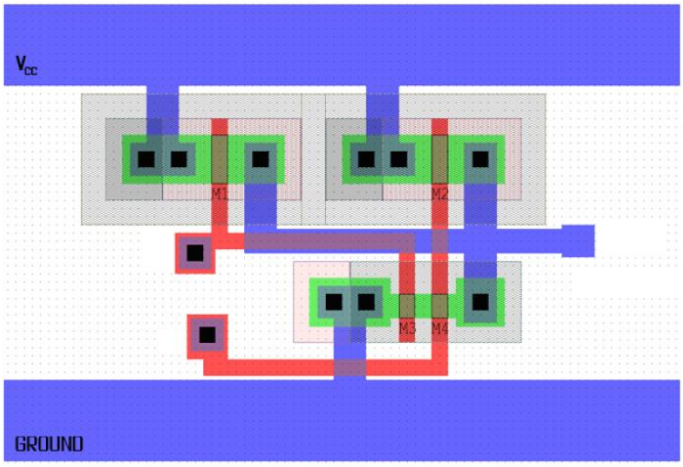
Question 4 (25)

1. ***Draw the CMOS transistor level for this complex Gate and draw the stick diagram for it F=E+(AB)+CD(15 points)***





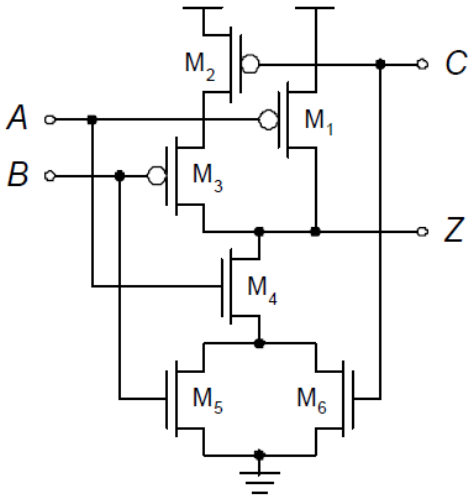
2. ***Consider the following figure below, what type of logic gate is this? Do you think the designer balance the rise and fall time? (10 points)***

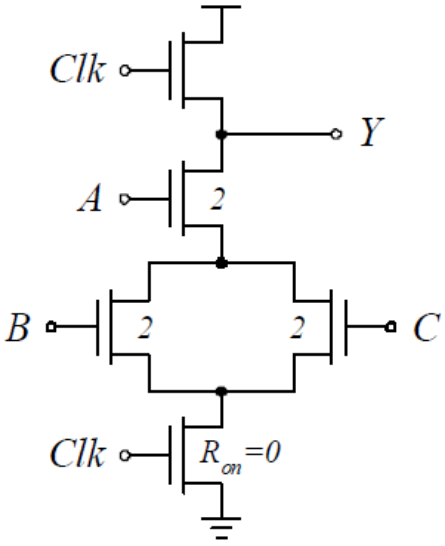


NAND2. The pull-up network has two PMOSFETs in parallel and the pull-down network has two NMOSFETs in series. Interestingly, we can see that the designer didn't balance t_{phl} and t_{plh}.

Question 4 (25)

Draw static and dynamic implementation for F=(C+B).A **(10 points)**



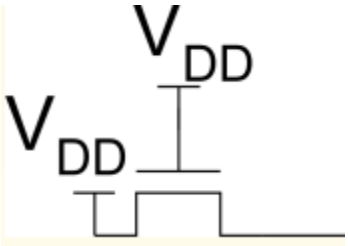


4- What is the output voltage of each of these devices: **(15 points)**

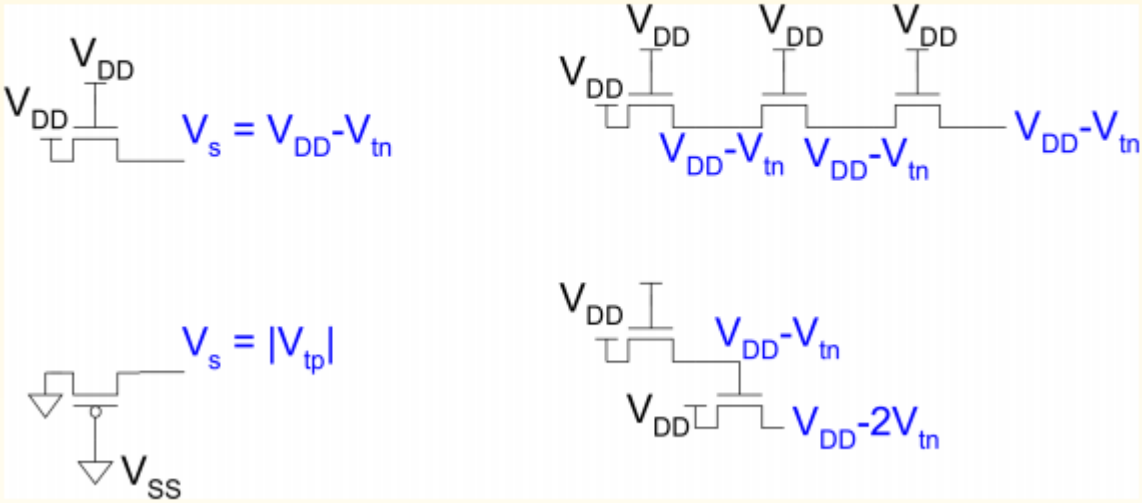
- If Vgd < Vt , channel pinches off near drain when Vds > Vdsat = Vgs – Vt

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{Cutoff} \\ \beta\,(V_{gs} - V_t - V_{ds}/2)\,V_{ds} & V_{ds} < V_{dsat} \quad \text{Linear} \\ \frac{\beta}{2}(V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \quad \text{Saturation} \end{cases}$$

-
- Example, pass transistor passing VDD Vg = VDD If Vs > VDD − Vt, Vgs < Vt Hence, transistor would turn itself of

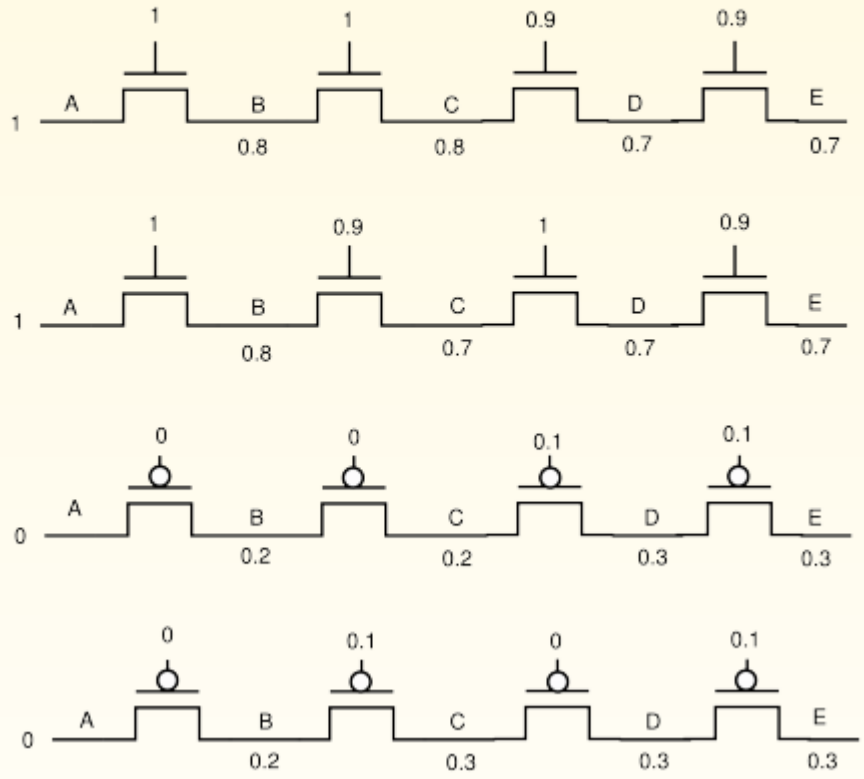


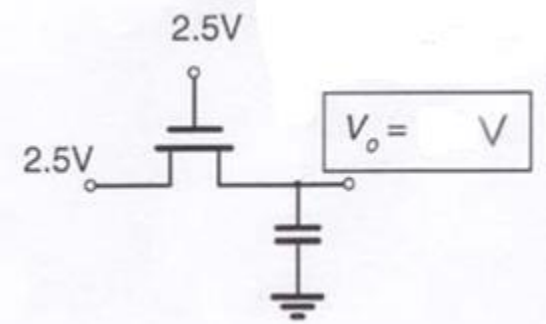
What would be the voltages on the different nodes?

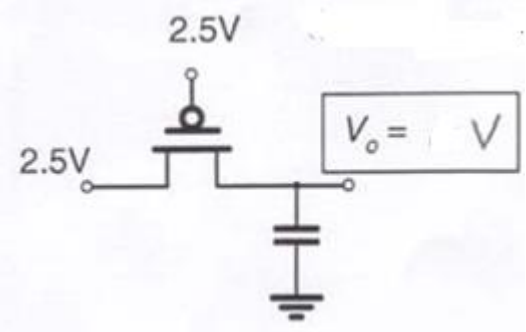


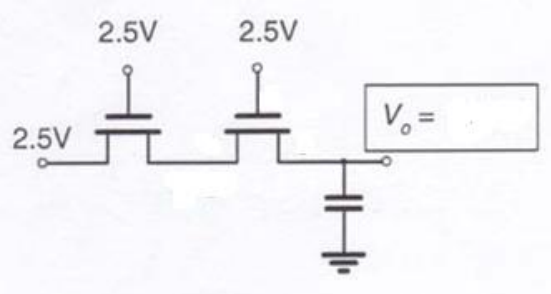
Assume: initial voltage of 0.5V on all the internal nodes

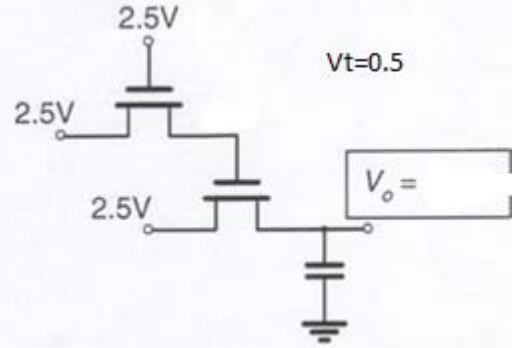
$V_{dd} = 1.0V$, $V_{t_n} = 0.2V$ and $|V_{t_p}| = 0.2V$

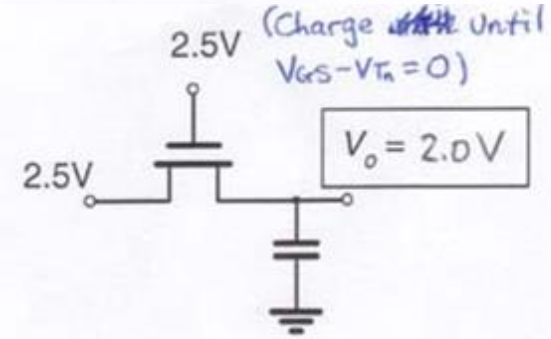


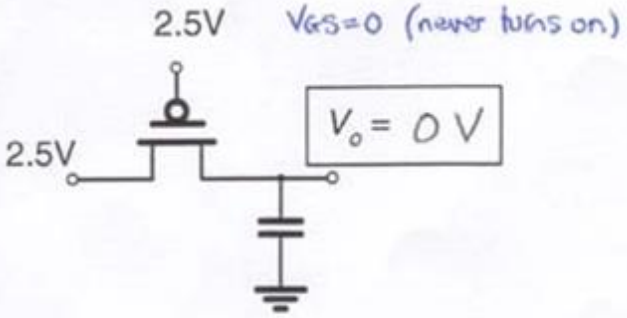


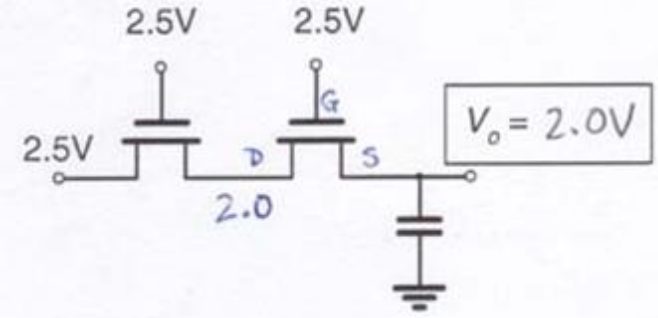


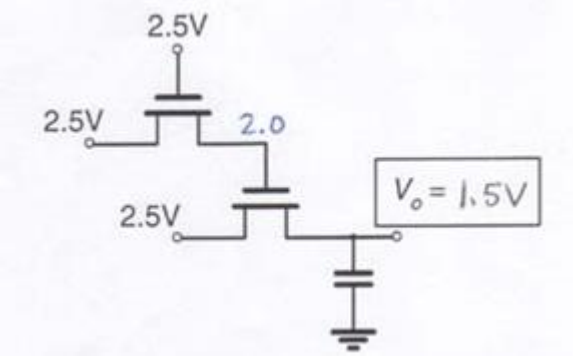






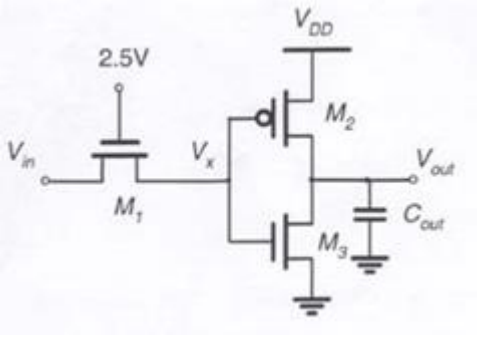






Question 4 (10)

Consider a three trainsitor circuit as shown in figure below. Vdd=2.5V and input signal switch between 0 and Vdd with sharp rise and fall times. All transistor are minimum length l=0.25UM, trainsestor width W2=2um, W1=1um. Note: ignore body effect. Find M3 transistor width such that the switching point of the inverter (Vm) is placed in the middle of Vx signal swing **(10 points)**



$V_{IN} = 2.5V \rightarrow V_{XH} = 2.5 - 0.4 = 2.1V$

$V_{IN} = 0 \rightarrow V_{XL} = 0V$

$$V_m = \frac{V_{XH} - V_{XL}}{2} = 1.05V$$

At $V_{out} = V_m$, $V_{DS} = -1.45V$ for PMOS M_2 and $V_{DS} = 1.05V$ for NMOS M_3, which means both M2 and M3 are velocity Saturated ($V_{DSATP} = -1$, $V_{DSATn} = 0.6$).

We know for the inverter $I_{M2} = I_{M3}$, so we can solve for the width of M3 using the velocity saturated current equations.

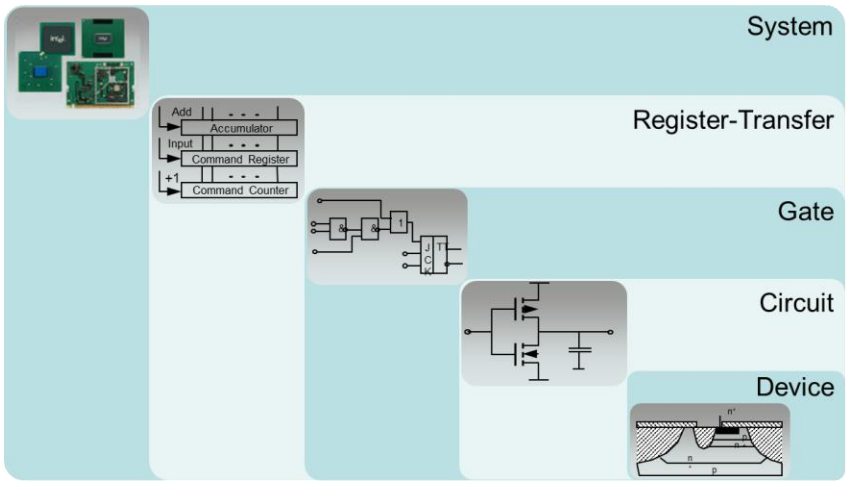
$$\frac{I_{DS3}}{I_{SD2}} = \frac{W_n k_n' V_{DSATn}\left(V_m - V_{tn} - \frac{V_{DSATn}}{2}\right)}{W_p k_p' V_{DSATP}\left((V_{DD} - V_m) + V_{tp} + \frac{V_{DSATP}}{2}\right)} = 1$$

$$\frac{W_p}{W_n} = \frac{k_n' V_{DSATn}\left(V_m - V_{tn} - \frac{V_{DSATn}}{2}\right)}{k_p' V_{DSATP}\left((V_{DD} - V_m) - V_{tp} - \frac{V_{DSATP}}{2}\right)} = 1.46 ; \quad W_n = \frac{W_2}{1.46} \simeq 1.37\,\mu m$$

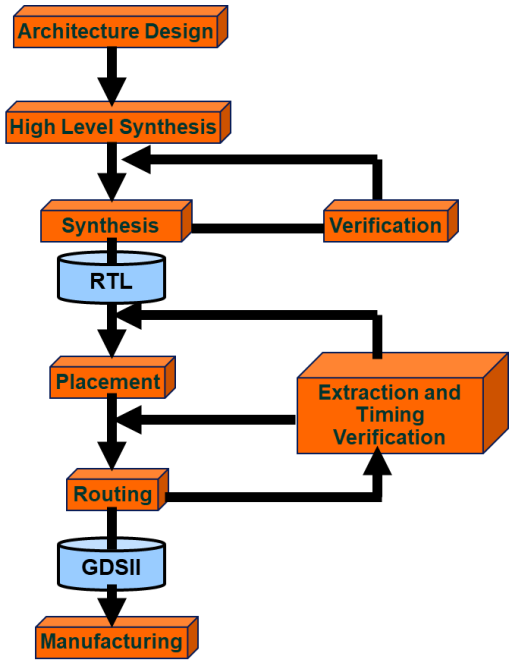
Question	Full Grade	Student Grade	ABET OUTCOME
1	30		
2	20		
3	16		
4	20		
5	30		

Question 1 (30)

1- Describe the flow of the design from specification to manufacturing **(10points)**



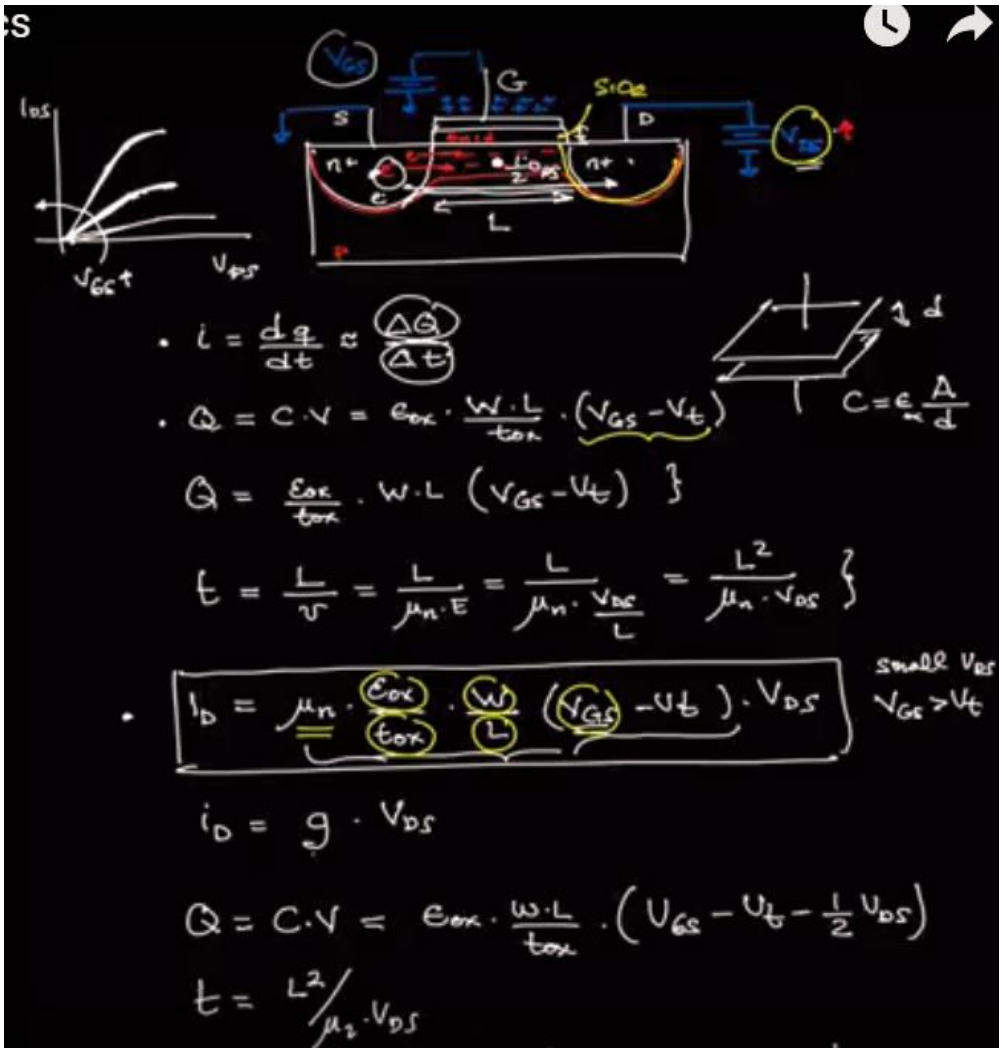
Or

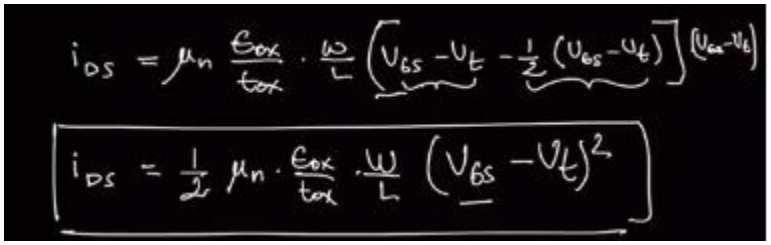


2- Derive the current equation for the NMOS transistor in linear region giving that : **(10 points)**

- Q=CV V=Vgs-Vt I=*dq/dt*

From slides :





3- How do you differentiate between two designs in terms of performance? (5points)

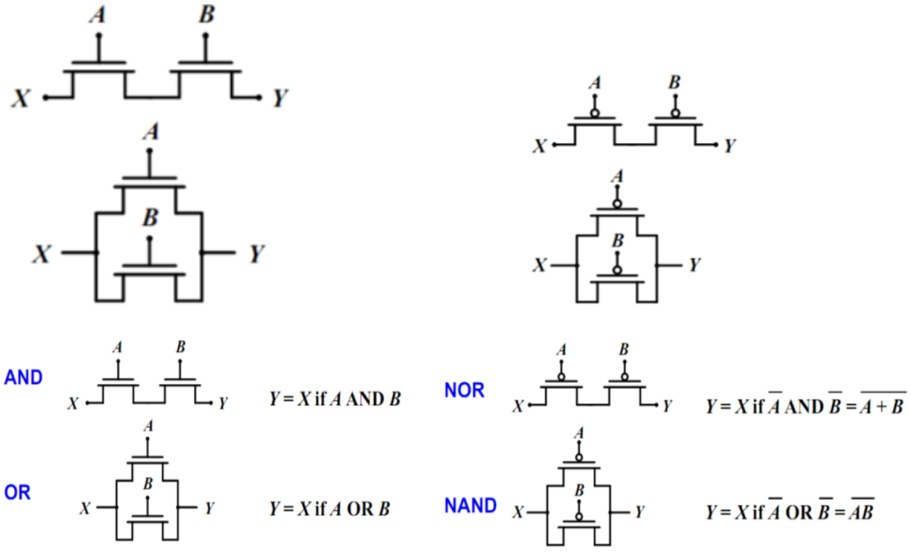
a. Area/Cost
b. Reliability
c. Scalability
d. Speed (delay, operating frequency)
e. Power dissipation
f. Energy to perform a function

2. *What are the main variables/parasitic that affects power dissipations* (5 points)

- ***Voltage? Increases***
- ***Leakage current , increase leakage power , V^2***
- ***Supply current , increase***
- ***Size of the load C_L? increases***
- ***Smaller devices ? less power***

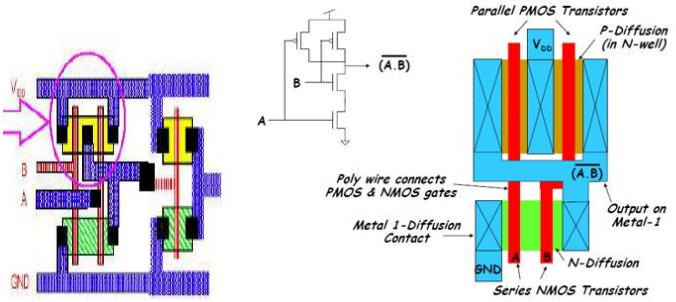
Question 2 (25)

1. *What type of logic function does these circuit do?* (5 points)

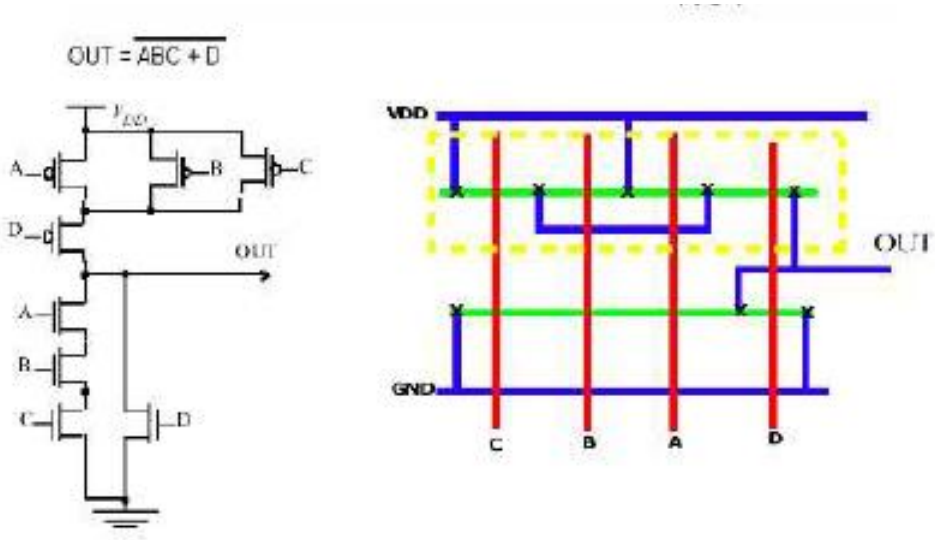


2. *Given the truth table below, (5 points)*

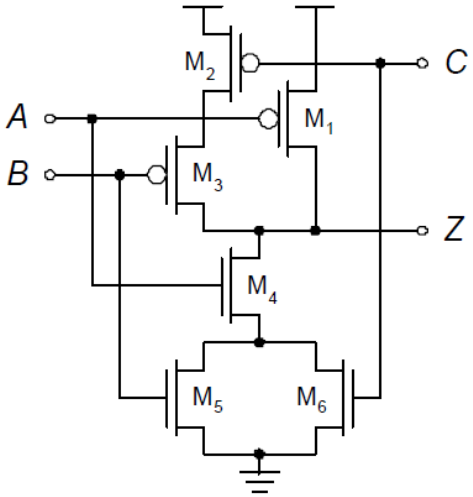
a. Draw stick digral/layout for 2-INPUT AND?



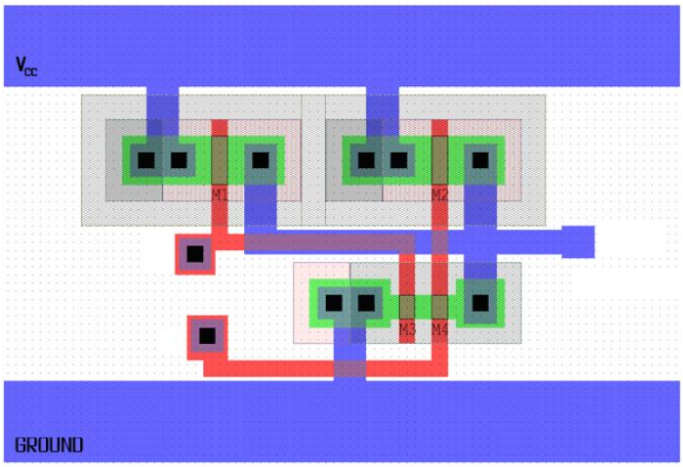
b. Draw stick diagram for Out= (ABC+D)' ***(5 points)***



c. Draw static implementation for F=(C+B).A (5 points)



1. Consider the following figure below, what type of logic gate is this? (5 points)



NAND2. The pull-up network has two PMOSFETs in parallel and the pull-down network has two NMOSFETs in series

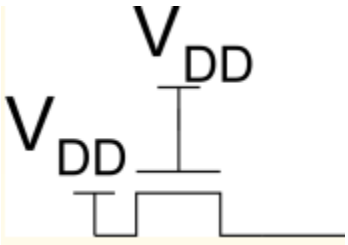
Question 4 (24)

1- What is the output voltage of each of these devices: **(15 points)**

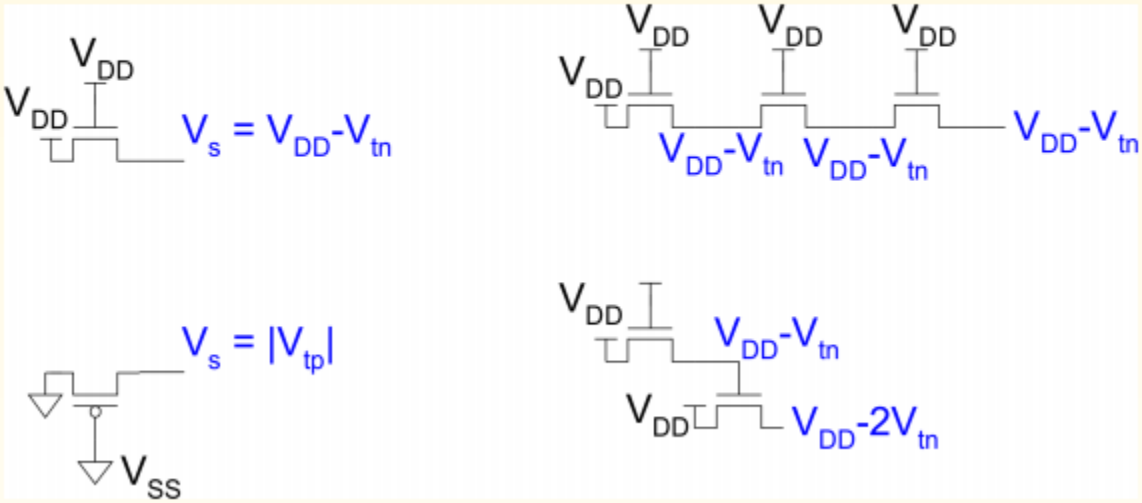
- If Vgd < Vt , channel pinches off near drain when Vds > Vdsat = Vgs – Vt

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{Cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} & \text{Linear} \\ \frac{\beta}{2}(V_{gs} - V_t)^2 & V_{ds} > V_{dsat} & \text{Saturation} \end{cases}$$

-
- Example, pass transistor passing VDD Vg = VDD If Vs > VDD − Vt, Vgs < Vt Hence, transistor would turn itself of

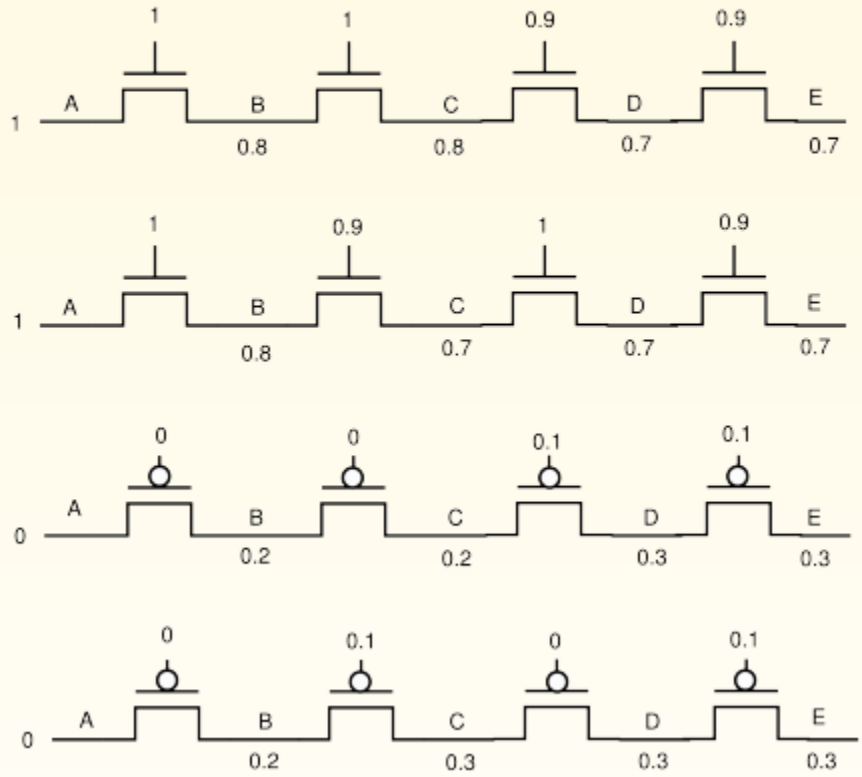


What would be the voltages on the different nodes?

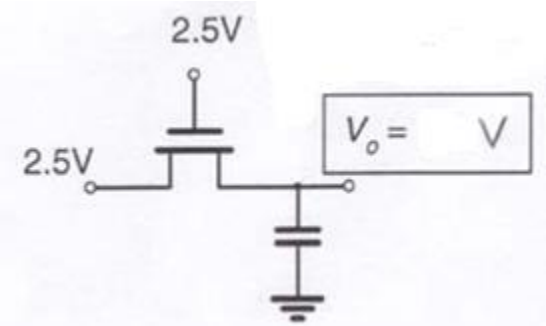


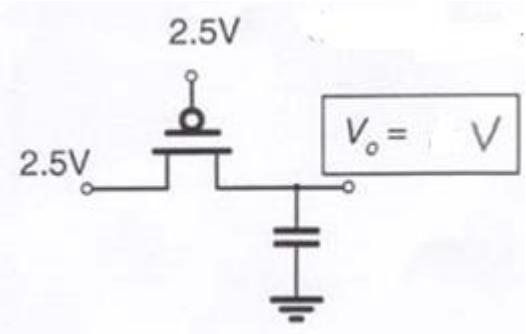
Assume: initial voltage of 0.5V on all the internal nodes

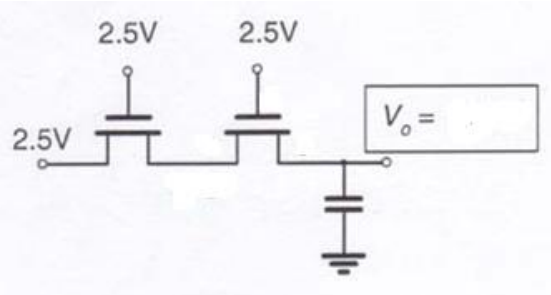
$V_{dd} = 1.0V$, $V_{t_n} = 0.2V$ and $|V_{t_p}| = 0.2V$

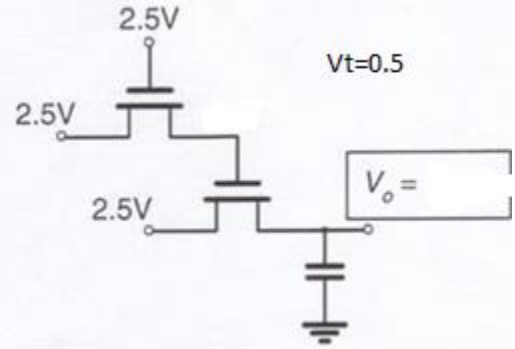


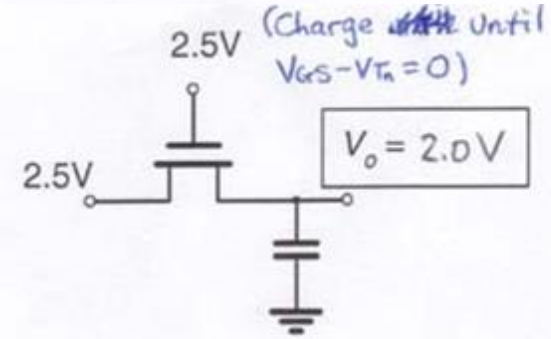
Extra thing just to understand … these we asked in previous exam

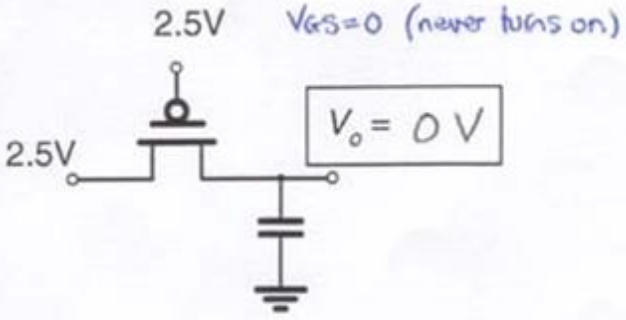


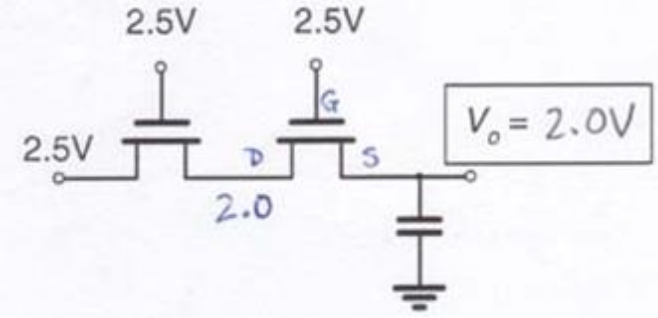


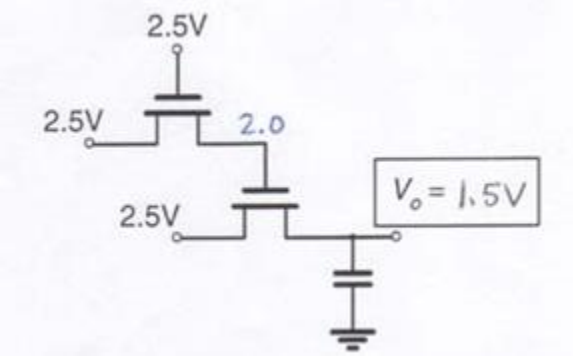






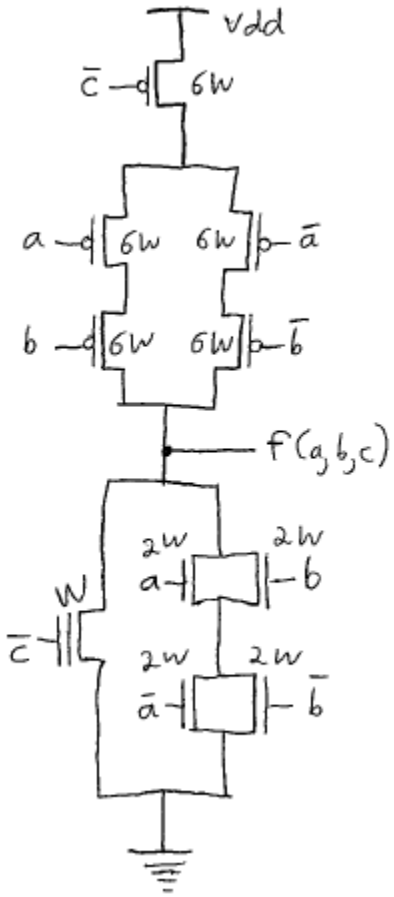






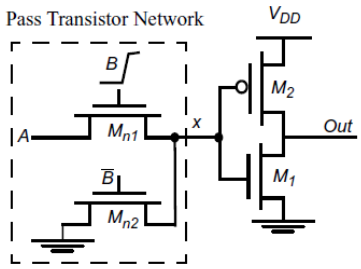
Question 4 (16)

A. a) Shown the circuit diagram for a static CMOS implementation what function it represent ? ***(4 points)***



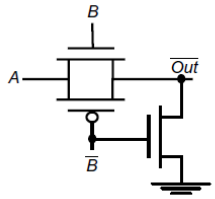
$$f(a,b,c) = (ab + \bar{a}\bar{b})c$$

B. What is the logic function performed by this circuit?**(3 points)**



The circuit is a NAND gate.

C. Implement the same circuit using transmission gates. (3 points) -AND GATE



D. In this problem, the circuits are implemented in 0.25um technology, and all the transistors have the minimum channel lengths.a. Consider the CMOS inverter from Fig. 2.a. If the NMOS transistor has channel width W_n and the PMOS transistor has channel width, W_p, label the voltage transfer characteristics from FIG. 2.b that correspond to following device sizes:(6 points)

A: $W_n = 5\mu m$, $W_p = 5\mu m$

B: $W_n = 1\mu m$, $W_p = 5\mu m$

C: $W_n = 5\mu m$, $W_p = 1\mu m$

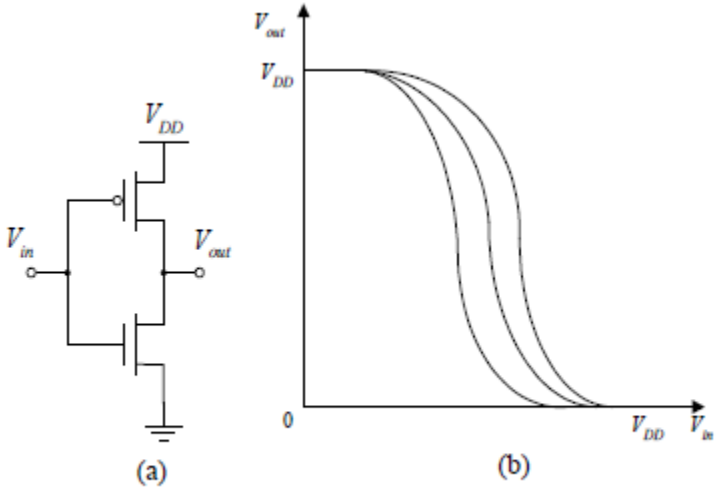
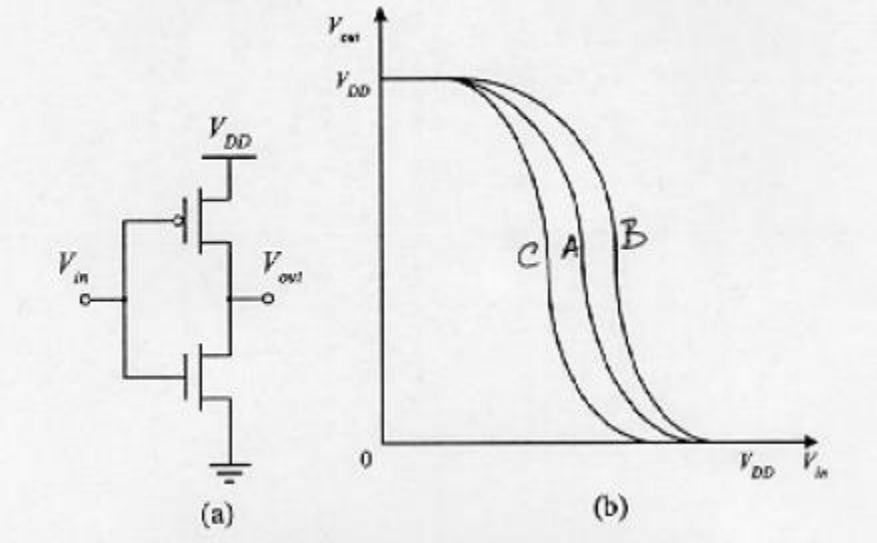


FIG. 2 CMOS inverter and Voltage Transfer Characteristics



NEED ALSO TO EXPLAIN RATION OF MOBILITY FOR N AND P

$$I_D = \frac{\mu_n \varepsilon_{ox}}{2T_{ox}} \frac{W}{L} (V_{GS} - V_{tn})^2 \qquad \text{(Saturated State)}$$

$$I_D = \frac{\mu_n \varepsilon_{ox}}{2T_{ox}} \frac{W}{L} \left[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2 \right] \qquad \text{(Non-Saturated State)}$$

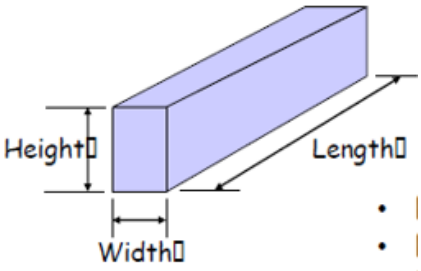
$$K = \frac{\mu \varepsilon_{ox}}{2T_{ox}} \qquad V_t = V_{to} \pm \gamma \left(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|} \right)$$

Q1: 25 points

1. What are the two types of CMOS transistor? Explain the Working Region of both devices , are they sized the same to have equal rise and fall time , if not why ? (6 points)
   - P channel and N channel semiconductor devices OR PMOS or NMOS, For CMOS technology
   - N works when we have positive voltage on the gate, N mos when we have zero voltage on the gate
   - No, N faster than P so p has bigger size
2. How does the Current flow in CMOS? From where to where? (2 points)
   - Nmos d→s
3. What are the basic design matrixes? (6 points)
   - Area/cost, Power, speed
4. What or how does the temperature affect CMOS devices? (2 points)
   - As temperature increased, the Speed will be go low as temp increased because Vt will increase
5. Explain What do we mean by process node? And how does that affect IC characteristics ? (3 points)
   - The technology node (also process node, process technology or simply node) refers to a specific semiconductor manufacturing process and its design rules.
   - Different nodes often imply different circuit generations and architectures. Generally, the smaller the technology node means the smaller the feature size, producing smaller transistors which are both faster and more power-efficient. Historically, the process node name refered to a number of different features of a transistor including the gate length as well as M1 half-pitch
6. What is drive strength? (2 points)

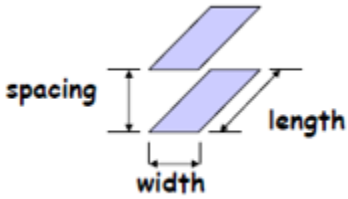
- Driver has raise/fall time proportional to the load

7. If you have wire as in the figure below, How do you calculate its resistance? What can I do toreduce the resistance by almost half ? (2 points)



- R= rL/A = r.Length /(width*length)
- Use different r, reduce length or increase width

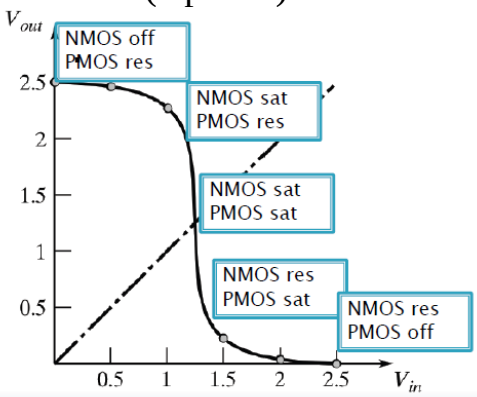
8. If we have 2 wires (plates as in figure below, how do you calculate the capacitance between them ? (2 points)



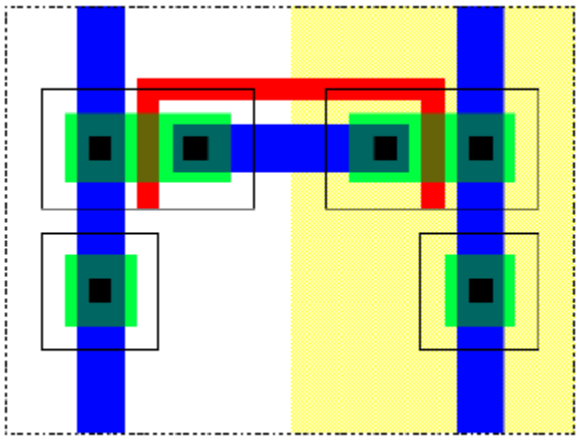
9. C=eps*A/d

Q2: 25 points

1. Draw a VTC curve for a CMOS invertor and SHOW regions of operation for each device (3 points)

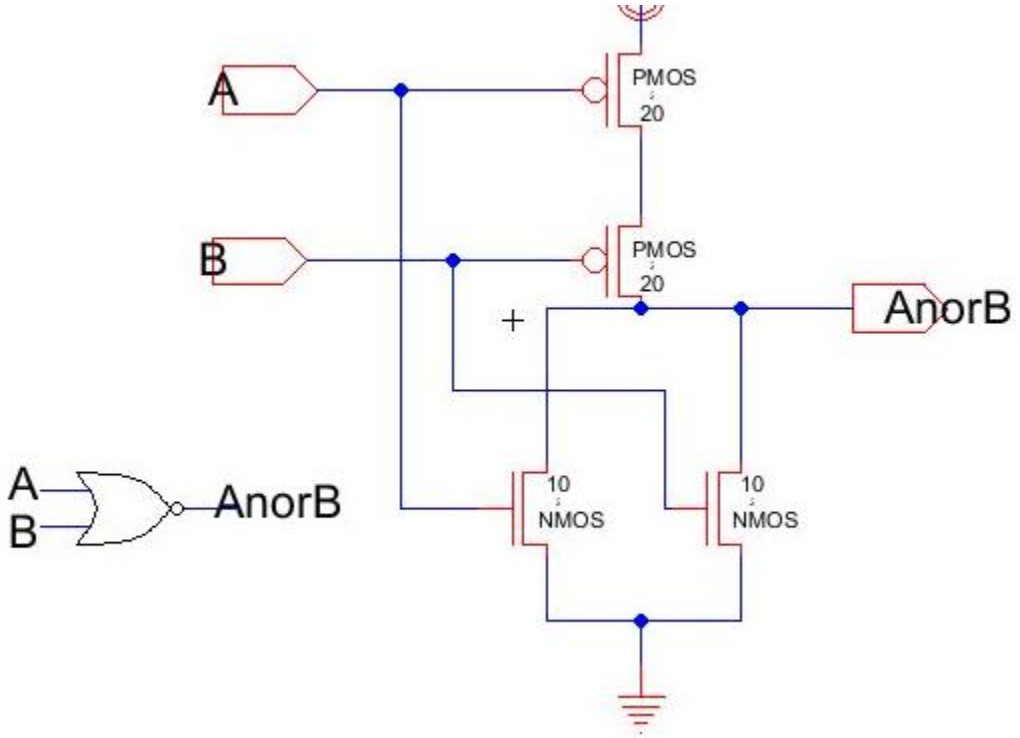


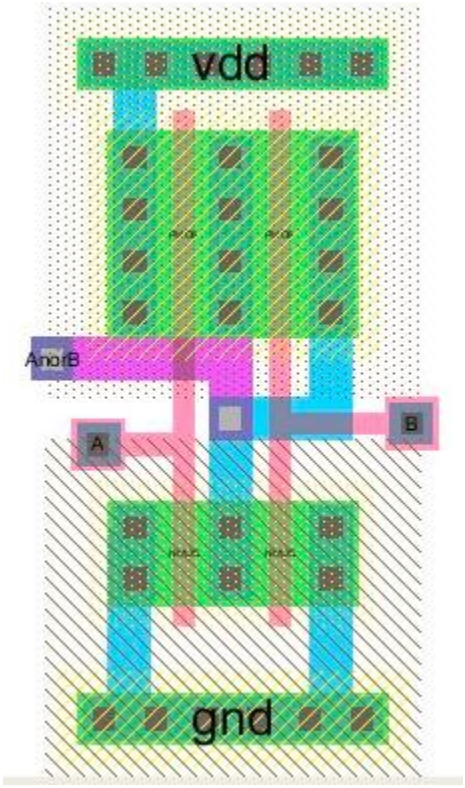
2. What will happen to the rise and fall slopes if we double both the NMOS and PMOS width? (2 points) lower
3. Draw A detail layout showing all materials and estimate dimension for inverter with p device size of 3u and n device of 1 u using 25nm process (5 points)



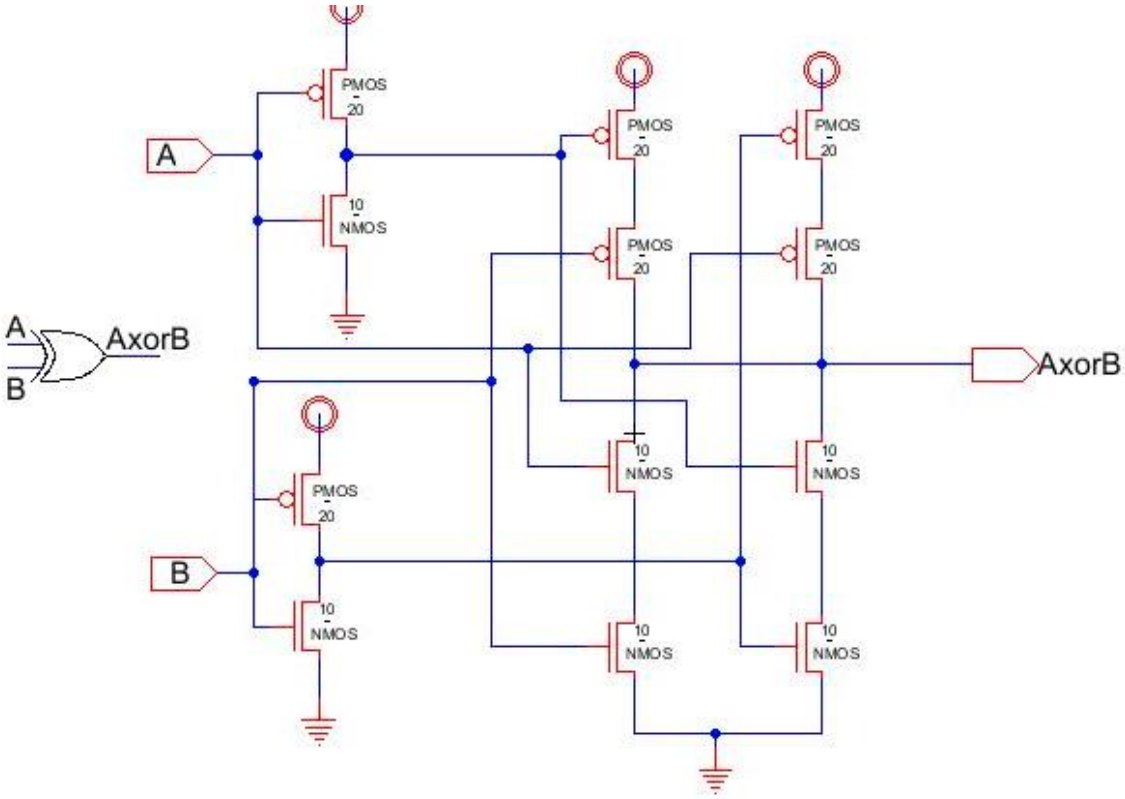
4. Why do VLSI chips have multiple metal layers? What are these used for? Why so many? (2 points)
   - Used for routing, the device become smaller, so we can have many devices so we can add more function in the same chip which required lot of routing, so we need more layers

5. Draw schematic and layout for a CMOS 2 input NOR gate which will have equal rise and fall time as an inverter which has N to P ration 2 using 90nm process and N device width for regular inverter is =10u? Note mark all layers used in layout (8 points).





1. Draw schematic for 2 input XOR gate (transistor level only, (no layout is required and size them correctly assuming ratio of n/p ratio of 2 ? (5 points)



Q3: 25 points

1. How do you measure wire delay ? SLOPES? (4 points)
   a. 50% OF THE SIGNAL , 20/80% for slopes
2. What is the impact of technology scaling on Resistance, Capacitance and RC (3 points)

SEE NOTES LOWER PROCESS WILL HAVE LESS CAP AND LESS R IN GENRAL, BUT WIDTH of wires can't be lower since it is small so it will have larger cap so it does not scal as devices width and length so wire rc will be dominant in low process

3. If you want to reduce the leakage, will you use the high threshold or the low threshold devices and why ? . (3 points)

4. Construct the CMOS logic circuit that implements= Y= a + (a' + b)' +cb' using the fewest possible transistors and size them to have equal rise and fall time with ration of n/p OF 2. You are allowed to use inverted inputs (e.g., a') rather than adding inverters to create these signals. (15 points)

solution

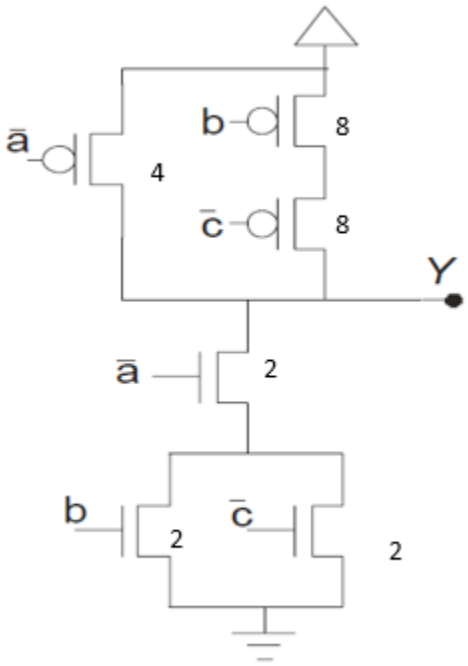
First let's simply the function to remove all inverted operations

$Y = a + (a\bar{b}) + c\bar{b}$

$Y = a + c\bar{b}$ (because A+AX = A)

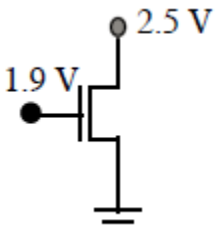
Thus

$Y_p = \bar{a} + \bar{c}b$, and $Y_n = \bar{a} \cdot \overline{c\bar{b}} = \bar{a} \cdot (\bar{c} + b)$, which looks correct because all AND/OR operations are complemented between Yp and Yn, and both have the same inputs. Substituting parallel connections for OR operations and series connections for ANDs, we get:

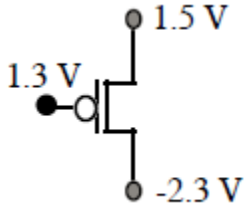


Q4: 25 points

1. Determine the bias state for the two circuit conditions if Vtn = 0.4 V. where Vtp = -0.4 V (10 points)

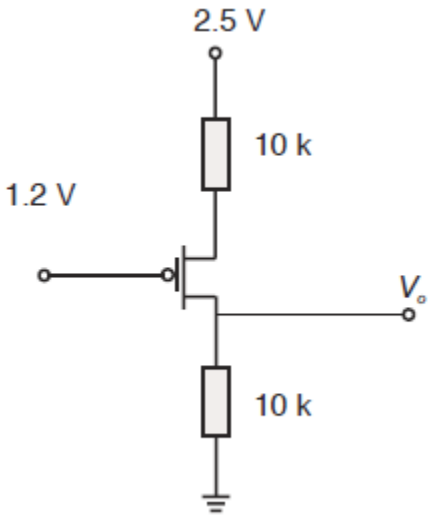


V_{GS} = 1.9 V, V_{DS} = 2.5 V, V_{tn} = 0.4 V, therefore V_{GS} = 1.9 V < 2.5 V + 0.4 V = 2.9 V. Eq. (3-7) is satisfied, and the transistor is in the saturated state described by



b) The gate voltage is not sufficiently more negative than either drain or source terminal to invert holes at the oxide interface, so that the transistor is in the offstate.

2. Calculate ID, VDS , and verify the assumed bias state of transistor M1 for Vtp = –0.4 V, Kp = 60 μA/V2, and W/L = 2. (15 points)



Assume a saturated bias state and

$$I_D = \frac{\mu\varepsilon_{ox}}{2T_{ox}}\frac{W}{L}(V_{GS} - V_{tp})^2$$

Since V_{GS} is not known, we must search for another expression to supplement this equation.

We can use the KVL statement

$$\begin{aligned} V_{GS} &= 1.2 - (V_{DD} - (I_D R_S)) \\ &= 1.2 - 2.5 + I_D R_S \\ &= -1.3 + (10\ \text{k}\Omega) I_D \end{aligned}$$

We substitute this into the saturated current expression to get

$$\begin{aligned} I_D &= 60\ \mu\text{A}(2)\left[-1.3 + (10\ \text{k}\Omega) I_D + 0.4\right]^2 \\ &= 120\ \mu\text{A}\left[-0.9 + (10\ \text{k}\Omega) I_D\right]^2 \end{aligned}$$

This quadratic equation in I_D gives solutions

$$I_D = 35.56\ \mu\text{A},\ 227.8\ \mu\text{A}$$

The valid solution is $I_D = 35.66\ \mu\text{A}$, since the other solution for I_D when multiplied by the sum of the two resistors gives a voltage greater than the power supply. V_{DS} is then

$$\begin{aligned} V_{DS} &= I_D(20\ \text{k}\Omega) - V_{DD} \\ &= (35.56\ \mu\text{A})\ (20\ \text{k}\Omega) - 2.5\ \text{V} \\ &= -1.789\ \text{V} \end{aligned}$$

and

$$\begin{aligned} V_S &= V_{DD} - I_D R_S = 2.5 - (35.56\mu A)\ (10k\Omega) \\ &= 2.144\ V \end{aligned}$$

Verify the bias state

$$V_{GS} = V_G - V_S = 1.2 - 2.144 = -0.944\ \text{V}$$

Transistor M1 is in saturation since

$$\begin{aligned} V_{GS} &> V_{DS} + V_{tp} \\ -0.944\,\text{V} &> -1.789\,\text{V} - 0.4\,\text{V} \end{aligned}$$