

BIRZEIT UNIVERSITY

Faculty of Engineering and Technology Electrical and Computer Engineering Department

Digital Systems "ENCS234" Introduction to Quartus II

Prepared by: "Ayham Hashesh"

> Objective

- Download Quartus II software tool.
- Create a simple task to take an idea how to use Quartus II software tool.

> Introduction

The Altera Quartus II software tool is an available environment for System on Programmable Chip design. This tutorial is not intended to be an exhaustive reference manual for the Quartus II software. Instead, it is a guide that explains how to install Quartus II software tool, build a project, compile a created project and then simulate it.

Table of Contents

1 How to Download Quartus	2
2 Task	
1 Project Creation	8
2 Compilation	11
3 Simulation	13
4 Symbols Creation	

1 How to Download Quartus II

Open the following link to Download Quartus II

➤ Link:

http://www.mediafire.com/file/eqd7xidoan3exqv/90_quartus_free.exe/file?fbclid=IwAR0Mmufw-YBRjv4I7uGM9I_6V_5WKokZ20z_ITPc9QJrNsL92IkrzMB-h8A

Follow up the following 16 Figures



Figure 1.1: After Opening the Link.

Figure 1.2: setup file, open it.



Figure 1.3: Fill yourname and company name as shown.

Quartus II 9.0 Web Edition Setup		\times
Select Program Folder Please select a program folder.		
	Setup will add program icons to the Program Folder listed below. You may type a new folder nar or select one from the existing folders list. Click Next to continue.	ne,
	Program Folder:	
	Altera	
	Existing Folders: Accessibility	~
	Accessories Administrative Tools	
	AnyDesk DOSBox-0.74-3	
	Maintenance Microsoft Office 2016 Tools	
	MySQL PSpice Student Start In	- 12
	System Tools	~
InstallShield	< Back Next > Cance	

Figure 1.4: Select Accessibility then click next.



Figure 1.5: Select custom then click next.

Quartus II 9.0 Web Edition Setup				\times
Select Features Select the features setup will install.				
SELECT ALL CHOICE	Select the features you want to ins	tall, and desele	ect the features you do not want to install.	
	 ✓ IP Library ✓ ACEX support ✓ APEX 20K/20KE /20KC suppo ✓ APEX II support ✓ Arria GX support ✓ Arria II GX support ✓ Arria II GX support ✓ Cyclone support 	384 MB 1 MB 33 MB 26 MB 80 MB 112 MB 12 MB 12 MB	s II software. This option is required to install a	
	Space Required on C: Space Available on C:	29. 1837:	27 MB 97 MB	
InstallShield	< <u>B</u> ack	<u>N</u> ext >	Cancel	

Figure 1.6: Select all choices.

Quartus II 9.0 Web Edition Setup		\times
Start Copying Files Review settings before copying	files.	
	Setup has enough information to start copying the program files. If you want to review or chan any settings, click Back. If you are satisfied with the settings, click Next to begin copying files. Current Settings: User Name and Company: AyhamHashesh; BZU Destination Directory	ge
	C:\MyDownloads\Quartus\quartus Design Directory: C:\MyDownloads\Quartus\qdesigns Program Folder: Accessibility	
	< >	× I
InstallShield	< Back Next > Canc	el]

Figure 1.7: Select next.



Figure 1.8: Wait it until it finished.

and the second se	Quartus II TalkBack	Х
# 1 in Performance & Productivity for CPLD, FPGA, and HardCopy* ASIC designs Question	Enable Advanced TALKBACK FEATURE NOTICE The TalkBack feature, included with the Licensed Program(s), enables ALTERA to receive limited information concerning your compilation of logic designs (but not the logic design files themselves) using the Licensed Program(s). One of the primary purposes of the TalkBack feature is to assist ALTERA in understanding how its customers use the Licensed Program(s) and ALTERA'S other products, so more effort can be	^
Q Design Software Version 9.0	placed on improving the reactires most important to users. To disable/enable the TalkBack feature, run qtb_install.exe located in your quartus/bin folder. INFORMATION COLLECTED ✓ Turn on the Quartus II software TalkBack feature	•
Adera.	OK Can	icel

Figure 1.9: To create a shortcut on the Desktop.

Figure 1.10: Select as shown.

Quartus II 9.0 Web Edition Setup

	InstallShield Wi	izard Complete			
	Setup has finished	installing Quartus	II 9.0 Web Editio	on on your computer.	
	View readme.tx	ત્ર			
InstallShield		< <u>B</u> ack	Finish		Cancel

Figure 1.11: Select Finish.





Figure 1.13: Select as shown.

Quartus	s II 9.0 Web Edition
	Thank you for installing the Quartus II Web Edition software - the #1 in performance and productivity. To upgrade to the full featured Subscription Edition please visit www.altera.com
Selec F C A	ct one of the following options Run the Quartus II software Add an IP license file (for users who have purchased IP)
L	OK Cancel

Figure 1.14: Select as shown.

STUDENTS-HUB.com

Start Designing	Start Learning
Designing with Quartus II software requires a project	The audio/video interactive tutorial teaches you the basic features of Quartus II software
Create a New Project (New Project Wizard)	Open Interactive Tutorial
Open Existing Project	

Figure 1.15: Select as shown.

Finally, you will have as shown in Figure 1.16

Quartus II File Edit View Project Assignments Processing Tools	Window Help	– o ×
ା ଜ ଜ ଜ ଜ ଜ ଜ ଜ ଜ ଜ ଜ ଜ ଜ ଜ ଜ ଜ ଜ ଜ ଜ ଜ		
Project Navigator	Tips & Tricks	
Complation Herarchy	Tips & Ticks Tips & Ticks Finable Version-Compating Finable Version-Compa	
Tasks × Row: Compilation ×		
Task G' Time (∧ ⊕ → Porple Design		View Quartus II Information
		Documentation
Type Message		
Message:	ical wanning N Error N subpressed N mag /	▼ Locate
For Help, press F1		Idle NUM

Figure 1.16

Now, we will take a simple task to take an idea about the software tool (Quartus II)

2 Task

By using the installed Quartus II software tool, make a design for Mux 2x1 the simulate it.

1 Project Creation

Select "File", then click on "New Project Wizard" as shown in Figure 1.1, then follow up the following figures (Figure 1.2 – Figure 1.12).



Figure 1.1

Figure 1.2

New Project Wizard: Directory, Name, Top-Level Entity [page 1 of 5] ×	New Project Wizard: Add Files [page 2 of 5]	×
What is the working directory for this project? STORE THE DROJECT C:\Users\AyhamHashesh\Desktop\Workspaces\Quartus\Mux_2x1	Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project. Note: you can always add design files to the project later.	•
What is the name of this project?	File name: Add	
mux2x1 PROJECT NAME	File name Type Library Design entry/sy HDL version Add A	All I
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.	Remo	ve
mux2x1	Propert	ies
/	Up	
See Executing Project Settings	Down	n
	Specify the path names of any non-default libraries.	
< Back Next > Finish Cancel	< Back Next > Finish Car	ncel

Figure 1.3



Device family				- Show in 'A'	vailable de	vice' list-	
Family: Cyclone II			-	Package:	Any		-
Devices: All			-	Pin count:	Any		-
Target device				Speed grad	de: Any		-
Auto device selecter	d bu the Fitte	r		Show :	advanced o	lavicas	
	1:1=1=	CHOK	CES GI	VES US	s THE	ible oplu	
 Specific device sele 	cied in Avair						
vailable devices:			NJALL	THE	UDE		
Name	L Core v	I F s	Liser 17	Memor	Embed	PU	_
FP2C20AF484A7	1.2V	18752	315	239616	52	4	_ `
EP2C20AF48418	1.2V	18752	315	239616	52	4	
EP2C20F256C6	1.2V	18752	152	239616	52	4	
EP2C20F256C7	1.2V	18752	152	239616	52	4	- 10
EP2C20F256C8	1.2V	18752	152	239616	52	4	
EP2C20F25618	1.2V	18752	152	239616	52	4	
EP2C20E484C6	1.2V	18752	315	239616	52	4	
EP2C20F484C7	1.2V	18752	315	239616	52	4	
<	1.97	10767	216		E.7		>
Companion device							
HardCopy:							\neg

Figure 1.5

Specify the other EDA tools $\mathchar`$ in addition to the Quartus II software $\mathchar`$ used with the project.		When you click Finish, the project will be created with the following settings:	
Design Entry/Synthesis Tool name: Format: Format: Run this tool automatically to synthesize the current design]	Project directory: C:/Users/AyhamHashesh/Desktop/Workspaces/Quartus/Mux_2x1/ Project name: mux2x1 Top-level design entity: mux2x1 Number of files added: 0 Number of suer libraries added: 0 Device assignments:	
Simulation Tool name: Kone> Format: Run gate-level simulation automatically after compilation]	Family name: Cyclone II Device: EP2C20F484C7 EDA tools: Cyclone State St	
Timing Analysis Tool name: <none> Format:</none>]	Simulation: < None> Timing analysis: < <none> Operating conditions: Core voltage: 1.2V Junction temperature range: 0-95 °C</none>	
Hun this tool automatically after compliation Sack Next > Finish Can	el	< Back Next > Finish C	ancel

Figure 1.6

Figure 1.7

After the previous steps you will have as shown in Figure 1.8. If you select files you will find it empty.

🥞 Q	🔇 Quartus II - C:/Users/AyhamHashesh/Desktop/Workspaces/Qua								
File	Edi	t	View	Project	Assignments	Processing	Tools		
D	È		Ø	🕹 X	₽ ₽ ∽	୍ଲ mux2x	:1		
Proje	ct Na	viga	ator —				* X		
Entit	y								
	Сус	lone	e II: EP	2C20F48			- 11		
	• •	mu	x2x1						
							- 11		
							- 11		
							- 11		
							11		
							- 11		
_ 	Hiera	rchy) 🖹 F	iles 🗗 De	sign Units				

Figure 1.8

Let us create our files.



Figure 1.9

Figure 1.10: Select Verilog HDL File

Write your code in the appeared empty blank as shown in Figure 1.11



Figure 1.11: Write your code here

Important Notes

- The blue words like (module, input, etcetera ...) are reserved words. Don't use these words as names for your variables.
- After write your code, press (Ctrl + S) to save it. You have to name the file as module name (in our case mux2x1), if you don't you code will not work.

🔇 Save As				×
Save in:	Mux_2x1	•	← 🗈 💣 📰▼	
Quick access	Name	^	Date modified 8/12/2019 1:11 PM	Type File fo
Desktop				
Libraries				
This PC				
Network				
	<			>
	File <u>n</u> ame:	mux2x1	•	<u>S</u> ave
	Save as type:	Verilog HDL File (*.v;*.vlg;*.verilog)	-	Cancel
		Add file to current project		

Figure 1.12: Name must be as module name

2 Compilation

Now, let us compile our project to check that there is no error. If you go back to Figure 1.8, you will find a change, your module has been created there. Right click on it then choose "Set as Top-Level Entity" as shown in Figure 2.1. then do as Figure 2.2

Important Notes

- Entity equivalent to module.
- This step to tell the Quartus which module to compile. Our project is simple but in complex projects many modules are exist. So, Quartus II can't decide by itself.

Files		1
	Open Remove File from Project	
	Set as Top-Level Entity	
	Create Symbol Files for Current File Create AHDL Include Files for Current File	
Historel	Properties	🕺 🖉 🥙 🎯 🕨 🕨 🧒 🏷 👦 🏷 😫 🕲 🔛
	Open in Main Window	Start Compilation 2x1.v
	 Enable Docking 	· · · · · · · · · · · · · · · · · · ·
ion. Joont	Close	

Figure 2.1: Select "Set as Top-Level Entity"

Figure 2.2: Select as shown to start compilation

After finsih you will have as shown in Figures (2.3 and 2.4). No need to worry about warnings)

If erroes are exist you will find them in the consule window.



Figure 2.3

Figure 2.4: Click Ok.

Now, Let us simulate our code to compare the results with studied one (Recall Table 1.1)

Selection	Input0	Input1	muxOutput
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Table 1.1: Mux 2x1 Truth Table

3 Simulation

Select "File" >> "New" >> "Vector Waveform File". (see Figure 3.1)



Figure 3.1

From the obtained empty blank, Right Click at the left side as shown in Figure 3.2

Waveform1.vv	/f									
	Maste	er Time Bar:	14.425 ns	 Image: Pointer: 	450 ps	Interval:	-13.98 ns	Start	E	nd:
► A ≫ € ■ # %		Name	Value at 14.43 ns	0 ps		10.0 ns	14.425 ns		20.0 ns	
			Cut	Ctril	X					
)注 火: 縦 XC) XE XE XE			Copy Paste	Ctrl+	·C >					
₽%(ĝ↓	<		Delete	C	el					>
			Zoom		>	Family Device Timing N	lodels		Cyclone II EP2C20F484C7 Final	
			Show All Hidde	en Nodes		Met timir	g requirements		Yes	

Figure 3.2

STUDENTS-HUB.com

Uploaded By: Malak Dar Obaid

Insert Node o	or Bus		×					
Name:	1		ОК					
Туре:	INPUT	-	Cancel					
Value type:	9-Level	-	Node Finder					
Radix:	ASCII	-						
Bus width:	1							
Start index:	0							
Display gray code count as binary count								

Select "insert" >> "insert node or bus ..." >> you will obtained as Figure 3.3





Figure 3.4: Follow the steps from 1 to 6

Insert Node o	r Bus		\times					
Name:	**Multiple Items**		OK					
Туре:	**Multiple Items**	-	Cancel					
Value type:	9-Level	-	Node Finder					
Radix:	ASCII	-						
Bus width:	1							
Start index:	0							
Display gray code count as bipary count								

Figure 3.5: Press Ok

STUDENTS-HUB.com

Uploaded By: Malak Dar Obaid

Waveform1.vw	f*			
	Master	Time Bar: 14.	425 ns 🔹	Pointer: 1.3 ns Interval: -13.13 ns Start: 0 ps End: 1.0 us
A ₩ €			Value at	0 ps 10.0 ns 20.0 ns
 ■		Name	14.43 ns	14.425 ns
	0	Selection	A 0	
	1∎	input0	A 0	
🗕 XW XL	⊡> 2	input1	A 0	
XE XE XE		muxOutput	AX	
X& X? XB				
88. €↓				
	<		>	< >>

As we can see from Figure 3.6, the output are don't cares at all the intervals.

Figure 3.6

Now we have to set the interval that we want to see the output at it.

Figure 3.7 must be done for all inputs. (Selection, input0 and input1)

I have used 5ns, 10ns and 15ns consecutively

mux2x1Wave.v	/wf								
	Master	Time Bar: 14.	425 ns	• •	Pointer:	200 ps	Interval:	-14.23 ns	Start:
┣ A ૠ ♥ ■ # ☆		Name	Value at 14.43 ns		Count Value	iming 3			×
$\sqrt{1}$ × 0 1	∎>0	Selection	A 0						
	<u>⊪1</u>	input0	A 0		Start time:	lo	ps	-	
	<u>∎>2</u>	input 1	A 0		End time:	1.0	us	•	
X번 XC \$\$\$ XC	@ 3	muxOutput	AX	IR					
X X? XB 🤰					- Transition	ns occur —			
82 41					C Relat	tive to clock	settings:		
<u>P</u> ;;; Z ♦	<		1		C P	ositive edge	9		
	,				O N	legative edg	je		
			S Summary og s & Synthesi	is	 At ab Count 	osolute times it every:	: 4	ns	<u> </u>
	6	🕂 🗃 🧰 Asseml	oler		Multir	blied bur 🔤	1		_
		≟ <i>(</i> ≣2 <mark>⊂а т</mark> ала:ла К	A		maid	billed by.	1		_
	Ľ		_						
<									
				-		- 5		OK _	Cancel

Figure 3.7: Must be done for all inputs.

mux2x1Wave.v	wf										- C ×
	Master	Time Bar: 14	.425 ns 📕	Pointer:	200 ps	Interval:	-14.23 ns	Start:	0 ps	End:	1.0 us
▶ A . € €		Name	Value at	0 ps		10.	0 ns	105	20	.0 ns	
🔲 🖊 😘		Name	14.43 ns				14	.425 ns			
$\sqrt{1}$ × 0 1		Selection	A 0				1			1	
	■>1	input0	A 0								
스 XY XL	₽ 2	input 1	A 0								
<u>∖</u> ₩ ½5 ₩2 \C	€	muxOutput	AX		********	*******	*********	×××××	*******	******	**********
X6 X7 XB											
58. 2↓											
1	<		>	<							>

After you finish you will have as shown in Figure 3.8. Output still Don't cares.

Figure 3.8

Before test our code press "Ctrl + S" to save it (you can choose any name). See Figure 3.9

😋 Save As				\times
Save in:	Mux_2x1	•	- 🗈 🖆 🎟 -	
Quick access Desktop Libraries This PC	Name	~ L_db	Date modified 8/12/2019 1:35 PM 8/12/2019 1:32 PM	Type File fc File fc
	<			>
	File name:	mux2x1Wave	▼ Si	ave
	Save as type:	Vector Waveform File (*.vwf)	✓ Ca	ncel
		Add file to current project		

Figure 3.9

Select as shown in Figure 3.10

 Quartus II - C:/Users/AyhamHashesh/Desktop/Workspaces/Quartus/Mux_2x1/mux2x1 - mux2x1

 File
 Edit
 View
 Project
 Assignments
 Processing
 Tools
 Window
 Help



Figure 3.10

Follow Figure 3.11

	Quartus II X
Simulation mode: Functional Generate Functional Simulation Netlist	
Simulation input: mux2x1Wave.vwf Add Multiple Files	Functional Simulation Netlist Generation was successful
Simulation period 2: NAME OF SAVED WAVE	
 Run simulation until all vector stimuli are used 	4
C End simulation at: 100 ns 💌	
Simulation options	
Automatically add pins to simulation output waveforms	
Check outputs Waverorm Comparison Settings	
Setup and hold time violation detection	> • •
Glitch detection: 1.0 Ins 💌	Cyclone II
Overwrite simulation input file with simulation results	EP2C20F484C7
Generate Signal Activity File:	dels Final
	requirements Yes
	elements 1 / 18,752 (<1%)
	mbinational functions $1/18,752(<1.6)$
0 % 00:00:00 6	View Quar Informat
🛃 Stop 😲 Open 🤐 Report	🔮 Document

Figure 3.11: follow the steps from 1 to 5.

After Pressing Report, the results will be shown as Figure 3.12

Simulation Waveforms													
Simulation mode: Functional													
Image: Master Time Bar: 14.425 ns Image: Master Time Bar: 17.43 ns Start En									http://www.com/ander/ande				
Α			Value	0 ps	10.	0 ns	20	.Qns	30.	0 ns			
€		Name	14.43 r			14.425	ins						
Ø,	P 0	Selection	AO			Ĩ							
Bb	⊡ •1	input0	A0										
-	₽ 2	input1	A 0										
99	 Ø3 	muxOutput	AU										
3				INPUTO	INPUT1	INPUTO	INPUT1	INPUTO	INPUT1	INPUTO	,		
80	<		>	< 0	0	0	0	1	0	0	>		

Figure 3.12

In the previous steps we can do the simulation for each component separately. But, in the real projects, there is more than one module. So, we will need something to make our design easier, this something called "Symbols"

4 Symbols Creations

Do as Figure 3.1. This symbol will be located in the memory to give us the ability to use it directly.



Figure 4.1" Create Symbol Files for Current File".

Figure 4.2

Select "File" >> "new" >> "Block Diagram/Schematic File" (see Figure 3.3)

New	×
	^
⊡- Design Files	
- AHDL File	
Block Diagram/Schematic File	
- EDIF File	
State Machine File	
SystemVerilog HDL File	
Tcl Script File	
Verilog HDL File	
WHDL File	
🚍 Memory Files	
Hexadecimal (Intel-Format) File	
Memory Initialization File	
😑 Verification/Debugging Files	
In-System Sources and Probes File	
- Logic Analyzer Interface File	
SignalTap II Logic Analyzer File	
Vector Waveform File	
🖻 Other Files	
AHDL Include File	
Block Symbol File	
Chain Description File	
Synopsys Design Constraints File	
Text File	~
OK	Cancel

Figure 4.3: Select as shown.



An empty blank (1) will be shown, double click on it well show blank (2). See Figure 3.4



✓ Note that: We will add the created blocks from "Blank 2" to "Blank 1".

From Figure 4.4

Number 3 (Project folder at the left side of blank 2)

contains our symbols (mux2x1 in our case).

Number 4 (the second folder) contains built-in modules like and gates, or gates, inputs and outputs ports and several useful components.

Number 5 used to search for components

Important Notes:

- Don't miss use buses, and be careful when you connect them as they connected as you need and no node consist from the collision between them.
- Number 6: Orthogonal node tool: One Bus (we will use for individual inputs)
- Number 7: Orthogonal Bus tool: multiple Buses (used when declare arrays in module, you have to name each bus!)

Now try to build the Figure 3.5. you can Compile and Simulate it as shown previously.

✓ Note that: you can change the name of components by double clicking on it

	mux2x1	
pin_name NPUT pin_name1 NPUT pin_name2 NPUT	input0 muxOutput - input1 Selection	SUTPUT pin_name3
	inst	

Figure 4.5: System Design