ENEE2360 Analog Electronics

T9:
Field Effect Transistor- FET

Instructor : Nasser Ismail

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FET Vs conventional Transistors (BJT)

Advantages

1- High input impedance ; ~100 M !

2- Fewer steps in manufacturing process.

3- More devices can be packaged into smaller area for integrated circuit **IC**

Disadvantages

1- Low values of voltage gain.

2- Poor high frequency performance.

3- Sensitivity to Electro-static Discharge (ESD) and special handling is required.

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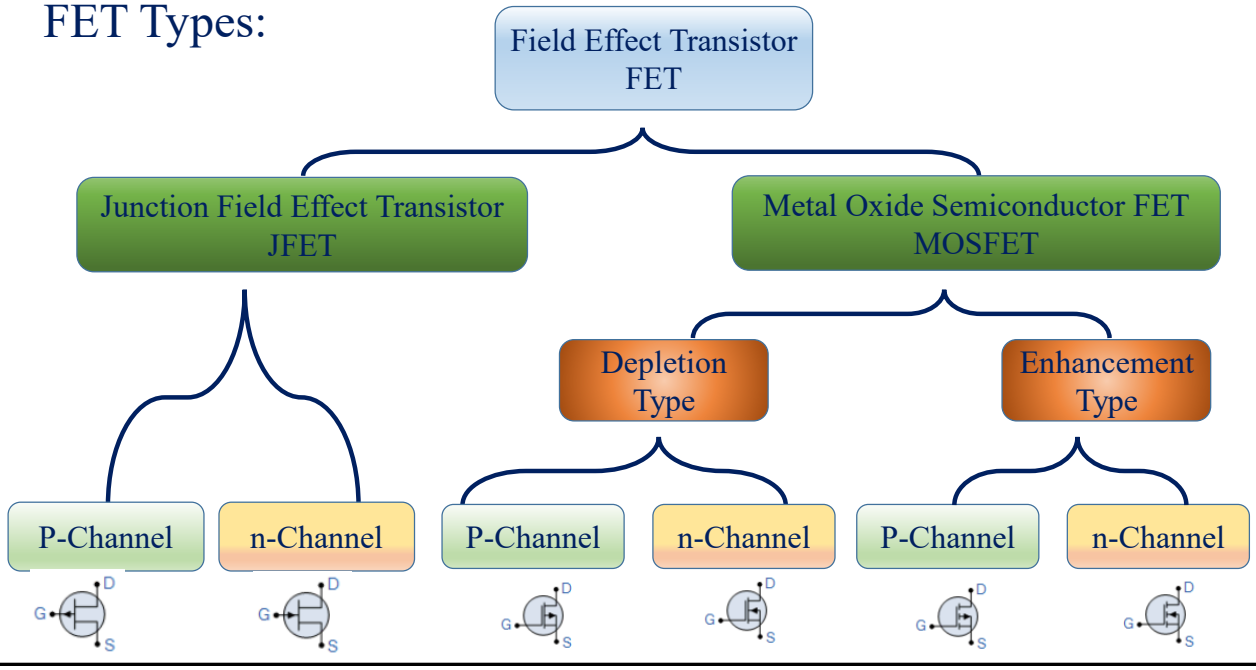
FET Types:

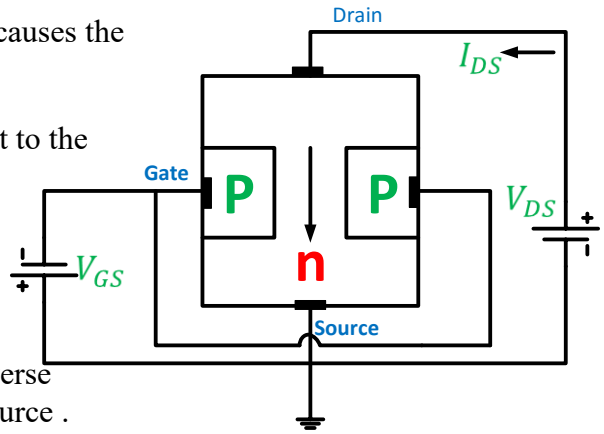


Junction Field Effect Transistor JFET

JFET construction:

- ✓ Reverse biasing the gate to source junctions causes the formation of the depletion region
- ✓ The drain has the proper polarity with respect to the source to establish the drain current I_{DS}
- ✓ The value of I_{DS} depends on the width of the channel.
- ✓ The width of the channel is controlled by reverse biasing the pn-junctions between gate and source .
- ✓ If the channel width increases I_{DS} increases .

n-channel JFET



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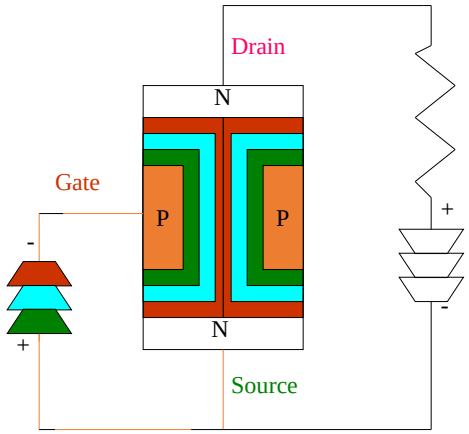
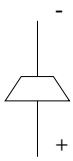
Operation of a JFET

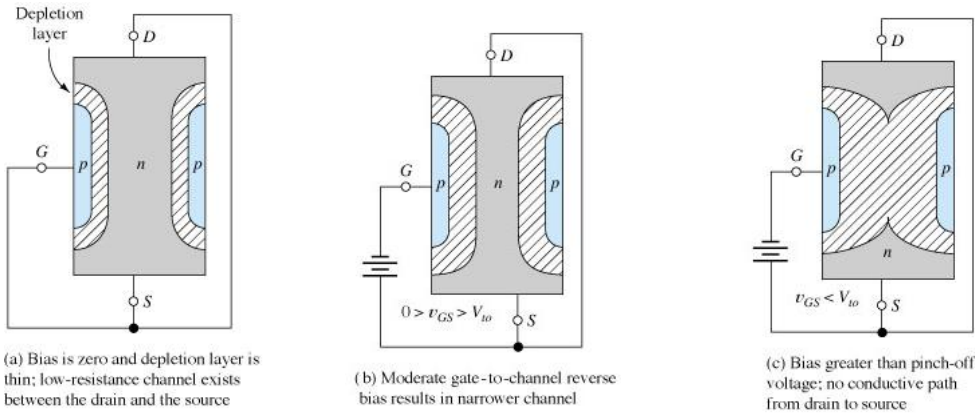




DC Voltage Source

http://www.learnabout-electronics.org/fet_03.php

N-Channel JFET Operation



The nonconductive depletion region becomes thicker with increased reverse bias. (*Note:* The two gate regions of each FET are connected to each other.)

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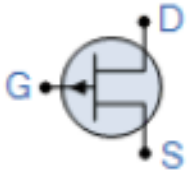
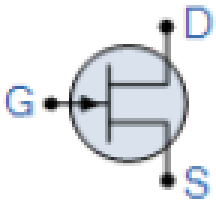
JFET Circuit Symbol:

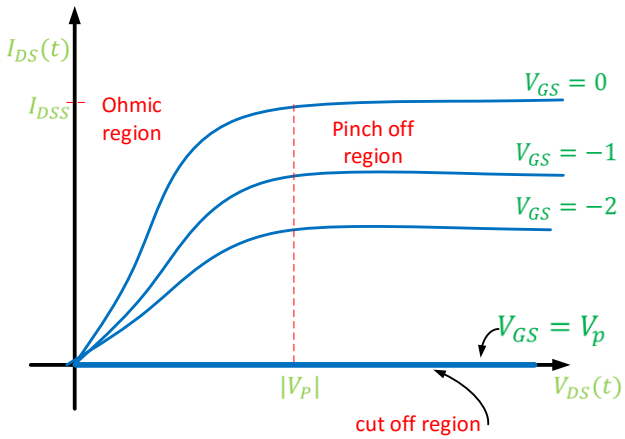
P-Channel

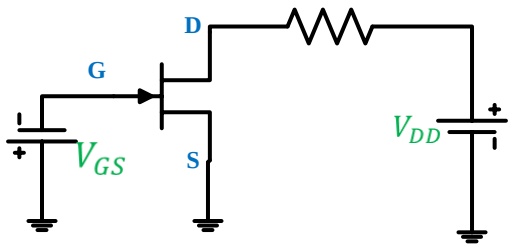


n-Channel



JFET output characteristic:





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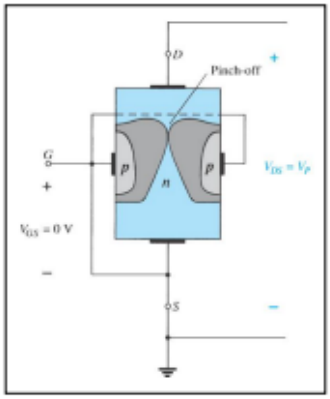
JFET Characteristics: Pinch Off

- If V_{GS} = 0 V and V_{DS} continually increases to a more positive voltage, a point is reached where the depletion region gets so large that it pinches off the channel.
  - This suggests that the current in channel (I_D) drops to 0 A, but it does not: As V_{DS} increases, so does I_D. However, once pinch off occurs, further increases in V_{DS} do not cause I_D to increase.

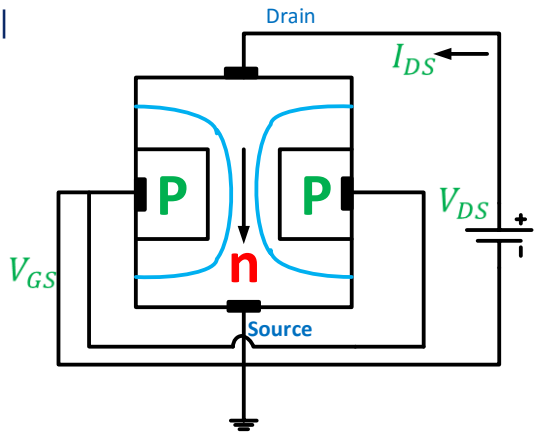


Pinch of voltage V_P:

For $V_{GS} = 0$,the value of V_{DS} at which I_{DS} becomes essentially constant
Is the absolute of the pinch of voltage $V_{DS} = |V_P|$

Some literature refer to Vp as $V_{GS(off)}$

$$V_P = \begin{cases} negative\ value\ for\ n\_channel \\ positive\ value\ for\ p\_channel \end{cases}$$



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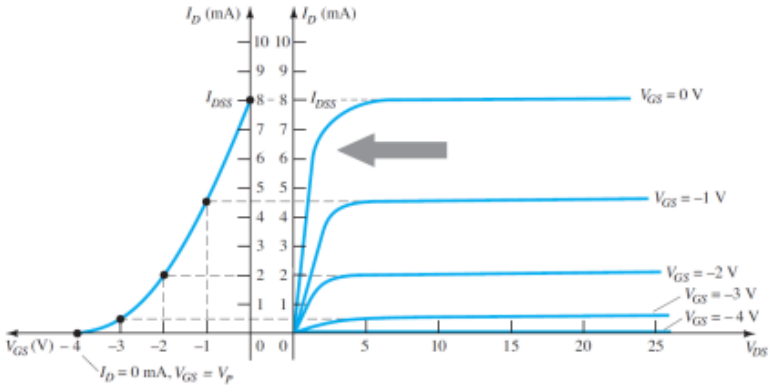
JFET Transfer characteristic curve:

$$I_{DS}(t) = I_{DSS}\left(1 - \frac{V_{GS}(t)}{V_P}\right)^2$$

In pinch off region:

$$V_P < V_{GS} \leq 0$$

$$|V_{DS}| > |V_P| - |V_{GS}|$$



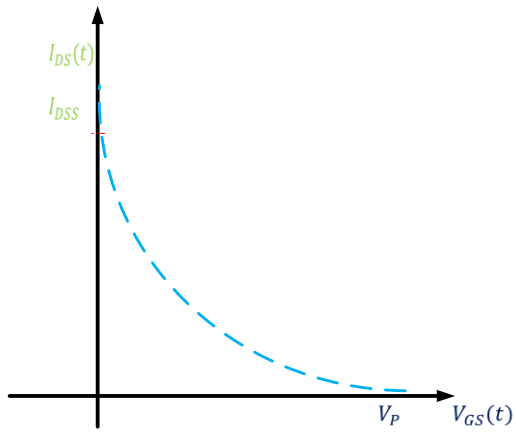
P-channel JFET

$$I_{DS}(t) = I_{DSS}\left(1 - \frac{V_{GS}(t)}{V_P}\right)^2$$

In pinch off region:

$$|V_{DS}| > |V_P| - |V_{GS}|$$

$$V_P > V_{GS} \geq 0$$



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Summary

Pinch off voltage:

- ✓ **The voltage that cusses the depletion region to touch and close the channel is called pinch off voltage**
- ✓ **For the n-channel JFET to be in the pinch off region:**

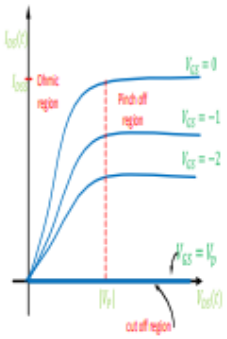
$$V_P < V_{GS} \leq 0$$

$$|V_{DS}| > |V_P| - |V_{GS}|$$

- ✓ **For the p-channel JFET to be in the pinch off region:**

$$|V_{DS}| > |V_P| - |V_{GS}|$$

$$V_P > V_{GS} \geq 0$$



Common JFET Biasing Circuits

- ➢ Fixed-Bias
- ➢ Self-Bias
- ➢ Voltage-Divider Bias

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Basic Current Relationships

For all FETs:

$I_G \cong 0$ A

$I_D = I_S = I_{DS}$

For JFETS

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

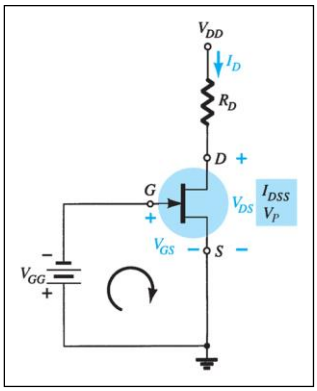
Fixed-Bias Configuration

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0\,\text{V}$$

$$\therefore V_D = V_{DS}$$

$$\therefore V_{GS} = -V_{GG}$$



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Example

$V_{GS} = V_G - V_S = -1.5 - 0 = -1.5\ \text{V}$

Assuming JFET is in pinch off region

1) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$= 10\ \text{mA}\left(1 - \frac{-1.5}{-4}\right)^2$

$= 3.9\ \text{mA}$

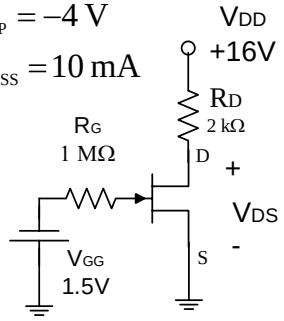
2) $V_{DS} = V_{DD} - I_D R_D$

$= 16 - ((2\text{k})(3.9\ \text{mA}))$

$= 8.2\ \text{V}$

$V_P = -4\ \text{V}$

$I_{DSS} = 10\ \text{mA}$



3)check for $|V_{DS}| > |V_P| - |V_{GS}|$?

$|8.2| > |-4| - |-1.5|$

assumption is true

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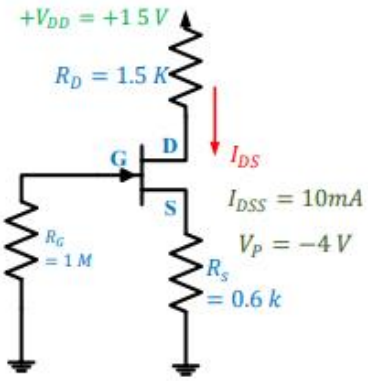
2) Self – bias circuit

- **Assume that the JFET is in the pinch off region**

$I_{DS} = I_{DSS}\ (1 - \frac{V_{GS}}{V_P})^2$

$V_{GS} = V_G - V_S$

$V_{GS} = -(0.6\text{K})\ I_{DS}$



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Sub 2 into 1

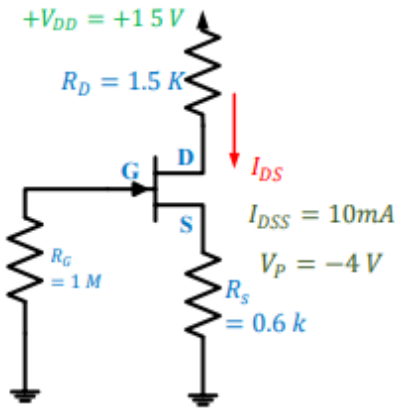
$$\therefore I_{DS} = 10 \times 10^{-3}\left(1 - \frac{-0.6K I_{DS}}{-4}\right)^2$$

I_{DS} = 14.77 mA , 3mA

Since $I_{DS} = 14.77\text{mA} > I_{DSS}$

$\therefore$ I_{DS} = 3mA

V_{GS} = -1.8 V



$V_{DD} = R_D I_{DS} + V_{DS} + R_S I_{DS}$

V_{DS} = 8.7 V

For the JFET to be in the pinch off

- $|V_{DS}| > |V_P| - |V_{GS}|$
  $> |-4| - |-1.8|$
  $|V_{DS}| > 2.2$ V

- Since $|V_{DS}| > 2.2$ V , the JFET is in the pinch off region and our assumption is ok and

- I_{DS} = 3.0 mA
  V_{DS} = 8.7 V
  V_{GS} = -1.8 V

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3) Voltage Divider bias circuit

$I_{DS} = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$ 1

$V_{GS} = V_G - V_S$

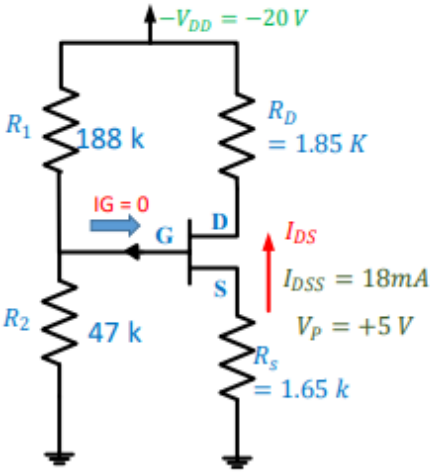
$V_G = \frac{47K}{47K+188K}(-20) = -4\ V$

$V_S = -R_S I_{DS} = -(1.65K)\ I_{DS}$

KVL:

$V_{GS} = -4 + (1.56K)\ I_{DS}$.....2

sub 2 into 1 , we obtain



$I_{DS} = \begin{cases} 4.02mA & \surd \\ 7.4\ mA & X \end{cases}$

$V_{DS} = -5.93\ V$

Example

V_S must be more positive than V_G

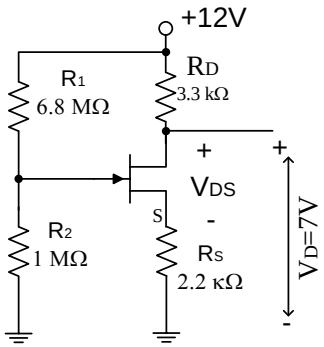
to keep the gate – source junction reverse biased

$V_S = I_D R_S$

$V_{GS} = \frac{R_2 V_{DD}}{R_1 + R_2}$

$V_{GS} = V_G - I_D R_S$

$V_{GS} = \frac{R_2 V_{DD}}{R_1 + R_2} - I_D R_S$



$V_D = V_{DD} - I_D R_D = 7\ \text{V}$

$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12-7}{3300} = 1.52\ \text{mA}$

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Example

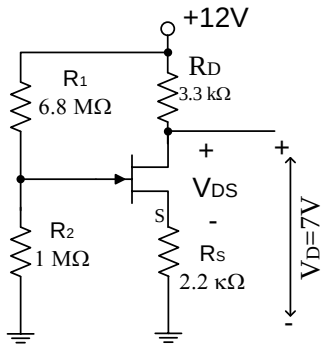
$$V_S = I_D R_S = (1.52\text{mA})\,(2.2\text{k}\Omega) = 3.34\text{ V}$$

$$V_G = \frac{1\text{ M}}{1\text{ M} + 6\text{ M}} 15 = 1.54\text{ V}$$

$$V_{GS} = 1.54 - 3.34 = -1.8\text{ V} < 0 \quad \Leftarrow \text{OK}$$

also

$$I_D = \frac{V_S}{R_S} = \frac{3.34}{2200} = 1.52\text{ mA}$$



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Metal Oxide Semiconductor Field Effect Transistor MOSFET

- 1) Depletion type MOSFET: DMOSFET
- 2) Enhancement type MOSFET: EMOSFET
- The MOSFET differs from the JFET in that it has no pn junction structure; instead, the gate of the MOSFET in insulated from the channel by a silicon dioxide (S_iO_2) large.
- Due to this the input resistance of MOSFET is greater than JFET.

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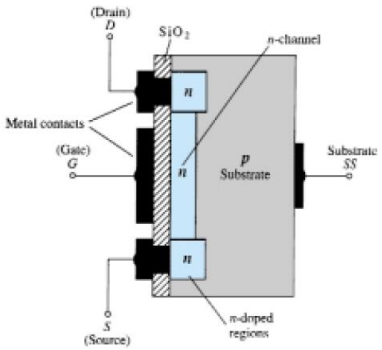
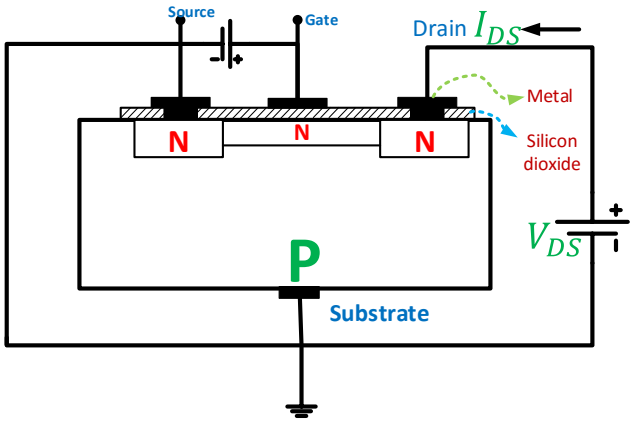
Depletion type MOSFET:

- Construction of n-channel DMOSFET:





Operation , characteristic and parameters of DMOSFET

♦ **n-channel DMOSFET**

- On the application of V_{DS} and keeping V_{GS}=0 electrons from the n-channel are attracted towards positive potential of the drain terminal .

- This establishes current through the channel to be denoted as I_{DSS} at V_{GS}=0 .

- If we apply negative gate voltage ($V_{GS}< 0$) the negative charge on the gate repel electrons from the channel . The number of repelled electrons depends on the magnitude of the negative voltage V_{GS}.

- The greater the negative voltage applied at the gate , the level of drain current will be reduced until it reaches zero ; $V_{GS}= V_P$.

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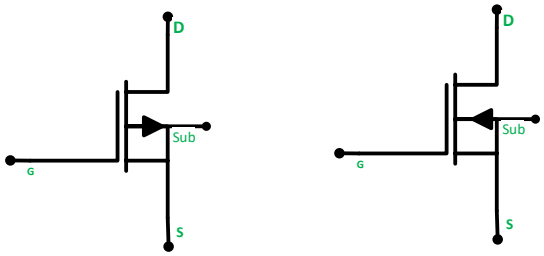
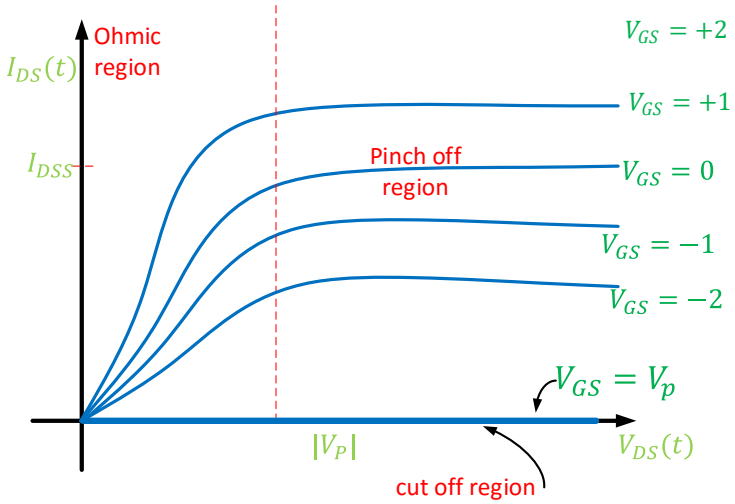
- For positive value of V_{GS}, the positive gate will draw additional electrons from the p-type substrate and the drain current increases .



P-channel DMOSFET

n-channel DMOSFET

Drain characteristics for an n-channel DMOSFET



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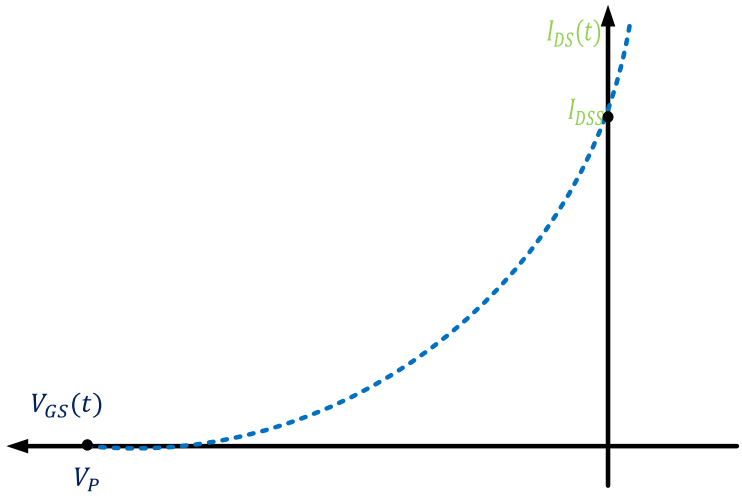
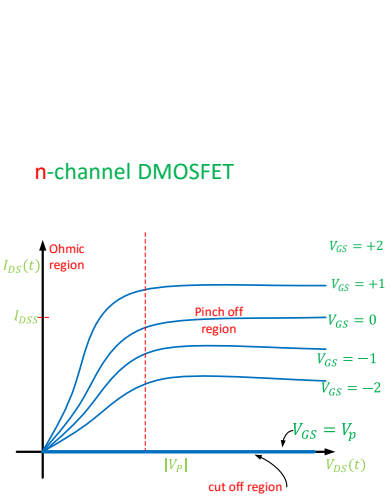
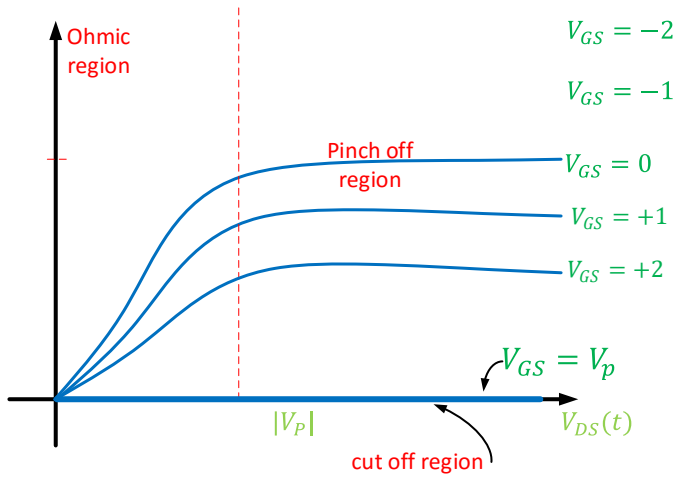
Transfer characteristics for an n-channel DMOSFET



Drain characteristics for an p-channel DMOSFET





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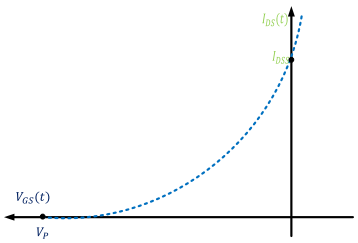
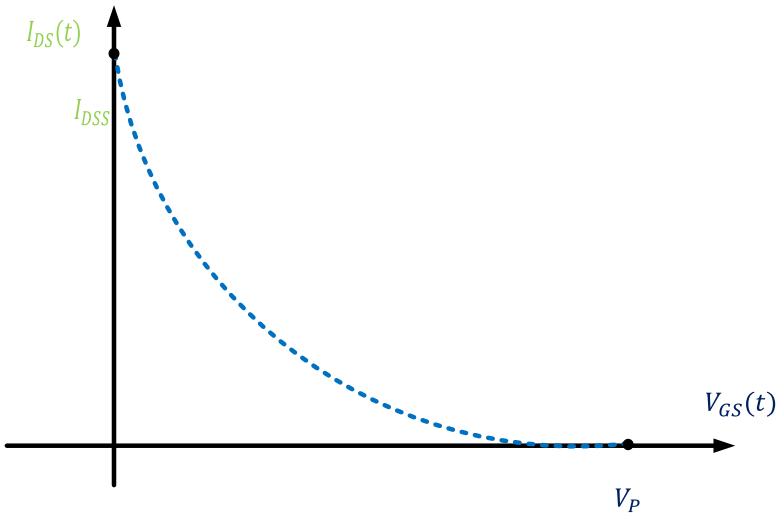
Transfer characteristics for an p-channel DMOSFET

n-channel DMOSFET





In the pinch off region

$$i_{DS}(t) = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

♦ For the n- channel

$V_{GS} > V_P$ (negative)
$V_{DS} > V_{GS} - V_P$

♦ For the p- channel

$V_{GS} < V_P$ (positive)
$V_{DS} < V_{GS} - V_P$

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Example

Suppose that the DMOSFET is in the pinch off region

$I_{DS} = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$ 1

$V_{GS} = V_G - V_S = V_G$

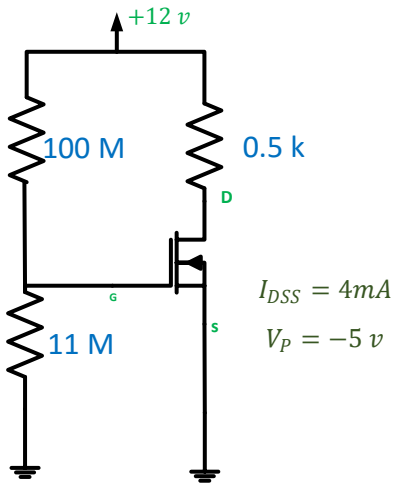
$V_G = \frac{11M}{11M+100M}(12) = 1.19$ v 2

sub 2 into 1 , we obtain

$I_{DS} = 6.13$mA $> I_{DSS}$!! THIS IS POSSIBLE AND DMOSFET WILL OPERATE IN ENHANCEMENT MODE

$V_{DS} = V_{DD} - 0.5K\ I_{DS} = 8.93$ v

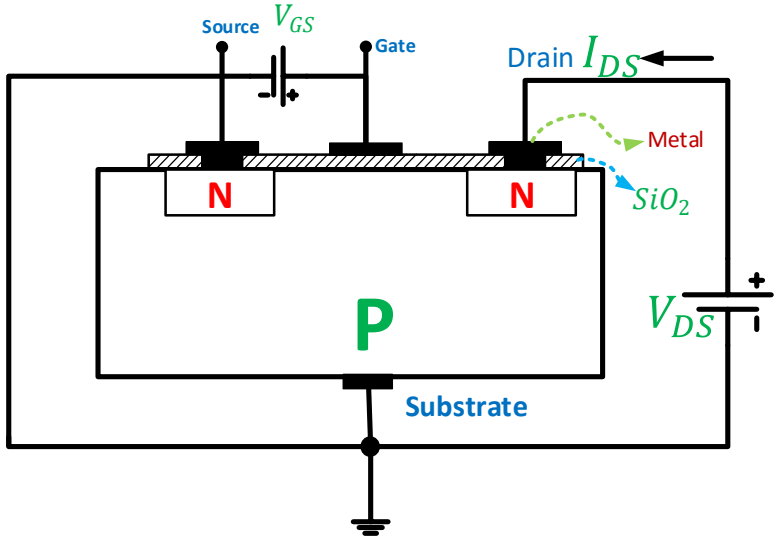
$V_{DS} >^{?} V_{GS} - V_P = 6.19$ v



$I_{DSS} = 4$mA $V_P = -5$ v

Enhancement Type MOSFET

- Construction of n-channel EMOSFET:



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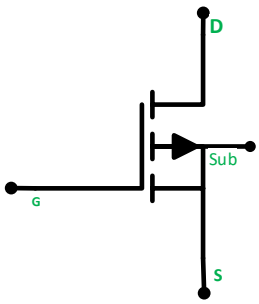
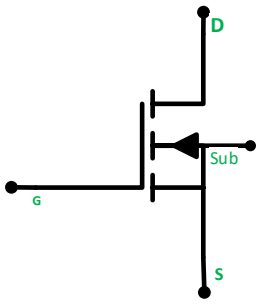
Operation , characteristic and parameters of EMOSFET

- On the application of $V_{DS}$and keeping V_{GS}=0 practically zero current flows .
- If we increase V_{GS} in the positive direction the concentration of electrons near the SiO_2 surface increases ,
- At particular value of V_{GS} there is a measurable current flow between drain and source ; I_{DS} .
- This value of V_{GS} is called threshold voltage denoted by V_T or $V_{GS(TH)}$
- A positive V_{GS} above V_T induce a channel and hence the drain current (I_{DS}) by creating a thin layer of negative charges (electrons) in the substrait adjacent to the SiO_2 large .

The conductivity of the channel is enhanced by increasing V_{GS} and thus pulling more electrons into the channel .



P-channel
EMOSFET



n-channel
EMOSFET

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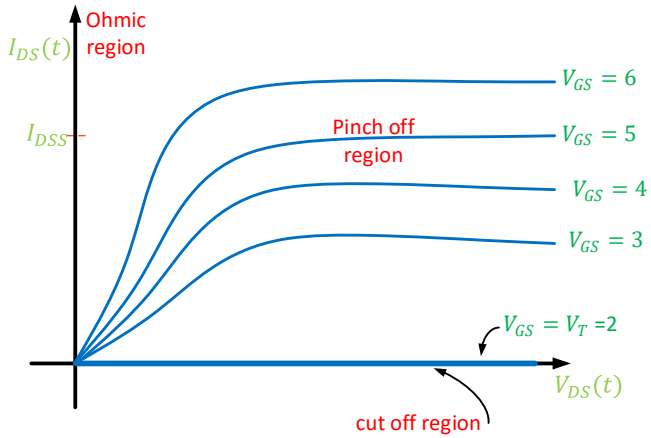
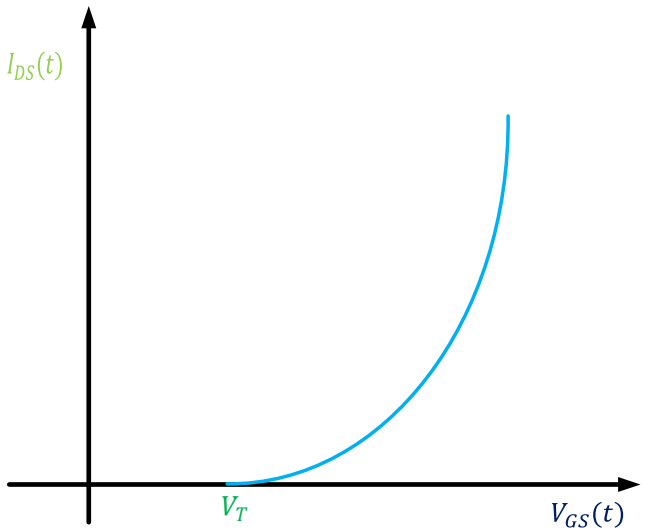
Drain characteristics for an n-channel EMOSFET



Transfer characteristics for an n-channel EMOSFET



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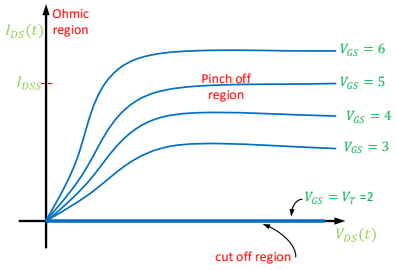
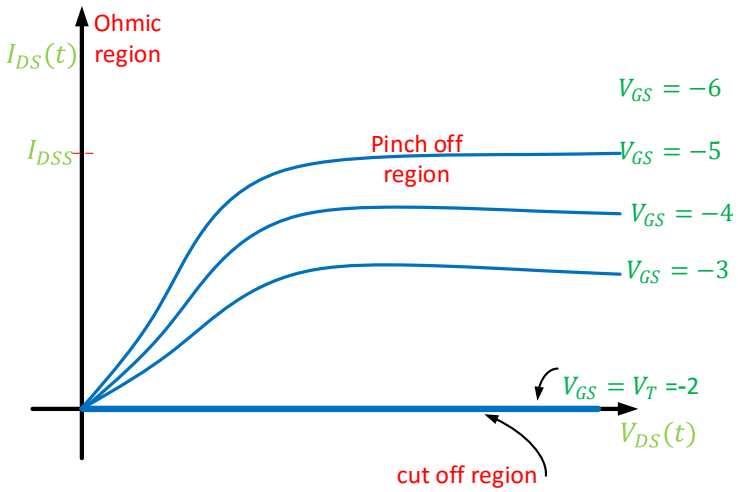
Drain characteristics for an p-channel EMOSFET

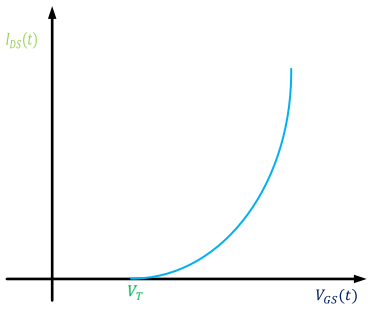
n-channel



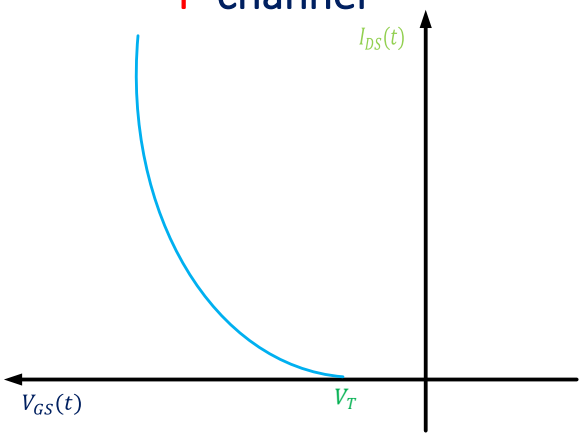


Transfer characteristics for an p-channel EMOSFET

n-channel



P-channel



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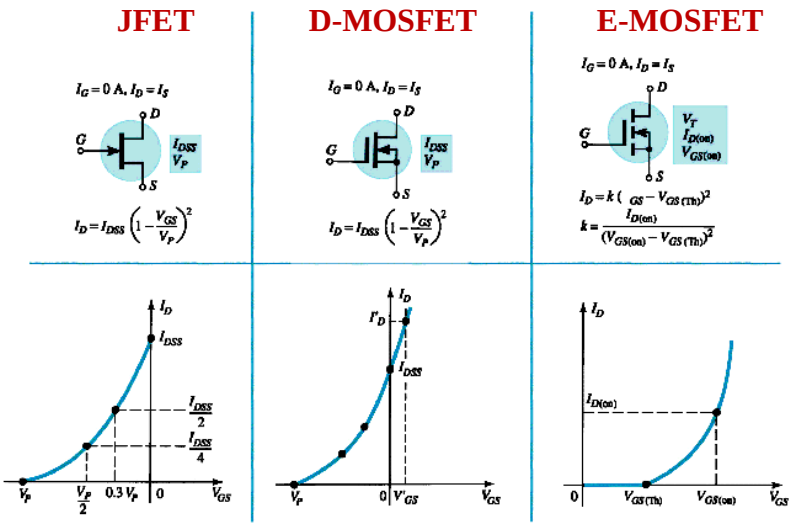
Summary Table



In the pinch off region- EMOSFET

$$i_{DS}(t) = K_n(V_{GS}(t) - V_T)^2$$

$$K_n = \frac{1}{2}K`_n\frac{W}{L}$$ Just for Information

$$K`_n = \mu_n C_{ox}$$ Just for Information

$$|V_{DS}| > |V_{GS} - V_T|$$

$V_{GS} > V_T$; n- channel
$V_{GS} < V_T$; p- channel

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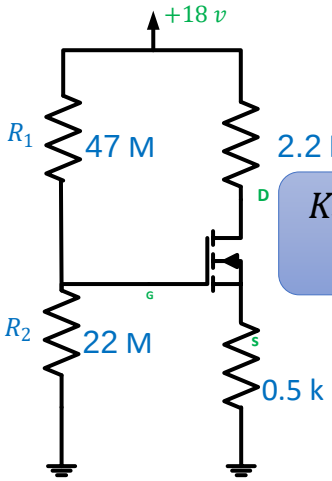
Example

$I_{DS}= K_n(V_{GS} - V_T)^2$ 1

$V_{GS}= V_G - V_S$

$V_G = \frac{22M}{22M+47M}(18) = 5.74v$



$K_n=0.25X10^{-3}A/V^2$
V_T = 2 v

$V_S= (0.5K)\ I_{DS}$

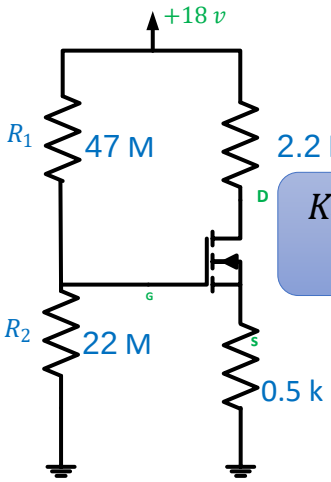
V_{GS} = 5.74 - (0.5K) I_{DS}.....2

solving for $\boldsymbol{V_{GS}}$:

V_{GS}= 4.78v √
= -8.78v X

I_{DS}=1.92m A

V_{DS}= 12.82> | $V_{GS} - V_T$|



$K_n=0.25X10^{-3}A/V^2$
V_T = 2 v

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Complementary MOS (cmos) inverter

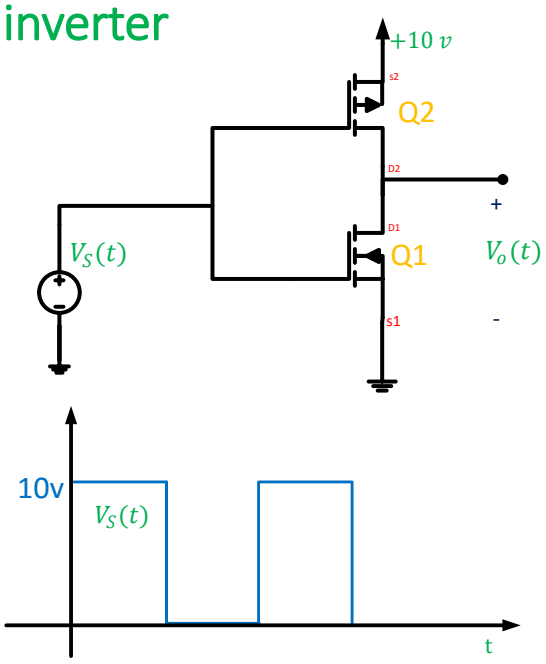
$V_{GS1} = V_{G1} - V_{S1} = 10\text{-}0 = 10\text{ v} > V_{T1}$

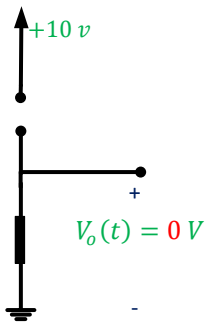
1) Let V_S(t) = 10 v

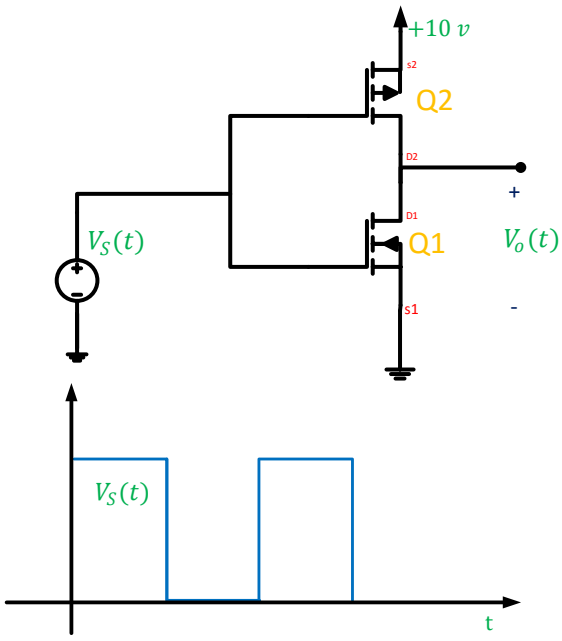
$V_{GS2} = V_{G2} - V_{S2} = 10\text{-}10 = 0\text{ v} > V_{T2}$

Q_1 is on , replaced with short circuit

Q_2 is off , replaced with open circuit







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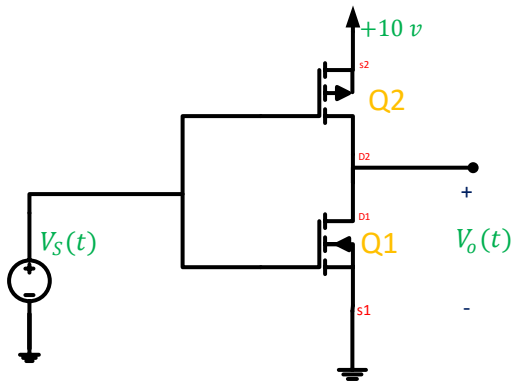
2) Let V_S(t) = 0 v

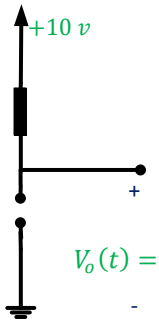
$V_{GS1} = V_{G1} - V_{S1} = 0 = 0\ v < V_{T1}$

Q_1 is off , replaced with open circuit

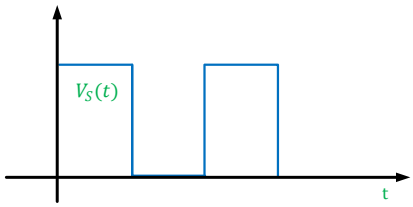
$V_{GS2} = V_{G2} - V_{S2} = 0\text{-}10 = -10\ v < V_{T2}$

Q_2 is off , replaced with short circuit

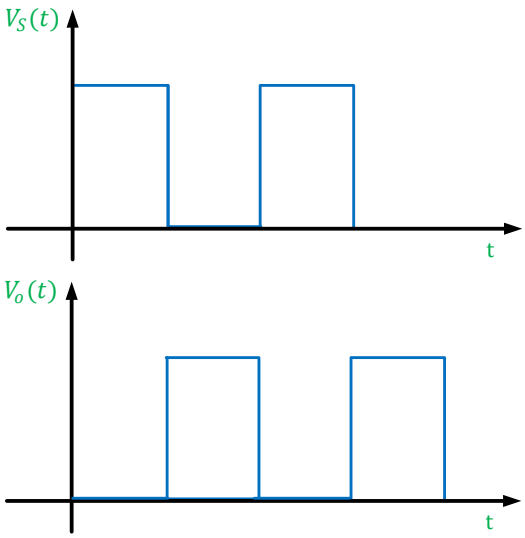




$V_o(t) = 10\ V$



Inverter = NOT GATE



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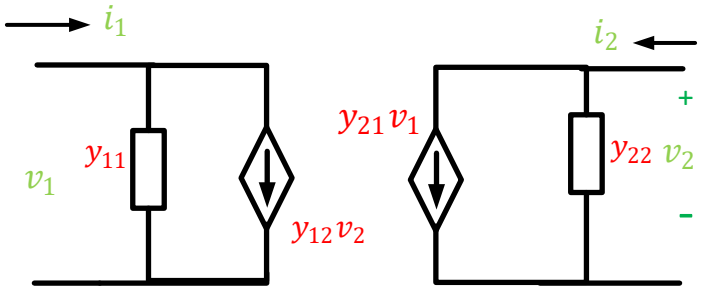
Ac small signal Equivalent for FET ← model derivation not required

$$i_1 = y_{11}v_1 + y_{12}v_2$$

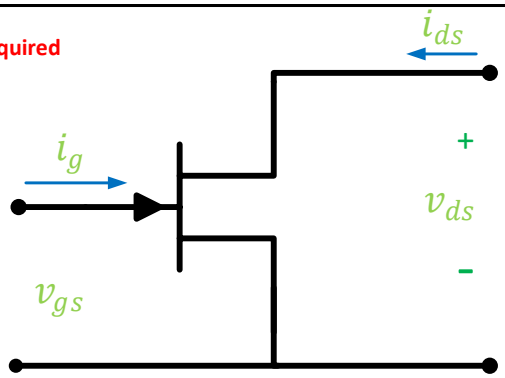
$$i_2 = y_{21}v_1 + y_{22}v_2$$



model derivation not required

$$i_g = y_{11}v_{gs} + y_{12}v_{ds}$$

$$i_{ds} = y_{21}v_{gs} + y_{22}v_{ds}$$



$$y_{11} = \frac{i_g}{v_{gs}}\Big|_{v_{ds}=0} = \frac{\Delta i_{G(t)}}{\Delta V_{GS(t)}}\Big|_{V_{DS(t)}=V_{DSQ}}$$

$\therefore y_{11} = 0$ (open circuit)

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model derivation not required

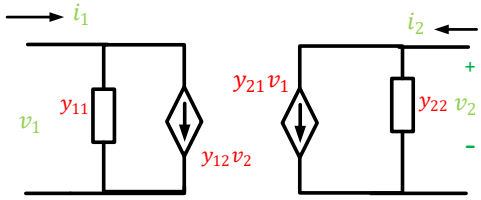
$$y_{12} = \frac{i_g}{v_{ds}}\Big|_{v_{gs}=0} = \frac{\Delta i_{G(t)}}{\Delta V_{DS(t)}}\Big|_{V_{GS(t)}=V_{GSQ}}$$

But $i_{G(t)}$=0

$\therefore y_{12} = 0$

$\therefore y_{12}v_{gs} = 0$

(open circuit)

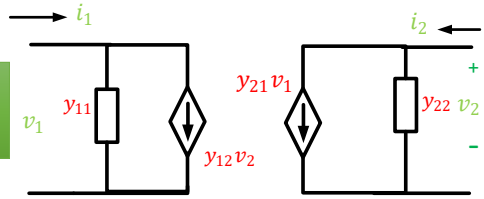


$$y_{22} = \frac{i_{ds}}{v_{ds}}\Big|_{v_{gs}=0} = \frac{\Delta i_{DS(t)}}{\Delta V_{DS(t)}}\Big|_{V_{GS(t)}=V_{GSQ}}$$

model derivation not required

$$\frac{1}{y_{22}} = r_{ds} = \frac{V_A}{I_{DSQ}}$$

$$y_{21} = \frac{i_{ds}}{v_{gs}}\Big|_{v_{ds}=0} = \frac{\Delta i_{DS(t)}}{\Delta V_{GS(t)}}\Big|_{V_{DS(t)}=V_{DSQ}}$$



$$y_{21} = \frac{d\, i_{DS(t)}}{d\, V_{GS(t)}}\Big|_Q$$

$y_{21} = g_m$; Forward Transconductance

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Definition: Transconductance g_m

For JFETs and DMOSFETs

$$g_m = \frac{\partial \mathrm{I_D}}{\partial \mathrm{V_{GS}}} = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}} \qquad g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

For EMOSFET

$$I_D = \mathrm{K}\left(V_{GS} - V_{GS(TH)}\right)^2 \Rightarrow g_m = \frac{\partial \mathrm{I_D}}{\partial \mathrm{V_{GS}}} = 2\mathrm{K}\left(V_{GS} - V_{GS(TH)}\right)$$

$$K = \frac{I_D}{\left(V_{GS} - V_{GS(TH)}\right)^2}$$

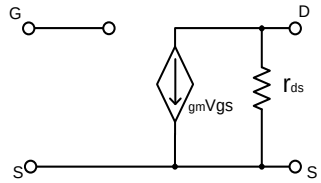
$$\left(V_{GS} - V_{GS(TH)}\right) = \sqrt{\frac{\mathrm{I_D}}{\mathrm{K}}}$$

$$\therefore g_m = 2K\sqrt{\frac{\mathrm{I_D}}{\mathrm{K}}} = 2\sqrt{\frac{\mathrm{I_D}K^2}{\mathrm{K}}} = 2\sqrt{\mathrm{I_D}K}$$

AC Small Signal Equivalent Circuit (MODEL Valid for all FET Types)

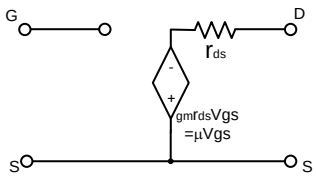
- In ac

$$g_m = \frac{i_d}{v_{gs}} \Rightarrow i_d = g_m v_{gs}$$



- Or

$\mu = g_m r_{ds}$ - amplification factor



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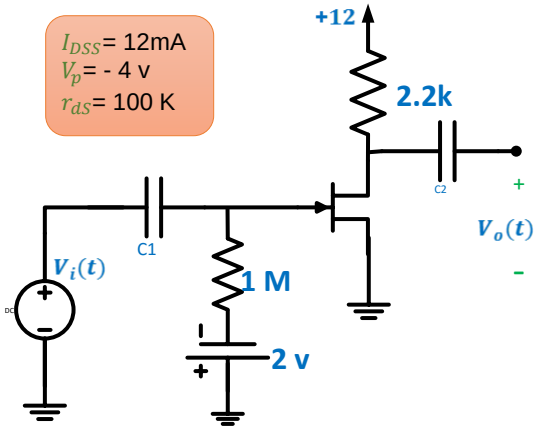
FET Ac Small Signal Amplifiers

- **1) Common Source Amplifier**

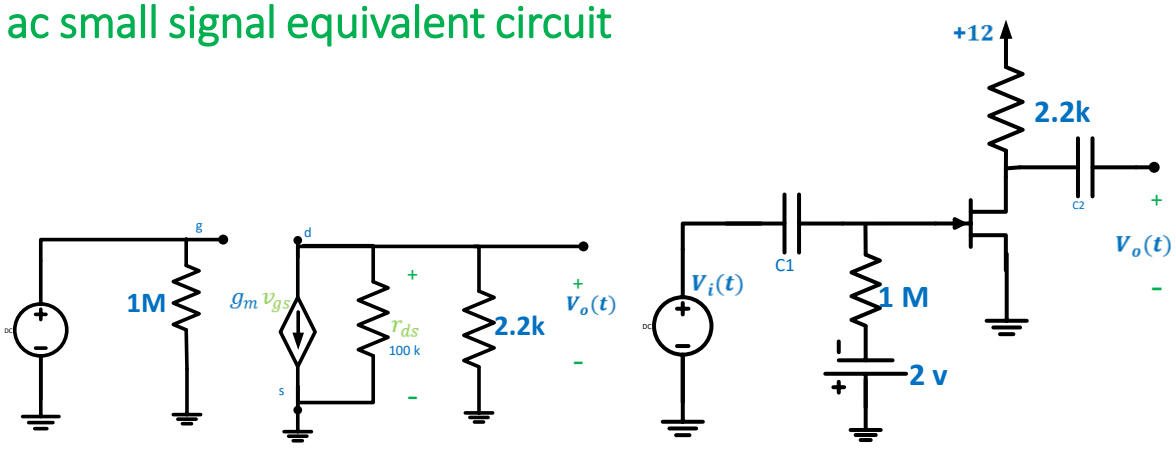
- $g_m = \frac{-2I_{DSS}}{V_p}\left(1 - \frac{V_{GS}}{V_P}\right)$

- V_{GS} = - 2 v

$\therefore g_m$ = 3m A/V



ac small signal equivalent circuit



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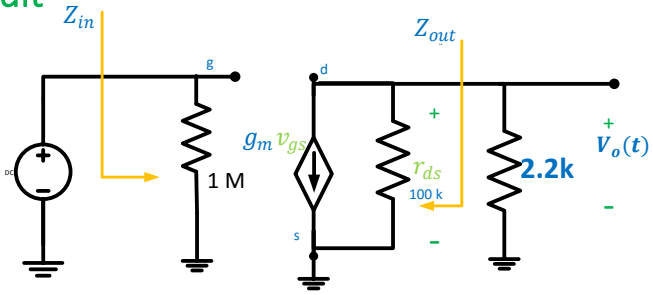
ac small signal equivalent circuit

$V_O = - g_m V_{gs}$(100K \\ 2.2K)

$V_{gs} = V_g - V_S$

$V_S = 0$

$V_g = V_i$



$A_v = \frac{V_O}{V_i} = - g_m$ (100K \\ 2.2K)

A_v = -6.6

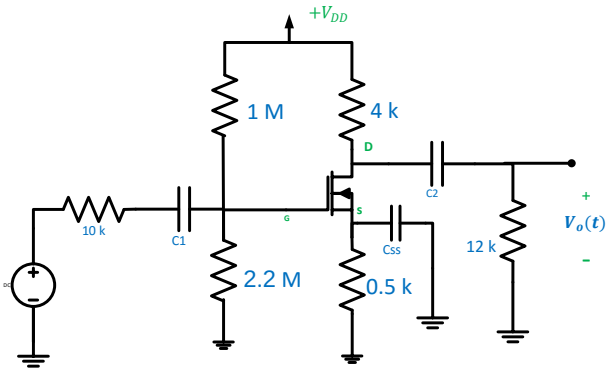
Z_i= 1MΩ

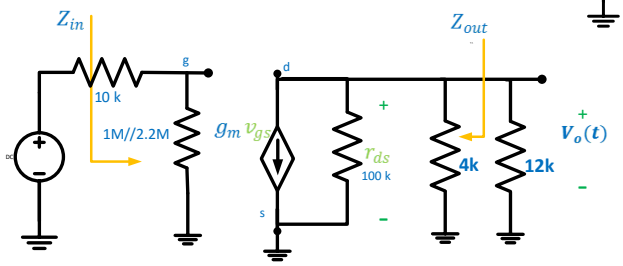
$Z_o = r_{ds}$ =100K

Example

g_m= 4 mS ; r_{ds} = 100KΩ

ac small signal equivalent circuit





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V_O= - $g_m V_{gs}$(100K \\ 4K \\ 12K)

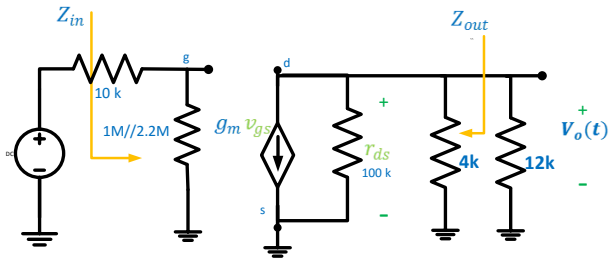
V_{gs}= V_g - V_S

$v_g = \frac{1M\backslash\backslash 2.2M}{1M\backslash\backslash 2.2M+10K} v_i \quad ; v_s = 0$

$A_v = \frac{V_O}{V_i}$= -11.48

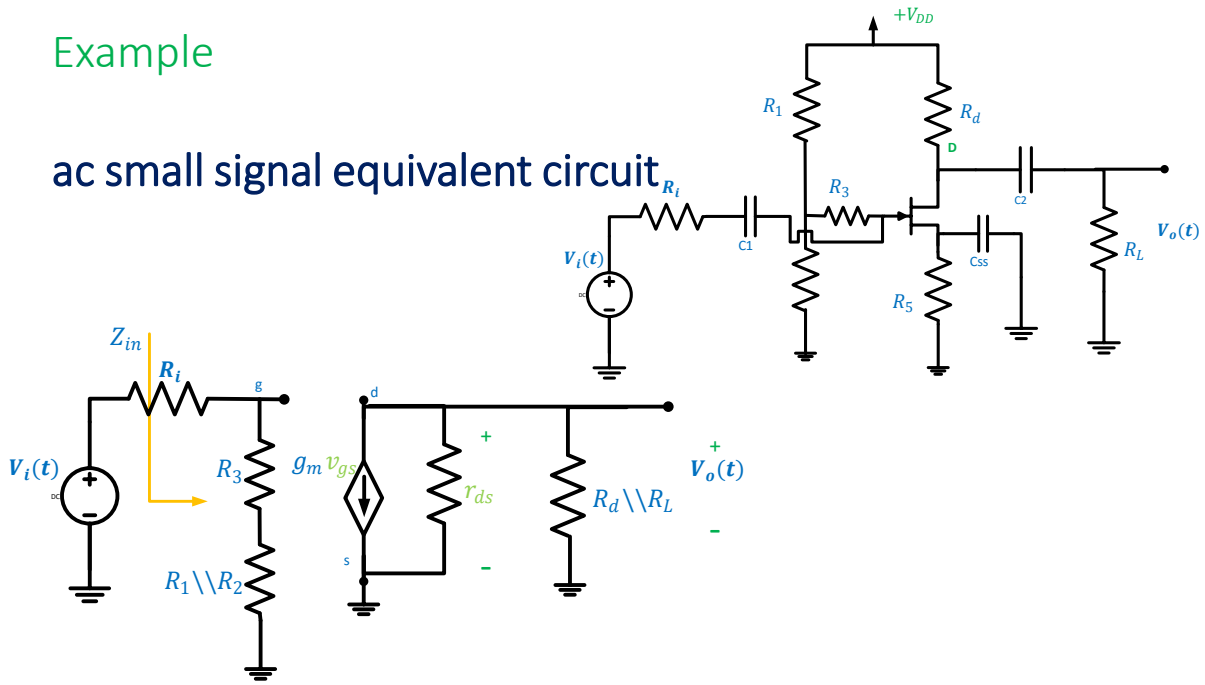
Z_i= 1M\\ 2.2M

Z_o= 100K \\ 4K



Example

ac small signal equivalent circuit



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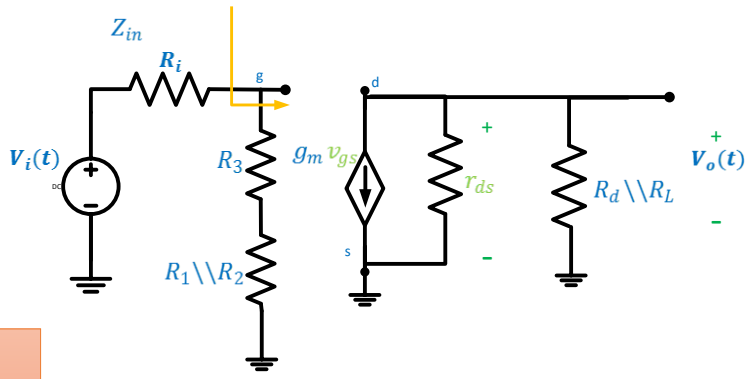
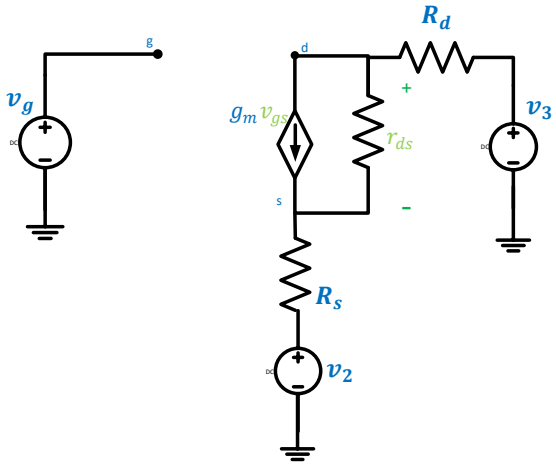
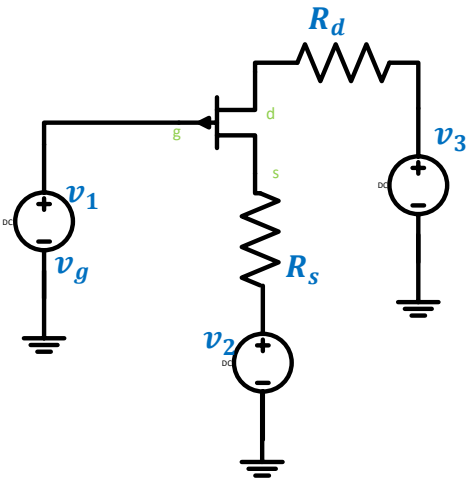


$$Z_i = R_3 + R_1 \backslash\backslash R_2$$

Impedance Reflection

ac small signal equivalent circuit





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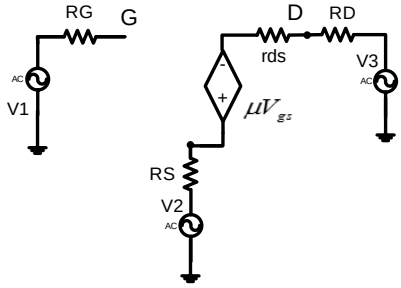
Impedance Reflection



KVL for the drain - source loop

$$V_3 - i_D R_D - i_D r_{ds} - i_D R_S + \mu V_{gs} - V_2 = 0 \quad \text{.....(1)}$$

but

$$V_{gs} = V_g - V_S = V_g - (i_D R_S + V_2) \quad \text{.....(2)}$$

substituting (2) in (1) yields:

$$V_3 - i_D R_D - i_D r_{ds} - i_D R_S + \mu(V_g - (i_D R_S + V_2)) - V_2 = 0$$

$$V_3 - i_D R_D - i_D r_{ds} - i_D R_S + \mu V_g - \mu i_D R_S - \mu V_2 - V_2 = 0$$

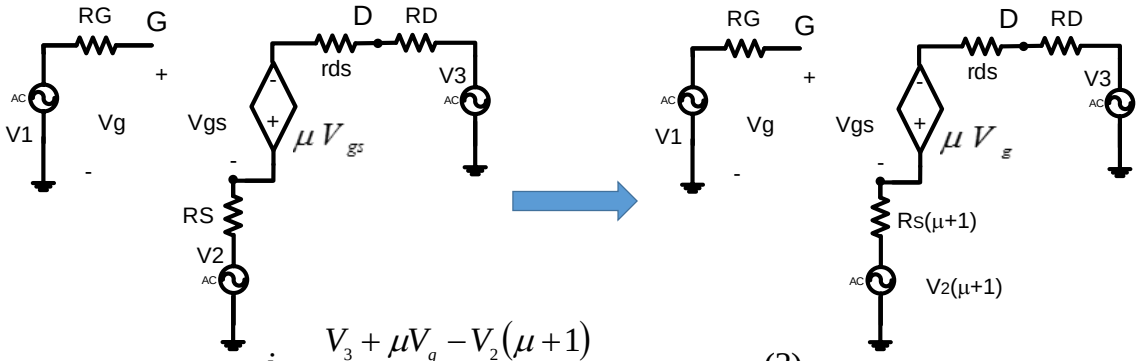
$$V_3 - i_D R_D - i_D r_{ds} - i_D R_S(\mu + 1) + \mu V_g - V_2(\mu + 1) = 0$$

$$i_D R_D + i_D r_{ds} + i_D R_S(\mu + 1) = V_3 + \mu V_g - V_2(\mu + 1)$$

$$V_3 - i_D R_D - i_D r_{ds} - i_D R_S + \mu(V_g - (i_D R_S + V_2)) - V_2 = 0$$

$$i_D = \frac{V_3 + \mu V_g - V_2(\mu + 1)}{R_D + r_{ds} + R_S(\mu + 1)} \quad \text{.....(3)}$$

(3) is the drain Equivalent circuit equation



$$i_D = \frac{V_3 + \mu V_g - V_2(\mu + 1)}{R_D + r_{ds} + R_S(\mu + 1)} \quad \text{.....(3)}$$

(3) is the drain Equivalent circuit equation

Reflection from Source to Drain

$$\mu V_{gs} \Rightarrow \mu V_g$$

$$R_S \Rightarrow R_S(\mu + 1)$$

$$V_2 \Rightarrow V_2(\mu + 1)$$

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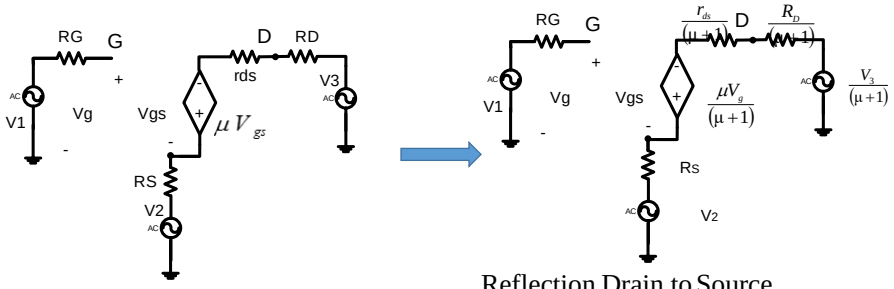


divide eq. (3) by $(\mu+1)$

$$i_D = \frac{\frac{V_3}{(\mu+1)} + \frac{\mu V_g}{(\mu+1)} - V_2}{\frac{R_D}{(\mu+1)} + \frac{r_{ds}}{(\mu+1)} + R_S} \quad \text{.....(4)}$$

(4) is the source equivalent circuit equation

Reflection Drain to Source

$$\mu V_{gs} \Rightarrow \frac{\mu V_g}{(\mu+1)}$$

$$R_D \Rightarrow \frac{R_D}{(\mu+1)}$$

$$r_{ds} \Rightarrow \frac{r_{ds}}{(\mu+1)}$$

$$v_3 \Rightarrow \frac{v_3}{(\mu+1)}$$

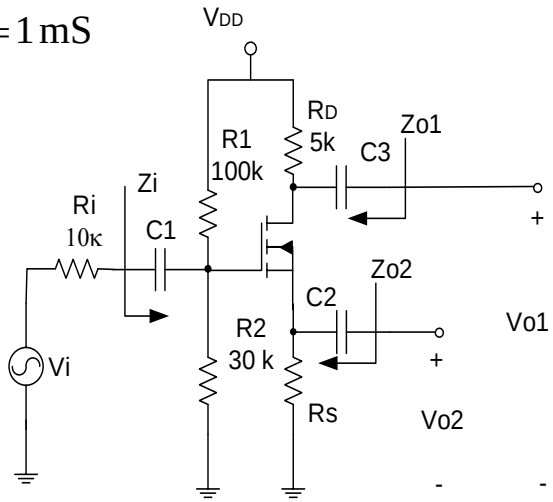
Example: Phase Splitting circuit

- Two outputs:
  - Vo1 from drain
  - Vo2 from source

$$r_{ds} = 100\,k\Omega$$

$$g_m = 1\,mS$$

Find A_V, A_I, Z_{O1}, Z_{O2} and Z_I



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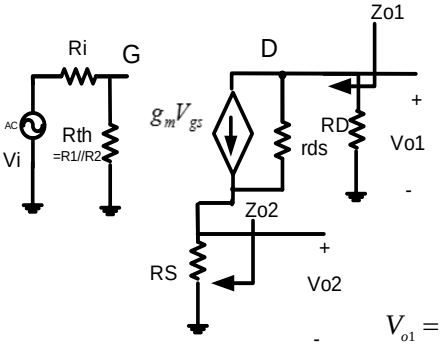
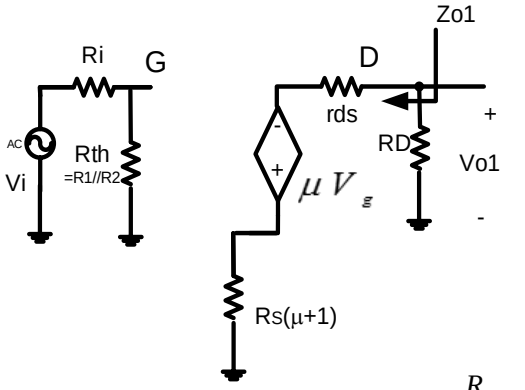
Solution: ac ss equivalent circuit

1) To Find Z_{O1}, V_{O1} Drain equivalent circuit is required since both of these quantities are seen from the drain



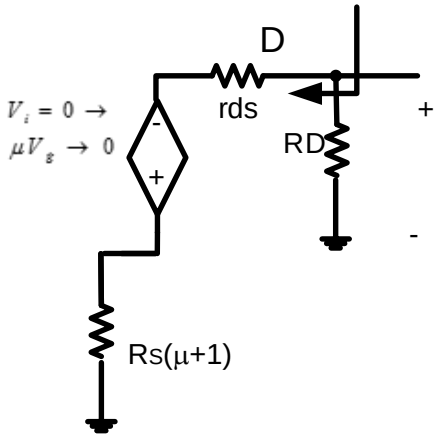


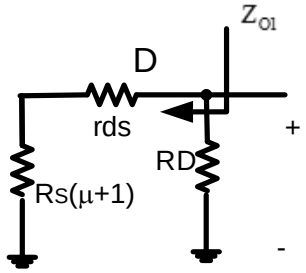
$$V_{o1} = \frac{R_D}{R_D + r_{ds} + R_S(\mu+1)}\left(-\mu V_g\right)$$

$$V_g = V_i \frac{R_{th}}{R_{th} + R_i}$$

$$Av = \frac{V_{o1}}{V_i} = (-\mu)\frac{R_D}{R_D + r_{ds} + R_S(\mu+1)} \cdot \frac{R_{th}}{R_{th} + R_i}$$

2) To Find $Z_{O1}\big|_{\substack{Vi=0\\Vg=0}}$





$$Z_{O1}\big|_{\substack{Vi=0\\Vg=0}} = R_D \,//\left[r_{ds} + R_s(\mu+1)\right]$$

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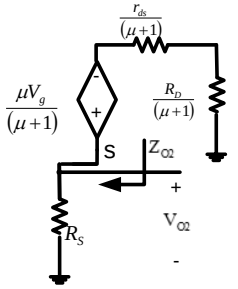
Solution: continued

3) To Find Z_{O2}, V_{O2} Source equivalent circuit is required since both of these quantities are seen from the source

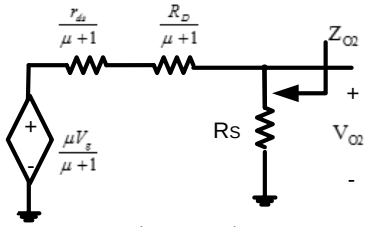


Reflection Drain to Source

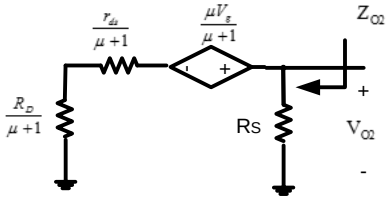
$$\mu V_{gs} \Rightarrow \frac{\mu V_g}{(\mu+1)}$$

$$R_D \Rightarrow \frac{R_D}{(\mu+1)}$$

$$r_{ds} \Rightarrow \frac{r_{ds}}{(\mu+1)}$$



$$V_{o2} = \frac{R_{|S}}{\frac{R_D + r_{ds}}{(\mu+1)} + R_S}\left(\frac{\mu V_g}{(\mu+1)}\right)$$

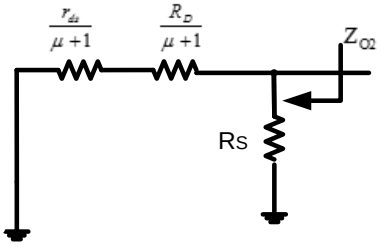


$$V_g = V_i \frac{R_{th}}{R_{th} + R_i}$$

$$A_{v2} = \frac{V_{o2}}{V_i} = \frac{\mu}{(\mu+1)} \frac{R_{|S}}{\frac{R_D + r_{ds}}{(\mu+1)} + R_S} \cdot \frac{R_{th}}{R_{th} + R_i}$$

Solution: continued

4) To Find $Z_{O2}\big|_{\substack{Vi=0 \\ Vg=0}}$



$$Z_{O2}\Big|_{\substack{Vi=0 \\ Vg=0}} = R_S \,//\left[\frac{r_{ds} + R_D}{(\mu+1)}\right]$$

If $r_{ds} = \infty$

$$Z_{O2}\Big|_{\substack{Vi=0 \\ Vg=0}}\Big|_{r_{ds}\to\infty} = R_S \,// \frac{1}{g_m}$$

$$\frac{R_d + r_{ds}}{\mu+1} = \frac{R_d + r_{ds}}{g_m r_{ds} + 1}$$

$$\lim_{r_{ds}\to\infty} \frac{R_d + r_{ds}}{g_m r_{ds} + 1} = \frac{1}{g_m}$$

$$Z_i = R_{th} = R_1 \,// \, R_2$$

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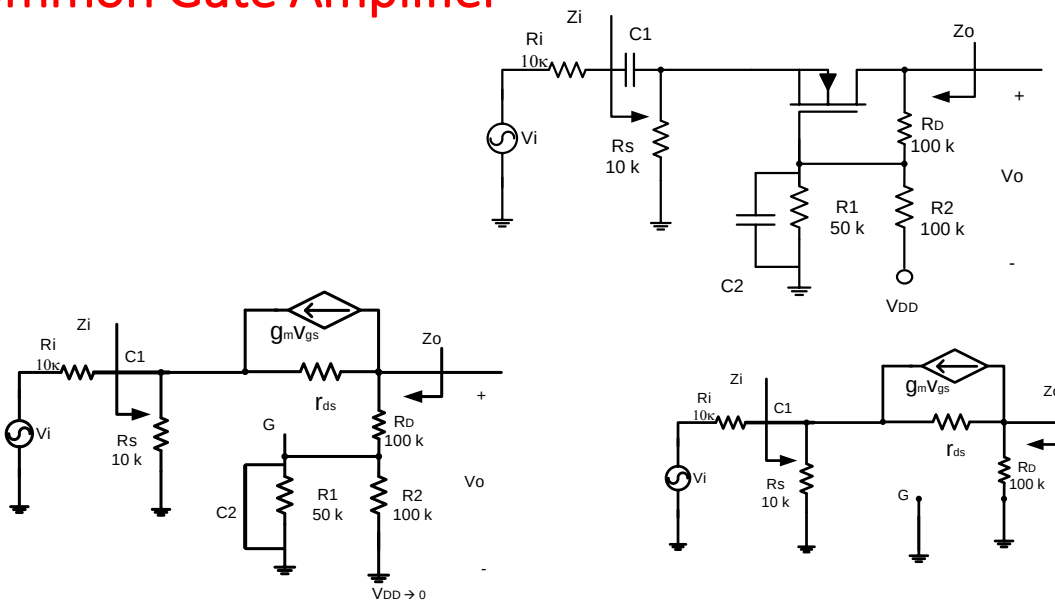
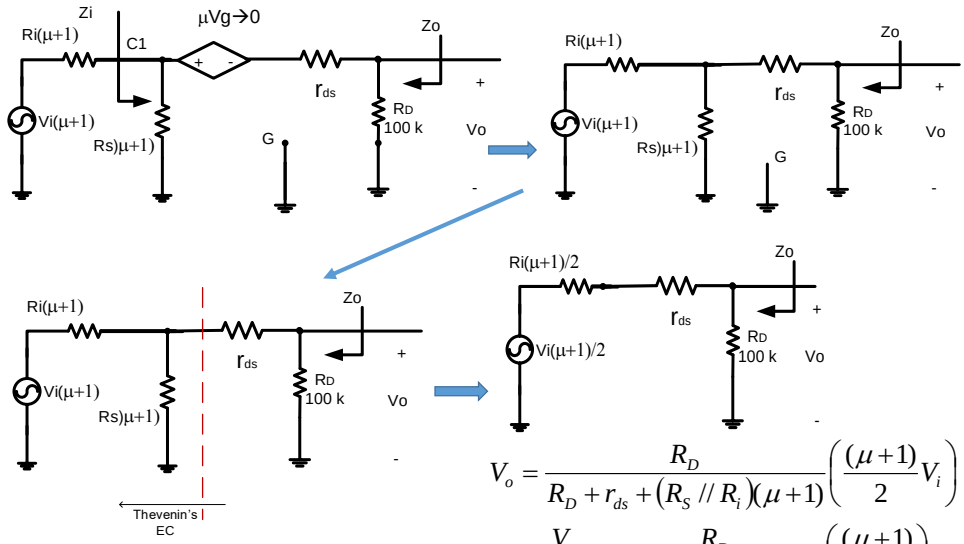
Common Gate Amplifier



Drain Equivalent circuit to find Vo and Zo



$$V_o = \frac{R_D}{R_D + r_{ds} + (R_S // R_i)(\mu+1)}\left(\frac{(\mu+1)}{2}V_i\right)$$

$$Av = \frac{V_o}{V_i} = \frac{R_D}{R_D + r_{ds} + 5k(\mu+1)}\left(\frac{(\mu+1)}{2}\right)$$

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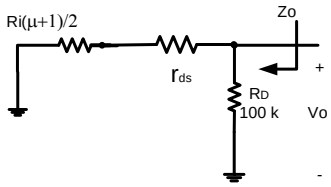
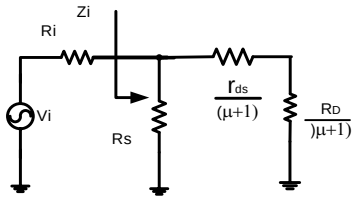
- Drain Equivalent circuit to find Vo and Zo



$$Z_O\big|_{Vi=0} = R_D \,//\left(r_{ds} + \frac{R_i(\mu+1)}{2} \right)$$

ENEE236

- To find Zi source equivalent circuit is needed



$$Z_i = R_S \,//\left[\frac{r_{ds} + R_D}{(\mu+1)} \right]$$

$$Z_i\big|_{r_{ds}\to\infty} = R_S \,// \frac{1}{g_m}$$

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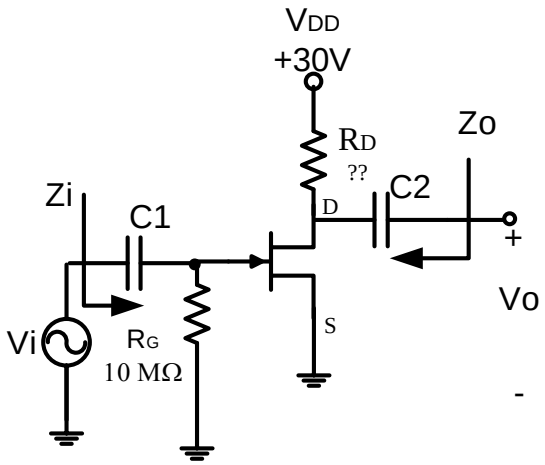
FET Amplifier Design (Important)

- Design a fixed bias network such that the ac voltage gain $|Av| = 10$, i.e. find value of R_D

$V_P = -4\,V$

$I_{DSS} = 10\,mA$

$r_{ds} = 50\,k\Omega$



Solution

$V_{GS} = V_G - V_S = 0V$

$I_D = I_{DSS}\left(1 - \frac{0}{-4}\right)^2 = I_{DSS} = 10mA$

For JFETs

$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$

$= \frac{2(10mA)}{|-4|}\left[1 - \frac{0}{-4}\right] = 5\,mS$

$V_{gs} = V_i$

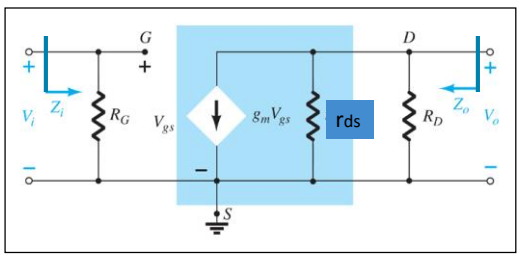
$A_v = \frac{V_o}{V_i}$

$V_o = -g_m V_{gs}(r_{ds}||R_D)$

$V_o = -g_m V_i(r_{ds}||R_D)$

$|A_v| = \left|\frac{V_o}{V_i}\right| = |-g_m(r_{ds}||R_D)|$

ac ss equivalent circuit



Since Av & gm are known , then

$|A_v| = \left|\frac{V_o}{V_i}\right| = |-g_m(r_{ds}||R_D)| = 10$

$\therefore (r_{ds}||R_D) = \frac{10}{g_m} = \frac{10}{5\,mS} = 2\,k\Omega$

Substitute $r_{ds} = 50\,k\Omega$

$(r_{ds}||R_D) = \frac{r_{ds}.R_D}{r_{ds} + R_D} = \frac{50\,k\Omega.R_D}{50\,k\Omega + R_D} = 2\,k\Omega$

$\rightarrow R_D = \frac{2\,k\Omega \;.50\,k\Omega}{48\,k\Omega} = 2.08\,k\Omega$

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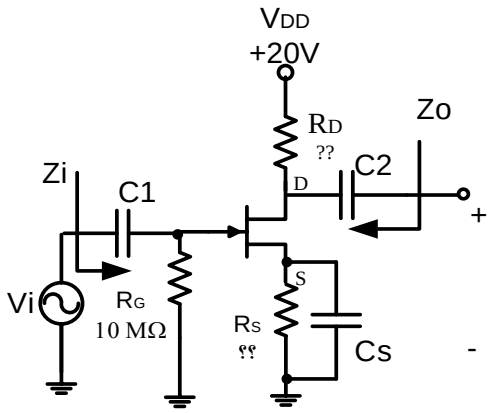
Design Example 2 (Important)

Choose the values of R_D and R_S that will result in voltage gain $|Av| = 8$ using the value of g_m defined at $V_{GSQ} = \frac{1}{4}V_p$

$V_P = -4\,V$

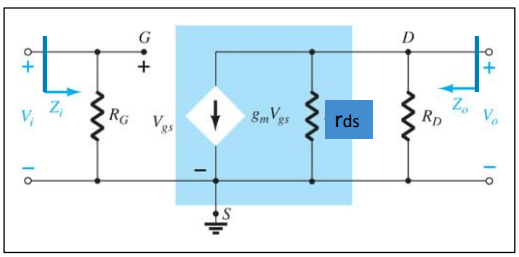
$I_{DSS} = 10\,mA$

$r_{ds} = 50\,k\Omega$



Solution (value of R_D?)

ac ss equivalent circuit



$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$= \frac{2(10mA)}{|-4|}\left[1 - \frac{-1}{-4}\right] = 3.75\,mS$$

$$V_{gs} = V_i$$

$$A_v = \frac{V_o}{V_i}$$

$$V_o = -g_m V_{gs}(r_{ds}||R_D)$$

$$V_o = -g_m V_i(r_{ds}||R_D)$$

$$|A_v| = \left|\frac{V_o}{V_i}\right| = |-g_m(r_{ds}||R_D)|$$

Since Av & gm are known , then

$$|A_v| = \left|\frac{V_o}{V_i}\right| = |-g_m(r_{ds}||R_D)| = 8$$

$$\therefore (r_{ds}||R_D) = \frac{8}{g_m} = \frac{8}{3.75\,mS} = 2.133\,k\Omega$$

Substitute $r_{ds} = 50\,k\Omega$

$$(r_{ds}||R_D) = \frac{r_{ds}.R_D}{r_{ds} + R_D} = \frac{50\,k\Omega.R_D}{50\,k\Omega + R_D} = 2.133\,k\Omega$$

$$\rightarrow R_D = \frac{2.133\,k\Omega\ .50\,k\Omega}{47.867\,k\Omega} = 2.22\,k\Omega$$

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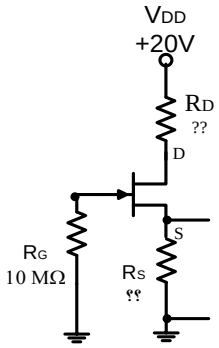
Value of Rs?

The value of R_S is determined from DC analysis



Given

$$V_{GS} = V_G - V_S = \frac{1}{4}V_p = -1$$

$$V_G = 0$$

$$V_S = I_D R_S = 1$$

$$but\ I_D = I_{DSS}\left(1 - \frac{-1}{-4}\right)^2 = I_{DSS}.0.5625 = 5.625mA$$

$$\therefore R_S = \frac{V_S}{I_D} = \frac{1\ \text{V}}{5.625\ \text{mA}} = 177.8\ \Omega$$

Design Example 3

Choose the values of R_D and R_S that will result in

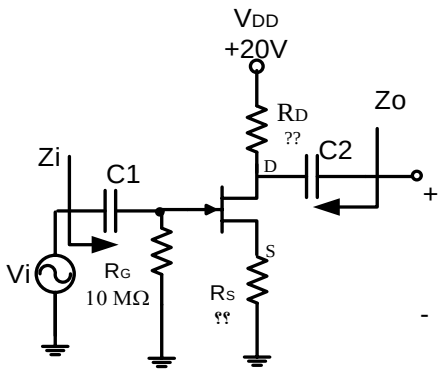
voltage gain $|Av| = 8$ using the value of g_m defined at $V_{GSQ} = \frac{1}{4}V_p$

$V_p = -4\ \text{V}$

$I_{DSS} = 10\ \text{mA}$

$r_{ds} = \infty$

Note: This is the same previous example except that no Cs (source capacitor)



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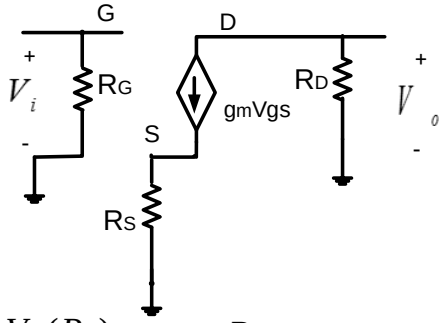
Solution

$V_{GS} = -1\,\text{V}$

$I_D = 5.625mA$

$g_m = 3.75\,\text{m}S$ (from previous example)

ac ss equivalent circuit



$$A_v = \frac{V_o}{V_i}$$

$$V_o = -g_m V_{gs}(r_{ds}||R_D)$$

$$V_{gs} = V_g - g_m V_{gs} R_S$$

$$V_g = V_i$$

$$V_{gs} = V_i - g_m V_{gs} R_S$$

$$V_i = V_{gs} + g_m V_{gs} R_S$$

$$V_o = \frac{-g_m V_{gs}(R_D)}{V_{gs} + g_m V_{gs} R_S} = \frac{-g_m R_D}{1 + g_m R_S}$$

$$|A_v| = \left|\frac{V_o}{V_i}\right| = \left|\frac{-g_m R_D}{1 + g_m R_S}\right| = 8$$

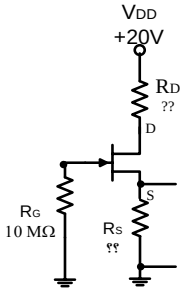
Since Av & gm and R_S are known , then

$R_S = 180\,\Omega$ (based on DC analysis)

$\therefore R_D = 3.573\,\text{k}\Omega$

Value of Rs?

The value of R_S is determined from DC analysis



Given

$$V_{GS} = V_G - V_S = \frac{1}{4}V_p = -1$$

$$V_G = 0$$

$$V_S = I_D R_S = -1$$

$$but\ I_D = I_{DSS}\left(1 - \frac{-1}{-4}\right)^2 = I_{DSS}.0.5625 = 5.625mA$$

$$\therefore R_S = \frac{V_S}{I_D} = \frac{1\ \text{V}}{5.625\ \text{mA}} = 177.8\ \Omega$$

choose standard value 180Ω

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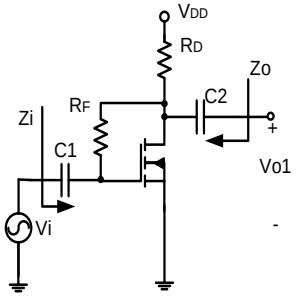
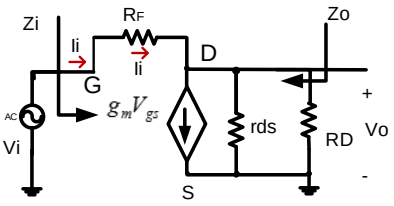
Drain Feedback Configuration (self study)





$$I_i = g_m V_{gs} + \frac{V_o}{R_D // r_{ds}}$$

$$V_{gs} = V_i$$

$$I_i = g_m V_i + \frac{V_o}{R_D // r_{ds}}$$

$$I_i - g_m V_i = \frac{V_o}{R_D // r_{ds}}$$

$$V_o = (I_i - g_m V_i)(R_D // r_{ds})$$

also

$$I_i = \frac{V_i - V_O}{R_F}$$

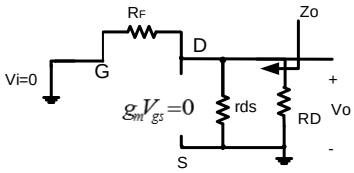
$$= \frac{V_i - ((I_i - g_m V_i)(R_D // r_{ds}))}{R_F}$$

$$I_i R_F = V_i - ((I_i - g_m V_i)(R_D // r_{ds}))$$

$$V_i[1 + g_m(R_D // r_{ds})] = I_i[R_F + (R_D // r_{ds})]$$

$$\therefore$$

$$Z_i = \frac{V_i}{I_i} = \frac{[R_F + (R_D // r_{ds})]}{[1 + g_m(R_D // r_{ds})]}$$



$$Z_{o|_{vi=0}} = R_D // r_{ds} // R_F$$

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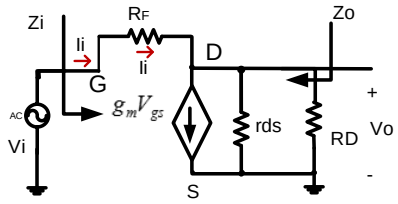

$$I_i = g_m V_{gs} + \frac{V_o}{(R_D // r_{ds})}$$

$$V_{gs} = V_i \quad also \quad I_i = \frac{V_i - V_O}{R_F}$$

$$\frac{V_i - V_O}{R_F} = g_m V_{gs} + \frac{V_o}{(R_D // r_{ds})}$$

$$\frac{V_i}{R_F} - \frac{V_O}{R_F} = g_m V_i + \frac{V_o}{(R_D // r_{ds})}$$

$$\frac{V_i}{R_F} - g_m V_i = \frac{V_o}{(R_D // r_{ds})} + \frac{V_O}{R_F}$$

$$V_i\left(\frac{1}{R_F} - g_m\right) = V_o\left(\frac{1}{(R_D // r_{ds})} + \frac{1}{R_F}\right)$$

$$A_V = \frac{V_o}{V_i} = \frac{\left(\frac{1}{R_F} - g_m\right)}{\left(\frac{1}{(R_D // r_{ds})} + \frac{1}{R_F}\right)}$$

Common Source Amplifier :Design

- **Design a Common source MOSFET Amplifier to provide a voltage gain $\left|\frac{V_o}{Vi}\right| = 10$, between a small signal voltage source having a resistance 10kΩ and load $R_L = 10k$**

and Zi = 1MΩ.

The MOSFET has rds = 20k , VT = 1.419 V , Kn = $\frac{2\ mA}{V^2}$,

and IDS = 5mA.

Assume VDD = 24V.

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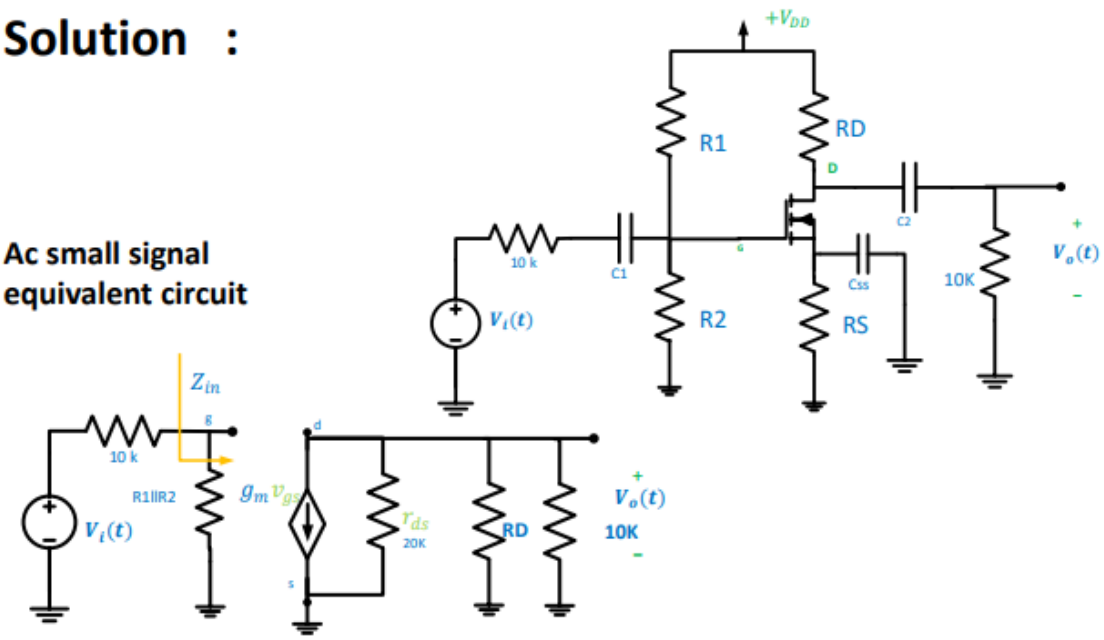
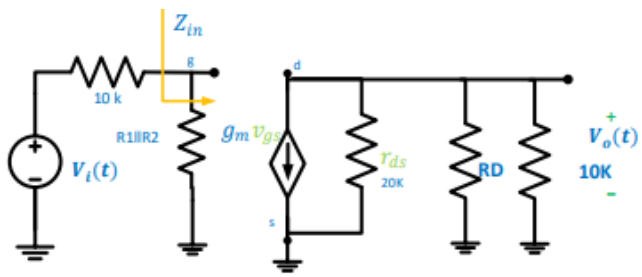
Solution :

Ac small signal equivalent circuit





$$v_O = -g_m v_{gs}(R_D \,\backslash\backslash\, r_{ds} \,\backslash\backslash\, 10K)$$

$$v_{gs} = v_g - v_S$$

$$vg = \frac{R1 // R2}{R1 // R2 + Ri} Vi = \frac{Zi}{Zi + Ri} Vi = \frac{1000k}{1000k + 10k} Vi$$

$$vg \cong Vi \qquad vs = 0 \qquad \therefore A_v = -g_m (R_D \,\backslash\backslash\, 20K \,\backslash\backslash\, 10K)$$

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$\therefore A_v = -g_m (R_D \,\backslash\backslash\, 20K \,\backslash\backslash\, 10K)$

Using $gm = 2\sqrt{Kn\, IDS}$ → gm = 6.23m℧

For Av = -10 → RD = 2.1KΩ

VDS = 8.7V Pinch off region

DC Analysis

Let VS = VDD/5 = 4.8V → RS = 0.96K Ω

$But\ I_{DS} = K_n(V_{GS} - V_T)^2$

$For\ I_{DS}$ = 5mA ∴ VGS = 3V

$V_{GS} = V_G - V_S$

∴ VG = 7.8V

NOW

$V_G = \frac{R2}{R2+R1}(24)$ = 7.8V

Z_i = R1\\ R2 = 1M Ω

Solving for R1 and R2 , we get

R1 = 3.1M Ω

R2 = 1.48M Ω

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