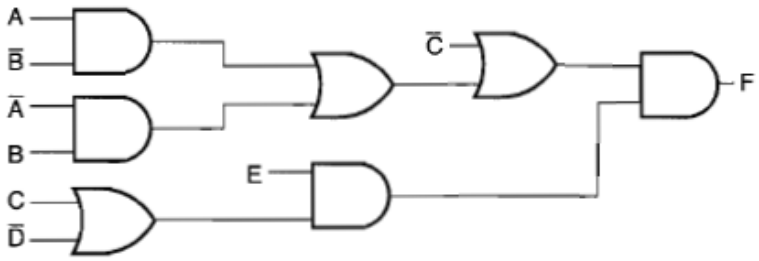
ENCS2340 | Section 2 | Fall 2024/2025
Chapter 3-4
Extra Exercises - 01

1. Show logic diagrams for implementing the logic circuit shown (without any modification) using each of the following:



   a. NAND gates Only
   b. NOR gates Only

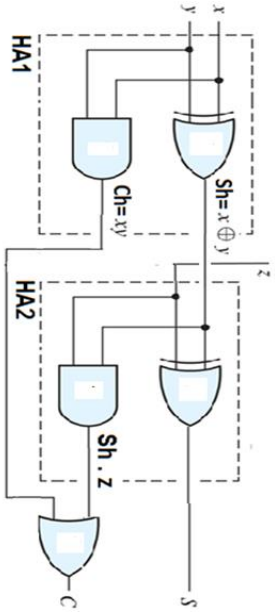
   Assume that both the variables and their complements are readily available.

2. Given $F(w,x,y,z) = \Sigma(0,2,5,7,8,10,13,15)$
   a. Using K-maps, verify that the following are optimized SOP implementations of F and F'
      $F = xz + \bar{x}\,\bar{z}$, $\bar{F} = x\bar{z} + \bar{x}\,z$
   b. Use the results in (a) to implement F in each of the following 2-level forms (Give a logic diagram in each case, assuming that both the variables and their complements are readily available):
      i. NAND-AND ii. NOR-OR
      iii. NAND-NAND iv. NOR-NOR
      v. AND-OR vi. AND-NOR
      vii. OR-NAND viii. OR-AND

3. We would like to design a combinational circuit that counts the number of 0s in a 4-bit binary input X (=X3X2X1X0). The output representing the number of 0s is Y (=…Y1Y0). X0 and Y0 are the LSBs.

   a. Give the truth table for the circuit
   b. Give an optimized SOP expression for each of circuit outputs using K-maps if required.

4. In the full adder (FA) circuit shown opposite, let propagation delays for the various gates be as follows: OR: 2.5 ns, AND: 2 ns, XOR: 5.5 ns.



   4.1. We would like to use the FA given as a building block to implement:

   a. A 1-bit adder
   b. A 2-bit ripple-carry adder

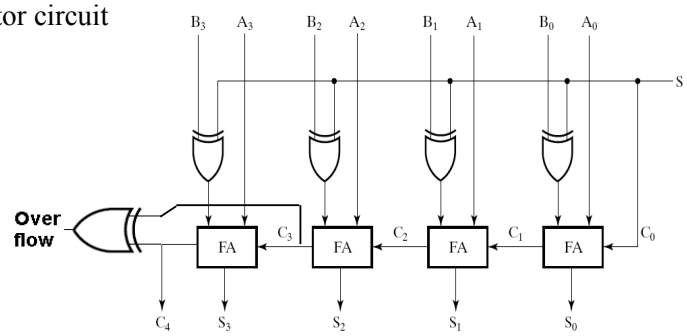
   The two inputs to an adder are A= …A1A0 and B= …B1B0 and an input carry Cin = 0. The Outputs are sum S=…S1S0 and an end carry Cout.

   For each of the two cases above:

   - Mark the critical propagation delay path on a circuit diagram of the adder.
   - Calculate the time delay for the adder in ns (based on the critical path).

   4.2. Calculate the throughput rate (= number of additions per second) for the 2-bit adder.

5. For the 4-bit 2's complement adder/subtractor circuit shown opposite:



Show all work required to perform the following operations in the 2's complement notation **and then** complete the missing information in the table below:

	Inputs			Output		Overflow Occurred? (Yes/No)	Is the result correct? (Yes/No)
	A	B	Subtract/$\overline{\text{Add}}$ [O/P = (A-B) or (A+B)]	C4	S (binary)		
a	0010	0101	0				
b	1100	1011	1				
c	0111	1101	0				
d	1100	0110	1				