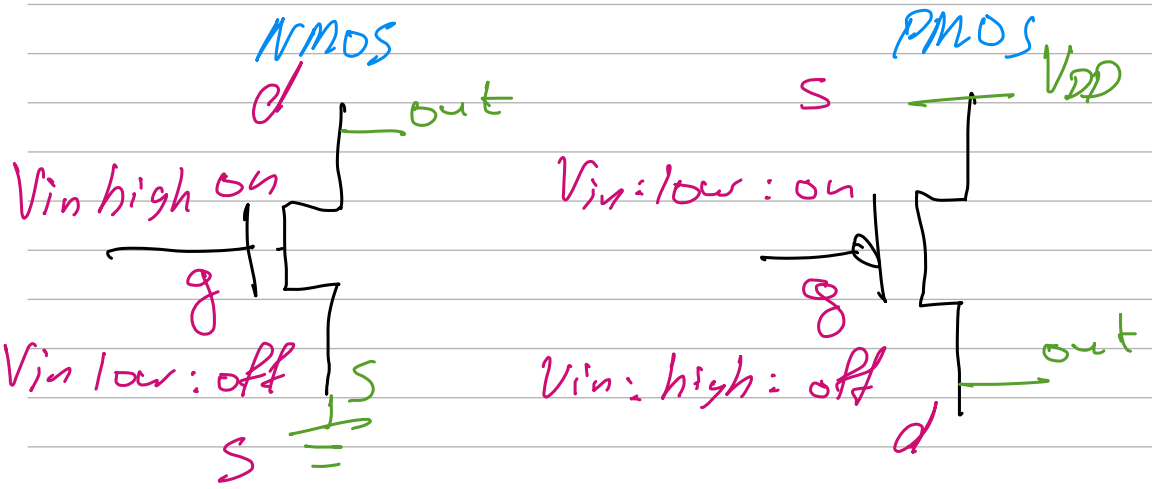
IC NOTES

References:

1. Digital Integrated Circuits
2. CMOS VLSI Design

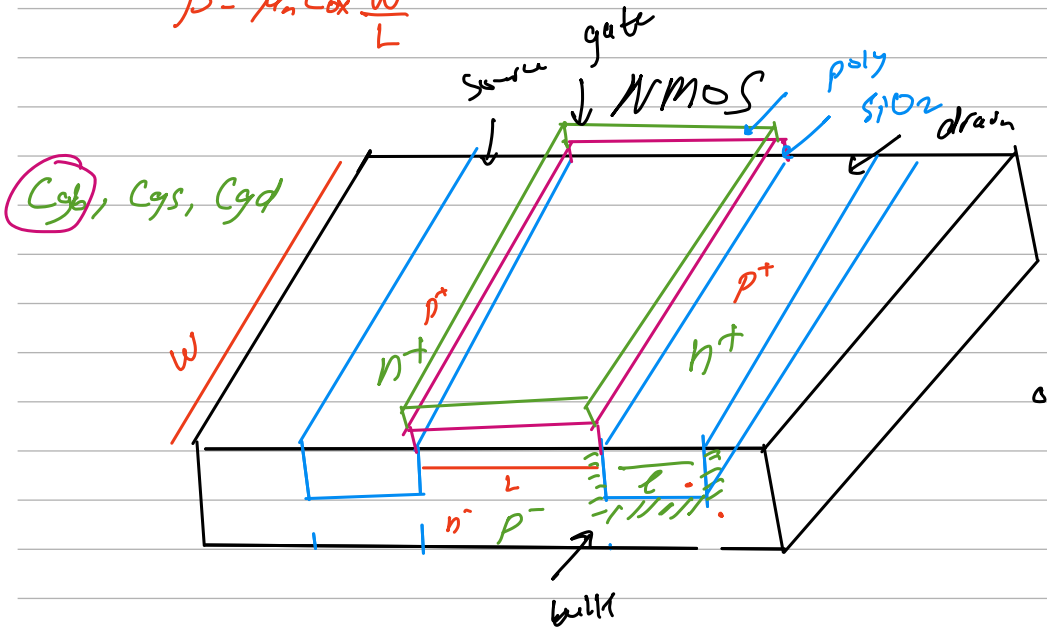
Prepared By: Ghazi Haj Qassem

MOS Transistor Theory



$$I_{DS} = \begin{cases} 0 & , V_{gs} < V_{tn} \quad \text{off (cutoff)} \\ \beta (V_{gs} - V_{tn} - V_{ds}/2) V_{ds} & , V_{gs} > V_{tn},\ V_{ds} \geq V_{gs} - V_{tn} \quad \text{linear (on)} \\ \frac{\beta}{2} (V_{gs} - V_{tn})^2 & , V_{gs} > V_{tn},\ V_{ds} > V_{gs} - V_{tn} \quad \text{saturation} \end{cases}$$

$$\beta = \mu_n C_{ox} \frac{W}{L}$$



C_{gb}, C_{gs}, C_{gd}

$$C = \frac{\varepsilon A}{d}$$

$$C_{gb} = \frac{\varepsilon_{ox} WL}{t_{ox}}$$

0.3 μm process

$$\lambda = \frac{L}{2}$$

$$C_{db} = \frac{\varepsilon L (\mu m)}{t}$$

C_{db} (/μm) $C = C_{db} W$

C_{sb} (/μm) $C = C_{sb} W$

C_{gb} (/μm²) $C = C_{gb} WL$ W/L

C_{ox}

Example:

Consider the NMOS inverter given.

V_{OL} : minimum output voltage

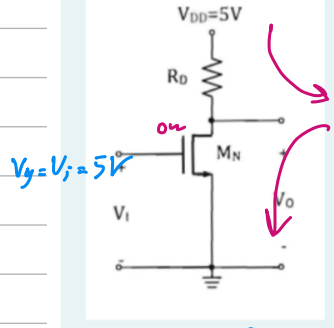
VDD = 5 V, R D = 22 Hohm

Vtn =:1.5 V, KN = 100 uA/V2 $= 0.1 mA/V^2$

Detrmine VOL(min) when Vi =Vdd

$V_{OL} = ?.5V$

Examle for answer to be written **VOL(min)=9.4v**



$V_g = V_i = 5V$

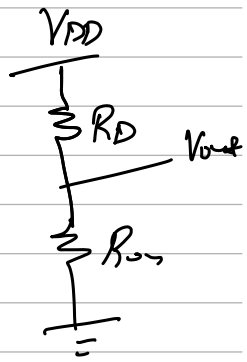
$V_s = 0$

$R_{on} = \frac{1}{2K_n(V_{DD}-V_{tn})} = \frac{1}{2(0.1)(5-1.5)} = \frac{1}{0.2(3.5)} = 1.43K\Omega$ (mA/V²)

$V_{OL} = \frac{R_{on}}{R_D+R_{on}} V_{DD} = 0.3V$

$0.3V < V_{gs} - V_{tn} = 3.5V$

$V_{ds} > V_{gs} - V_{tn} = ?.5V$



Example:

In the following circuit, the capacitance of CL is 50 fF.

CL is initially charged to 2.5 V. At time zero, its gate is attached ground, as shown in the figure. VT P = -0.5 V.

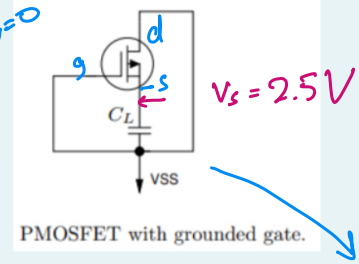
1) If we replace the PMOSFET with a 2 kΩ resistor, how long does it take for the capacitor to discharge to 1.25 V? *Your answer should be be like this (1)120ps)*

2) If we consider the transistor cut-off, what is the final voltage of the capacitor?

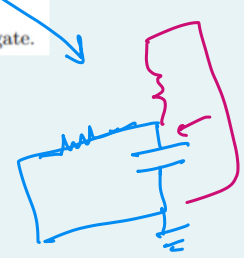
Your answer should be like this (2) 200v)

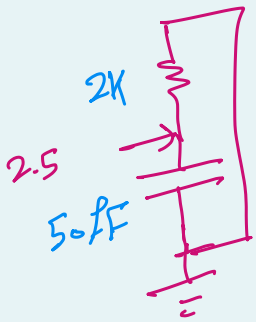
$C_L = 50fF$

$V_{tp} = -0.5V$



PMOSFET with grounded gate.





$t = \ln 2 \tau$

$V = V_0 e^{-\frac{t}{\tau}}$

$\frac{1}{2}V_0 = V_0 e^{-\frac{t}{\tau}}$

$t = \ln 2 \tau$

$= \ln 2 RC$

$= \ln 2 (2M)(50fF)$

$= 0.69(100 \times 10^{-12})$

$= 69 \times 10^{-12} = 69ps$

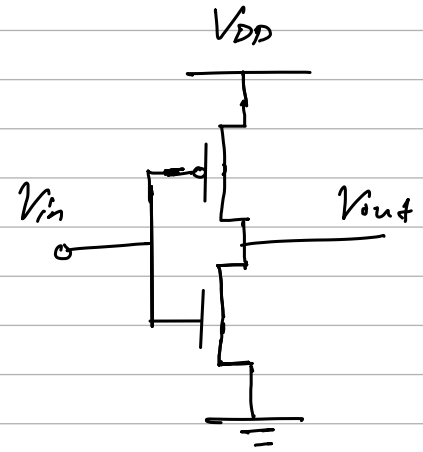
- A. 2)2.0v
- B. 2)2.25v
- C. 1) 69ps
- D. 1) 0.69ps
- E. 2)0.5v
- F. 1) 9ps
- G. 2)2.5v

$V_{gs} > V_{tp}$ $V_g - V_s > V_{tp} \Rightarrow -V_s > V_{tp} \Rightarrow V_s < -V_{tp} = 0.5V$

CMOS Inverter Operation

TABLE 2.2 Relationships between voltages for the three regions of operation of a CMOS inverter

	Cutoff	Linear	Saturated
nMOS	$V_{gsn} < V_{tn}$	$V_{gsn} \geq V_{tn}$	$V_{gsn} > V_{tn}$
	$V_{in} < V_{tn}$	$V_{in} > V_{tn}$	$V_{in} > V_{tn}$
		$V_{dsn} < V_{gsn} - V_{tn}$	$V_{dsn} > V_{gsn} - V_{tn}$
		$V_{out} < V_{in} - V_{tn}$	$V_{out} > V_{in} - V_{tn}$
pMOS	$V_{gsp} > V_{tp}$	$V_{gsp} \leq V_{tp}$ $V_g - V_s < V_{tp}$	$V_{gsp} < V_{tp}$
	$V_{in} > V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$ $V_g < V_{tp} + V_s$ $V_{in} < V_{DD} + V_{tp}$	$V_{in} < V_{tp} + V_{DD}$
	$V_g - V_s > V_{tp}$	$V_{dsp} > V_{gsp} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$
	$V_g > V_{tp} + V_s$ $V_{in} > V_{tp} + V_{DD}$	$V_{out} > V_{in} - V_{tp}$	$V_{out} < V_{in} - V_{tp}$

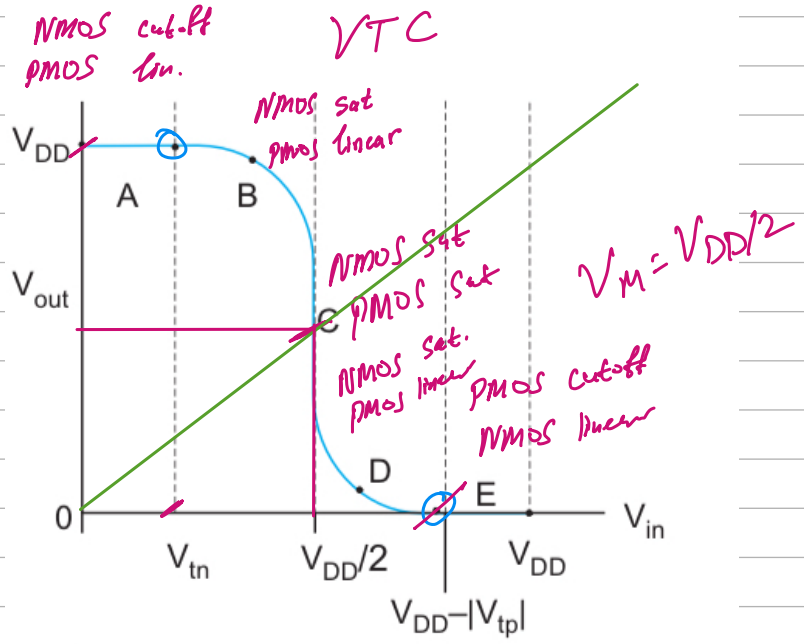


V_{in}	V_{out}
V_{DD} "1"	GND "0"
GND "0"	V_{DD} "1"

VTC of CMOS Inverter

TABLE 2.3 Summary of CMOS inverter operation

Region	Condition	p-device	n-device	Output
A	$0 \leq V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \leq V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \leq V_{DD} - \lvert V_{tp} \rvert$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	cutoff	linear	$V_{out} = 0$



① Switching Threshold (V_M): defined as the point where $V_{IN} = V_{OUT}$.

→ V_M is desired to be around the middle of the voltage swing ($V_M = V_{DD}/2$ for inverter)

→ This results in comparable high and low noise margins.

→ $W_p \uparrow$: $V_M \uparrow$, $W_n \uparrow$: $V_M \downarrow$

② Noise Margins

* V_{IH}, V_{IL} are defined when $\frac{dV_{out}}{dV_{in}} = -1$ (slope = -1).

V_{OH}, V_{OL}

V_{OH}: min output voltage

V_{IH}: min input voltage

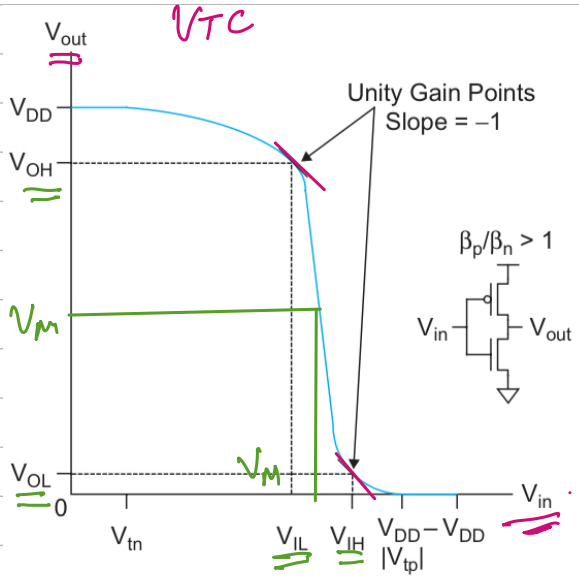
V_{IL}: max low input voltage

V_{OL}: max (low) output voltage

$W_n \uparrow$ $V_M \downarrow$

$W_p \uparrow$ $V_M \uparrow$

VTC



$NM_H = V_{OH} - V_{IH}$

V_{OH} — high region — V_{IH} — undefined — V_{IL} — low region — V_{OL}

$NM_L = V_{IL} - V_{OL}$

C. arrange the terms VOHmin, VIHmin, VILmax and VOLmax, and arrange them from lowest value to highest value. **(2 pts)**

$V_{OLmax} \leq V_{ILmax} \leq V_{IHmin} \leq V_{OHmin}$

FIGURE 2.30 CMOS inverter noise margins

Example:

Question **6**

Not answered

Marked out of 1.00

Flag question

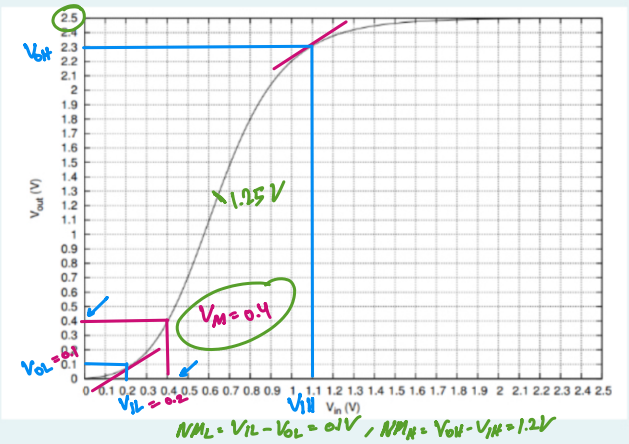
Consider the following transfer curve

What are its NMH and NML?

What is VM

* gain in buffer $\left(\frac{V_{out}}{V_{in}}\right) = 1$. Hence, slope = 1.

On the other hand, inverter gain = slope = -1.



$NM_L = V_{IL} - V_{OL} = 0.1V$, $NM_H = V_{OH} - V_{IH} = 1.2V$

NML ≈ Choose...

VM ≈ Choose...

NMH ≈ Choose...

The correct answer is: NML ≈ → 0.25 V, VM ≈ → 0.77 V, NMH ≈ → 1.5 V

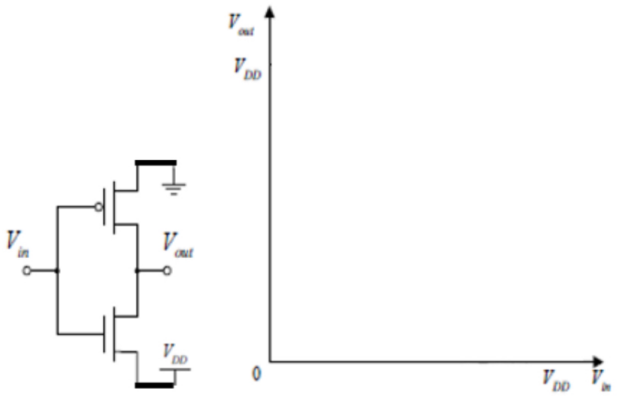
Extra:

4- In this problem, the circuits are implemented in 0.25um technology, and all the transistors have the minimum channel lengths .a. Consider the CMOS circuit from Fig. 2.a. If the NMOS transistor has channel width W_n and the PMOS transistor has channel width, W_p, label and sketch the voltage transfer characteristics from FIG. 2.b that correspond to following device sizes assuming Vtn and Vtp are threshold voltages for n and p devices :**(8 points)**

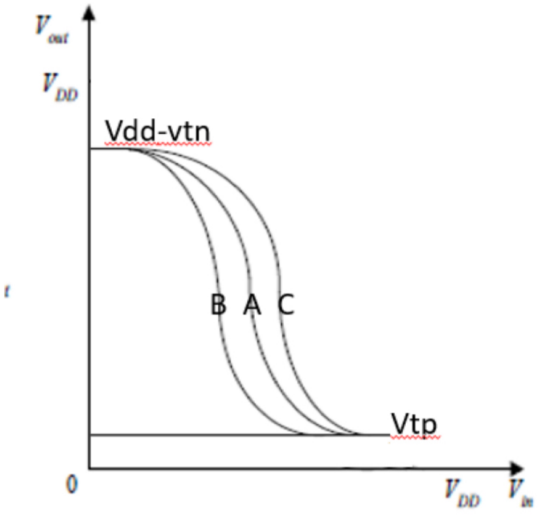
A: $W_n = 5\mu m$, $W_p = 5\mu m$

B: $W_n = 1\mu m$, $W_p = 5\mu m$

C: $W_n = 5\mu m$, $W_p = 1\mu m$



Sol.



3. Given three differences ways to design inverter. Match the right VTC curve to the right figure for each one. **[8 marks]**

Fig. A

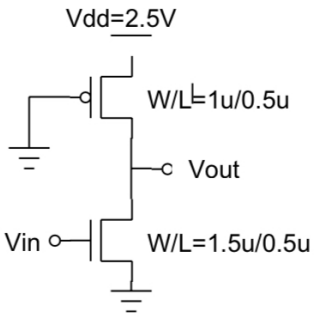


Fig. B

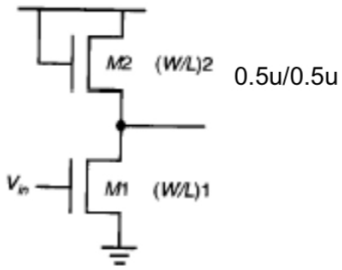
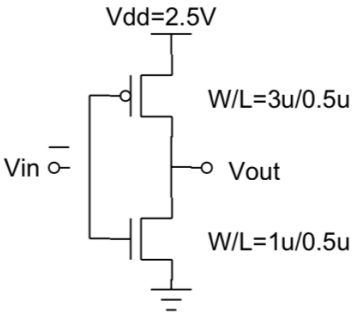
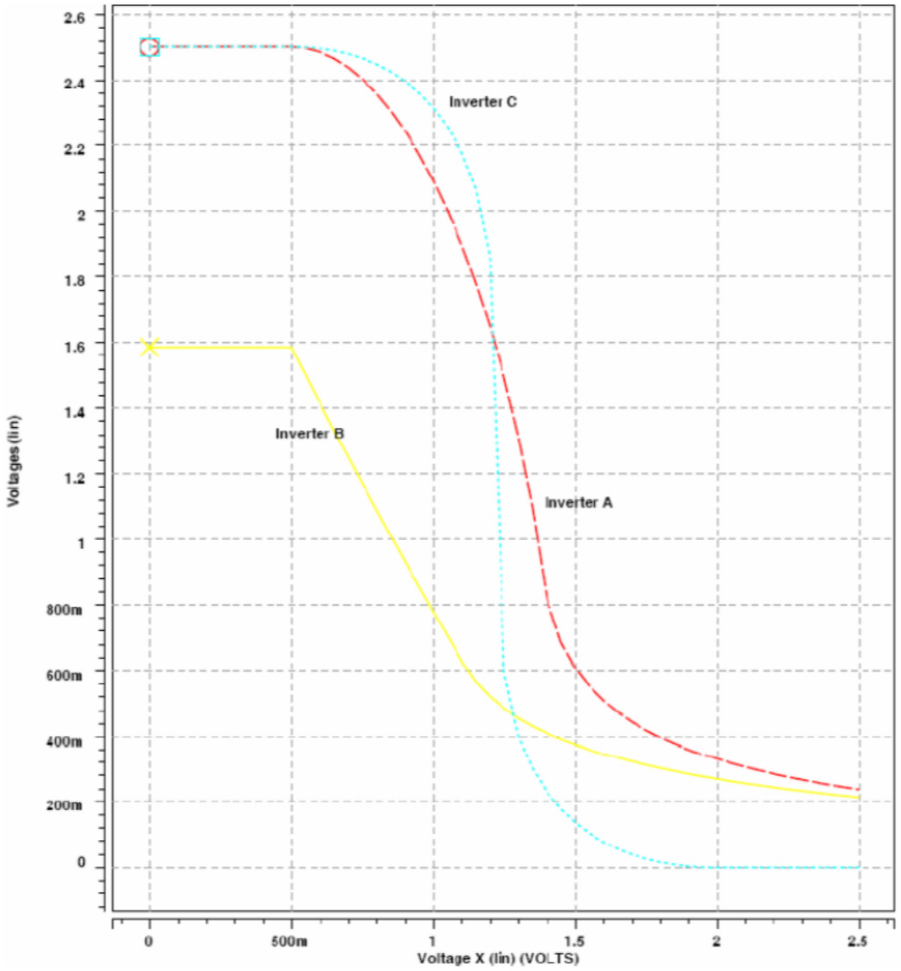


Fig. C



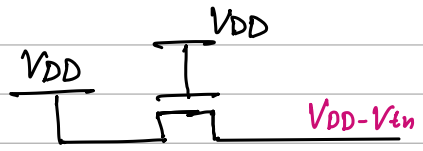
Sol.



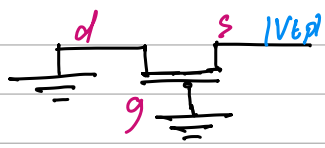
Pass Transistor DC Characteristics (Strong & Weak Signals)

* PMOS passes strong "1" (V_{DD}), and weak "0" = $|V_{tp}|$.
* NMOS passes strong "0" (GND), and weak "1" = $V_{DD} - V_{tn}$.

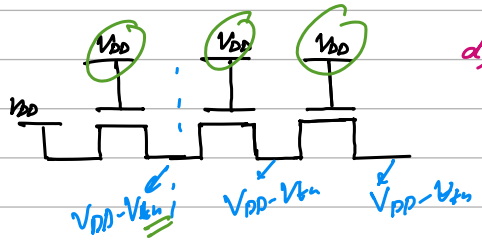
a)



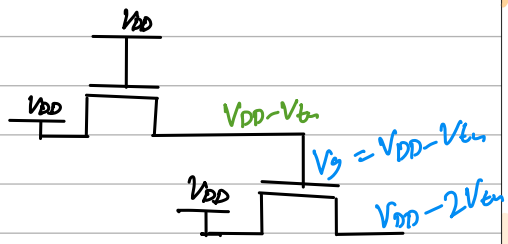
b)



c)



d)



* Note that the drain voltage is irrelevant to the output voltage.

Recall:

* NMOS ON:
  $V_{gs} > V_{tn} \Rightarrow V_g - V_s > V_{tn}$
  $V_s < V_g - V_{tn}$
* PMOS ON:
  $V_{gs} < V_{tp} \Rightarrow V_g - V_s < V_{tp}$
  $V_s > V_g - V_{tp}$ or $V_s > V_g + |V_{tp}|$

$V_s < V_g - V_{tn} < (V_{DD} - V_{tn}) - V_{tn} = V_{DD} - 2V_{tn}$

2.20 Give an expression for the output voltage for the pass transistor networks shown in Figure 2.35. Neglect the body effect.

$V_s > V_g + |V_{tp}| = 2|V_{tp}|$

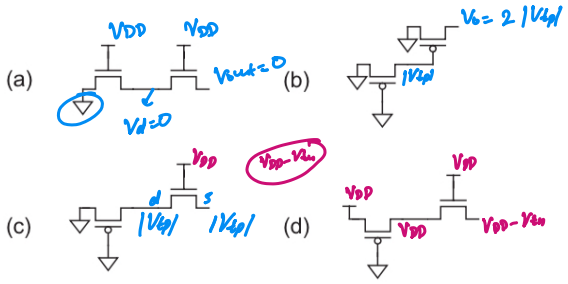


FIGURE 2.35 Pass transistor networks

2.21 Suppose $V_{DD} = 1.2$ V and $V_t = 0.4$ V. Determine V_{out} in Figure 2.36 for the following. Neglect the body effect.

a) $V_{in} = 0$ V $\Rightarrow V_o = 0$
b) $V_{in} = 0.6$ V $\Rightarrow V_o = 0.6$ V
c) $V_{in} = 0.9$ V $\Rightarrow V_o = 0.8$ V
d) $V_{in} = 1.2$ V. $\Rightarrow V_o = 0.8$ V

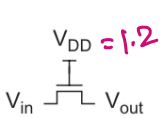


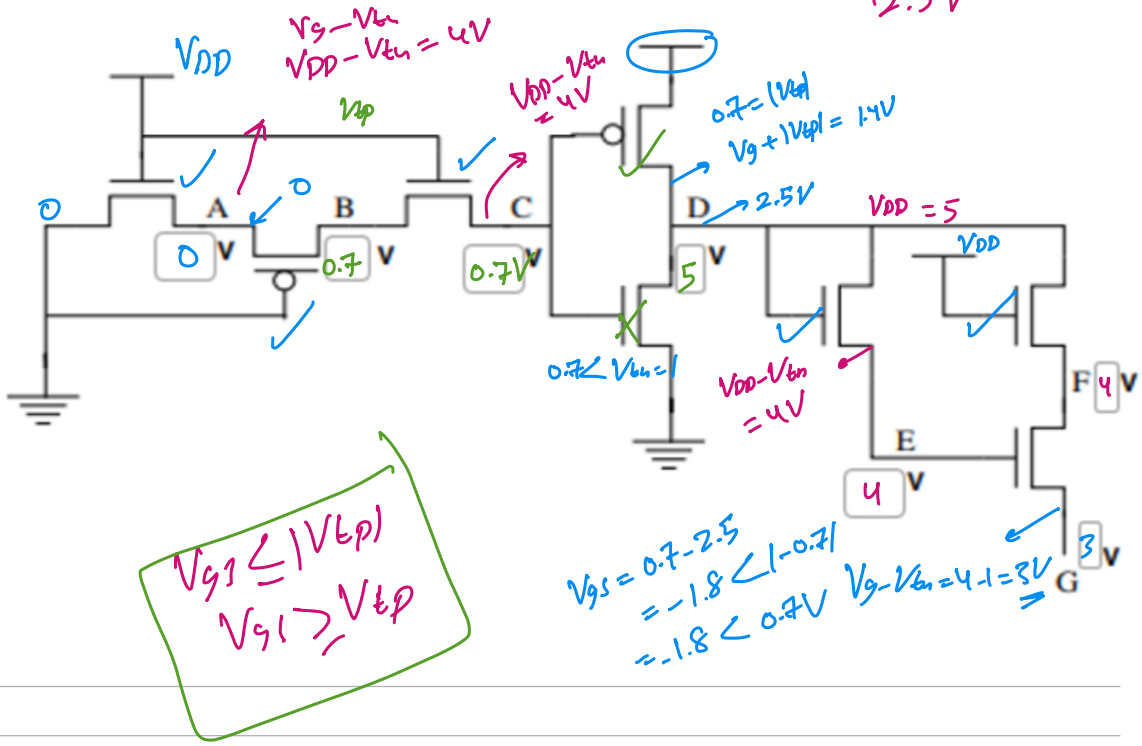
FIGURE 2.36
Single pass transistor

$V_g - V_t = 0.8$ V

Example:

$V_{DD}=5V,\ V_{tn}=1V,\ V_{tp}=-0.7V$

2.5V



$V_{g1} \le |V_{tp}|$

$V_{g1} \ge V_{tp}$

$V_{gs} = 0.7 - 2.5$

$= -1.8 < |-0.7|$

$= -1.8 < 0.7V$

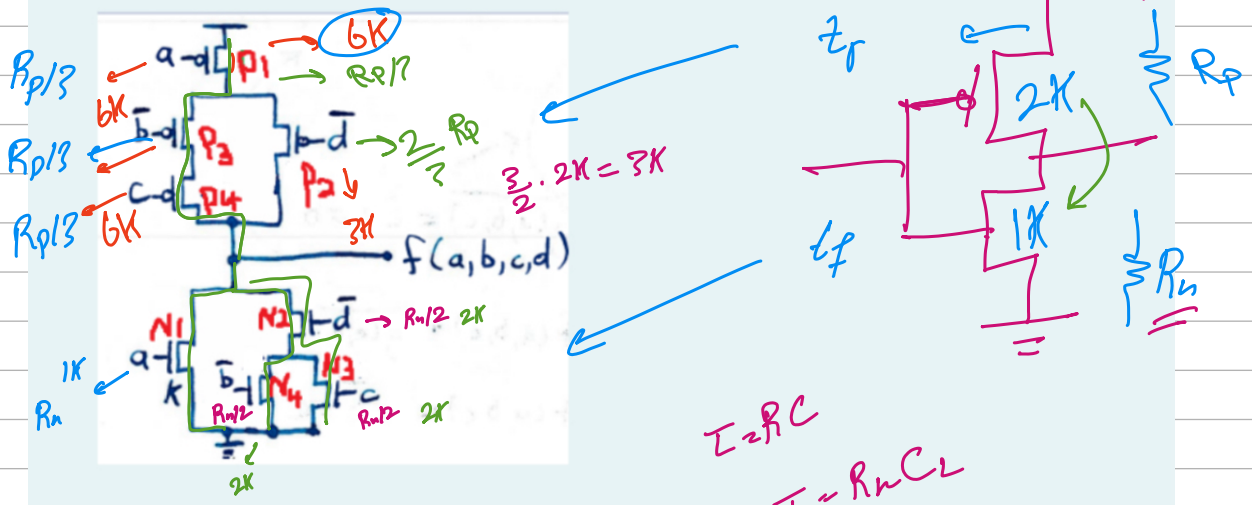
$V_g - V_{tn} = 4 - 1 = 3V$

Device Sizing:

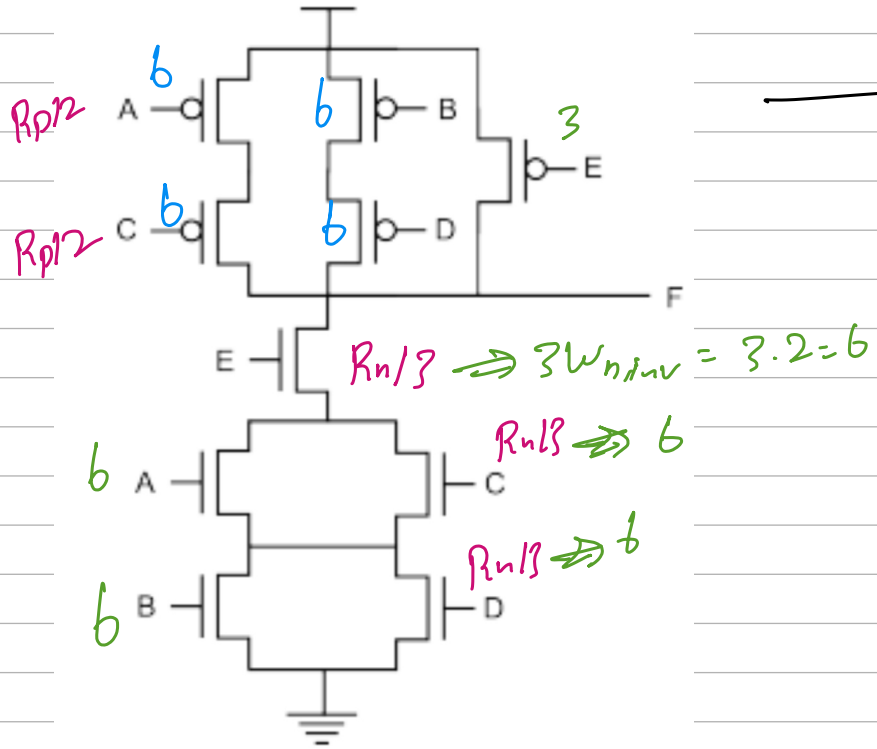
2λ

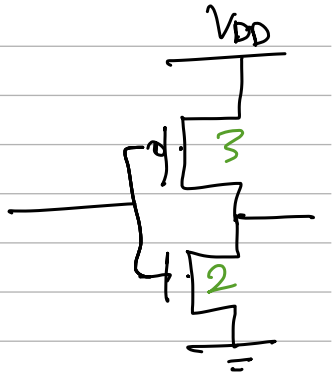
Example #1:

Match each transistor size based on an invertor of 1k for NMOS and 2k for PMOS



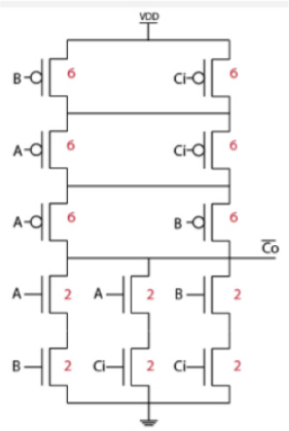
Example #2: Inverter: 3 (PMOS), 2 (NMOS).





Extra:

c. **What are the device sizes if it is going to match inverter with ratio of 2 for p and 1 for n (10 points)**



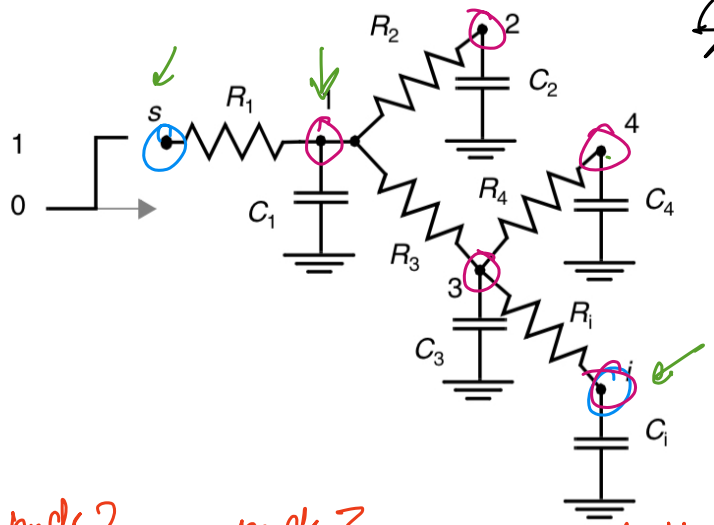
Elmore Delay

$$R_{ik} = \sum R_j \quad , \quad R_j \in [\text{path}(s \to i) \cap \text{path}(s \to k)] \quad \text{(path resistance)}$$

$$T_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

Example: compute the Elmore delay for node i.

$$\sum_{1}^{i} \text{path resistance} \times C_i$$



$s \to i$: R_1, R_2, R_i

$s \to 1$: R_1

node 1 node 2 node 3 node 4 node 5 (i)

$$T_D = R_1 C_1 + R_1 C_2 + (R_1 + R_3) C_3 + (R_1 + R_3) C_4 + (R_1 + R_3 + R_i) C_i$$

Example: compute the Elmore delay for node N.

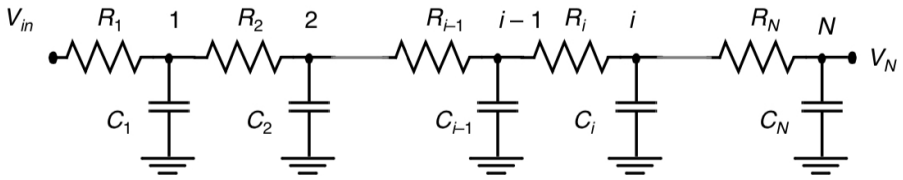
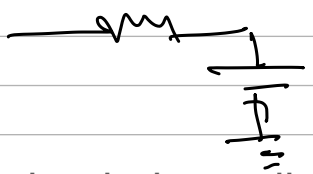


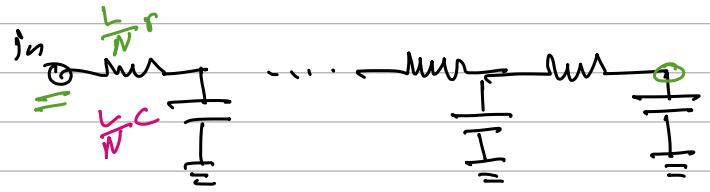
Figure 4.13 *RC* chain.

$$\tau_{DN} = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j = \sum_{i=1}^{N} C_i R_{ii}$$

$$T_D = R_1 C_1 + (R_1 + R_2) C_2 + \cdots + (R_1 + \cdots R_n) C_N$$



Example: Find the delay of a wire of length L, resistance r, capacitance c, partitioned into N identical segments.



$$\tau_D = \frac{L}{N}\frac{L}{N}rc + \frac{L}{N}\cdot\frac{L}{N}(r+r)c + \cdots + \frac{L}{N}\frac{L}{N}(Nr)c$$

$$= \left(\frac{L}{N}\right)^2 (1+2+\cdots N)rc = \left(\frac{L}{N}\right)^2 \frac{N(N+1)}{2}rc = \frac{L^2}{N}\frac{(N+1)}{2}rc$$

$$\tau_D = \frac{rcL^2}{2}\cdot\frac{N+1}{N}\Big|_{N\to\infty} = \frac{rcL^2}{2}$$

$$\tau_D = \frac{rcL^2}{2}$$

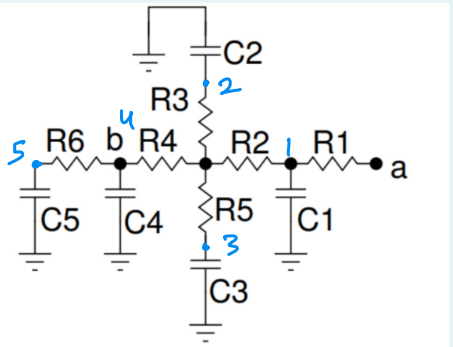
* If the length of the wire is doubled, its delay will be quadrupled.

Exercises:

1

Question 10
Not answered
Marked out of 1.00
Flag question

Determine the Elmore delay from Node a to Node b in the following circuit



- A. delay = (R1 +R2+R3+R4)(C4 +C5)
- B. delay = R1(C1 +C2 +C3) +R2(C2 +C3 +C4) +R4(C4 +C5)
- C. delay = R1(C1 +C2 +C3 +C4) +R2(C2 +C3 +C4) +R4(C4 +C5)
- D. delay = R1(C1 +C2 +C3 +C4 +C5) +R2(C2 +C3 +C4 +C5) +R4(C4 +C5)

The correct answer is: delay = R1(C1 +C2 +C3 +C4 +C5) +R2(C2 +C3 +C4 +C5) +R4(C4 +C5)

C_2, C_3 in parallel at node 2 $\Rightarrow$ add them.

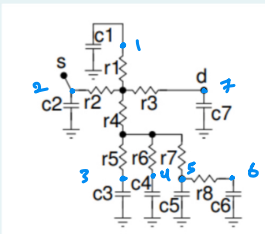
node 1 node 2 node 3 node 4 node 5

$$delay = R_1C_1 + (R_1+R_2)C_2 + (R_1+R_2)C_3 + (R_1+R_2+R_4)C_4 + (R_1+R_2+R_4)C_5$$
$$= R_1(C_1+C_2+C_3+C_4+C_5) + R_2(C_2+C_3+C_4+C_5) + R_4(C_4+C_5)$$

2

Question 11
Not answered
Marked out of 1.00
Flag question

Derive an expression for the time constant when driving node **d**. **Vs** changes from 0 V to 2.5 V at time zero. (delay from s to d)



- A. τd = r2 (c1 + c3 + c4 + c5 + c6) + (r2 + r3) c7.
- B. τd = r2 (c2 + r3+ c4 + c5 + c6) c7.
- C. τd = r2 (c1 + c3) + (r2 + r3+ c4 + c5 + c6) c7.
- D. τd = r2 (c1 + c3 + c4) + (r2 + r3+ c5 + c6) c7.

The correct answer is: τd = r2 (c1 + c3 + c4 + c5 + c6) + (r2 + r3) c7.

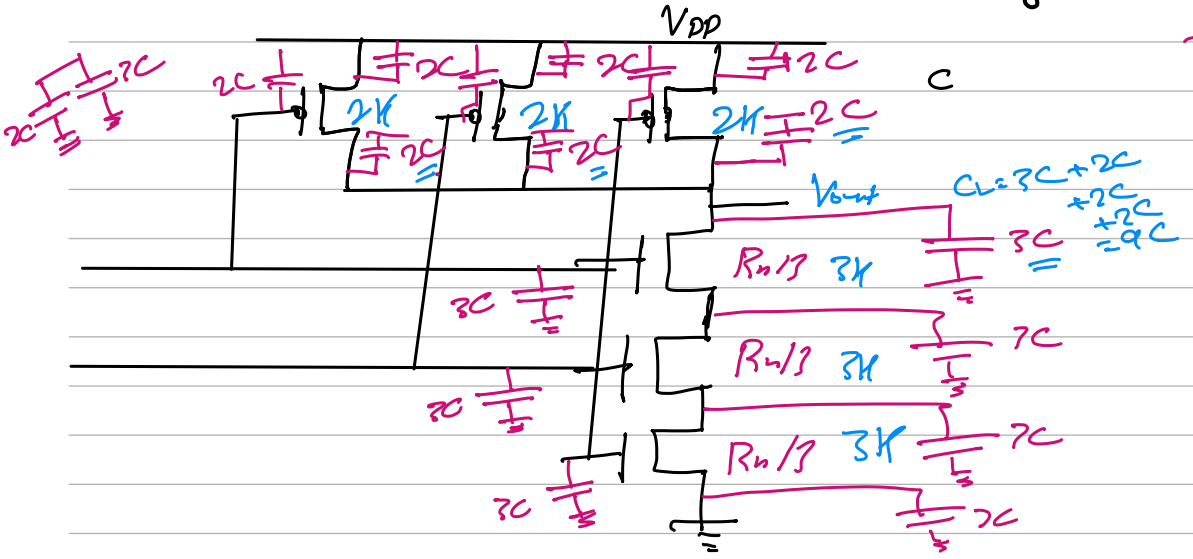
node 1 node 3 node 4 node 5 node 6 node 7

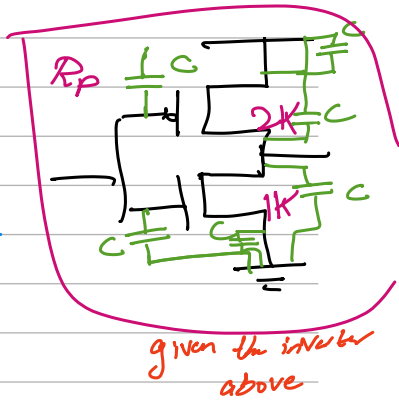
$$delay = r_2C_1 + r_2C_3 + r_2C_4 + r_2C_5 + r_2C_6 + (r_2+r_3)C_7$$
$$= r_2(C_1+C_3+C_4+C_5+C_6) + (r_2+r_3)C_7$$

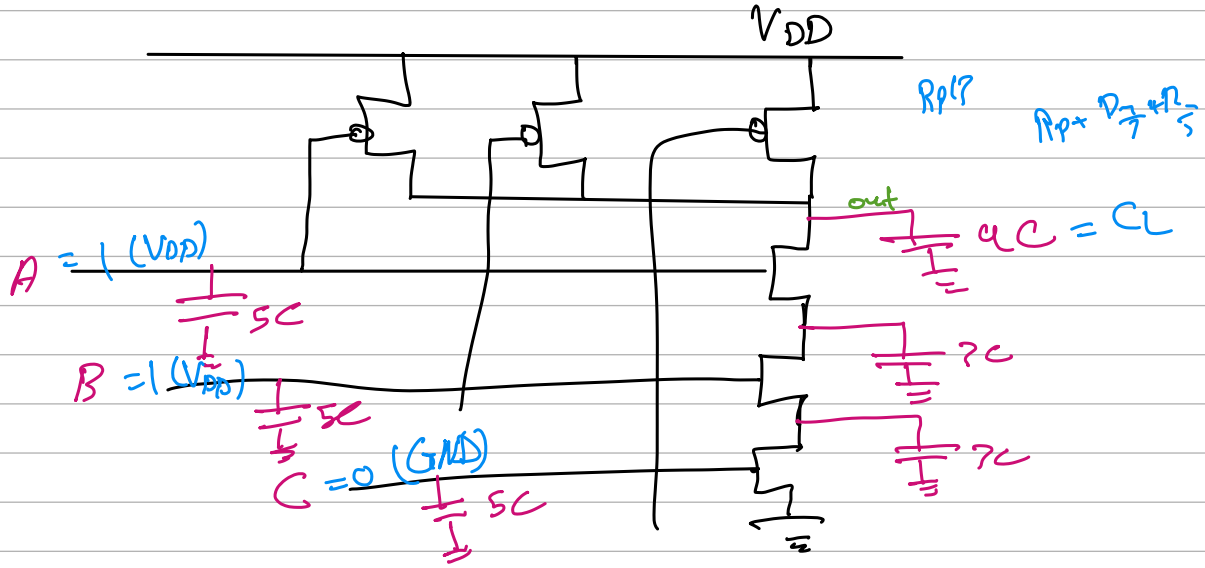
* What happened to node 2 ? $[path(s\to 2) = \emptyset \cap path(s\to d) = r_2, r_3] = \emptyset$
The path resistance from a node to itself is zero, since there is no intersection.

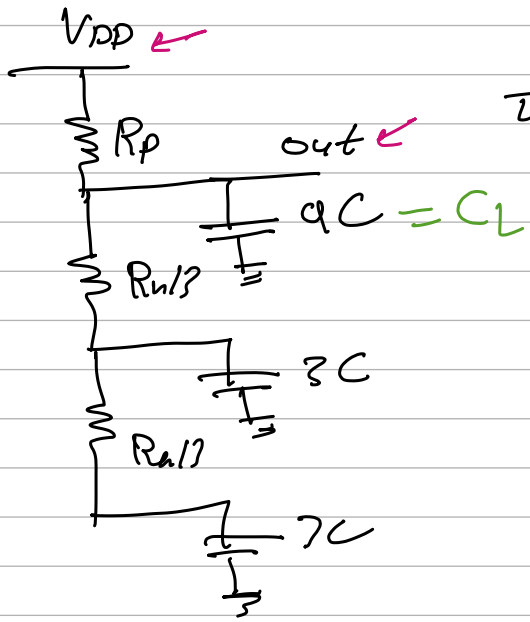
Propagation Delay

Example: Sketch a 3-input NAND gate with transistor widths to achieve effective fall and rise time equal to that of an inverter. Annotate gate & diffusion capacitances.

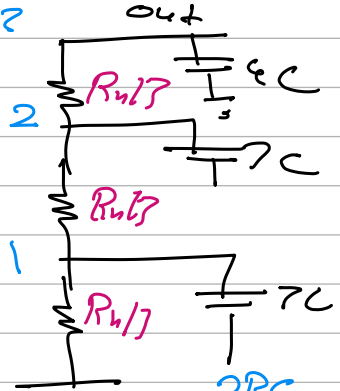






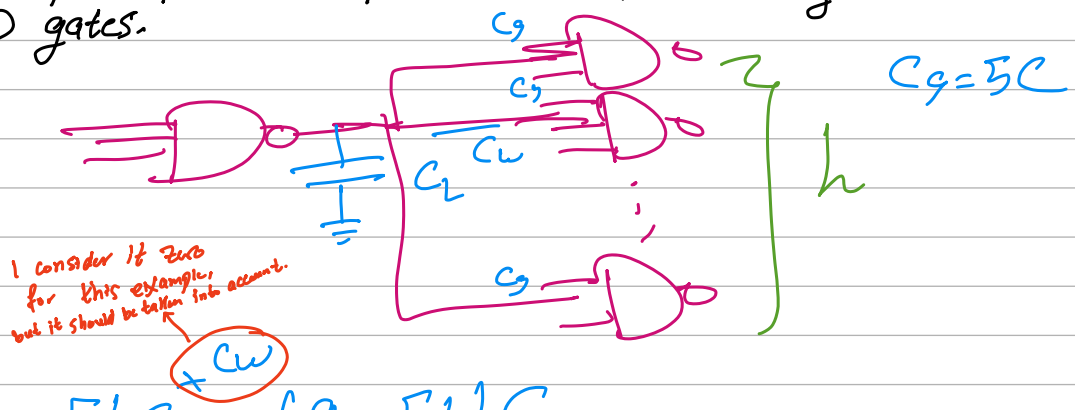


$$t_p = R_p(9C) + R_p(3C) + R_p(7C)$$
$$= 15CR_p$$

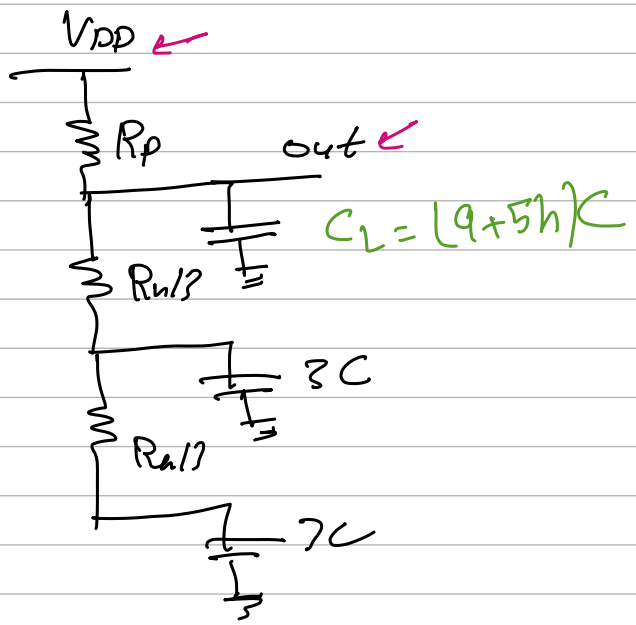


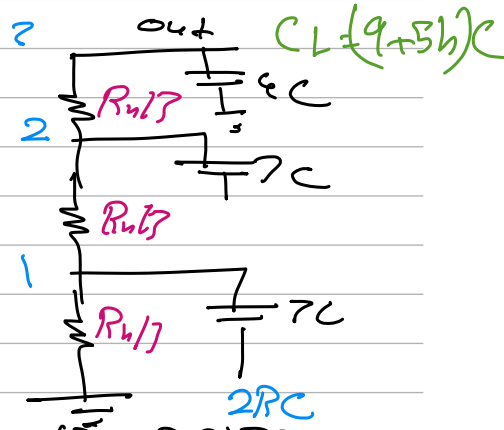
$$t_N = R_n/3(7C) + (R_n/7 + R_n/7)PC + (R_n/7 + R_n/7 + R_n/7)9C$$
$$= 12R_nC$$

Example: Estimate t_{pdf}, t_{pdr} for the previous 3-input NAND gate loaded with h identical NAND gates.



$$C_L = 9C + 5hC = (9+5h)C$$





$$\tau_N = R_n/3(7C) + (R/7 + R/7)3C + (R/7 + R/7 + R/7)9C = 12RC$$

$9RC$

$$t_r = R_p(9+5h)C + R_p(3C) + R_p(3C) = (15+5h)R_pC$$

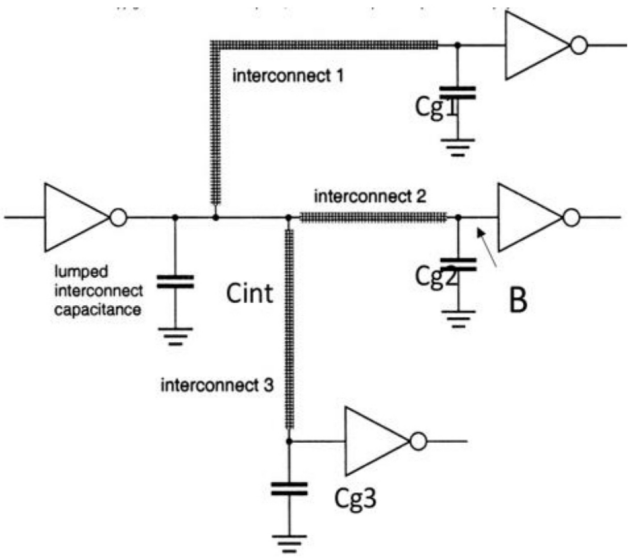
$$t_f = \frac{R_n}{3}(3C) + \left(\frac{R_n}{7} + \frac{R_n}{7}\right)(3C) + \left(\frac{R_n}{7} + \frac{R_n}{7} + \frac{R_n}{7}\right)(9+5h)C$$

$$= R_nC + 2R_nC + (9+5h)R_nC = (12+5h)R_nC$$

Similar Example:

B) Compute the worst-case rising and falling RC time constants at point B of the circuit below using the Elmore delay method. Assume all transistors **are unit sized** and wire **capacitance is lumped**. ***(7 pts)***

Assume **Rchn** = 2000 ohms. **Rchp** = 8604 ohms, Cg(n+p) = 20 ff, Cd(n+p) = 20ff, and Cint = 10 ff. Rint for interconnect1 is 10 ohms, interconnect2 is 5 ohms, and interconnect3 is 7 ohms.
Hint: Note that interconnect **capacitance is lumped at the beginning**, so we don't need to consider it separately for the 3 wires



Recall that channel resistance is inversely proportional to beta. So:

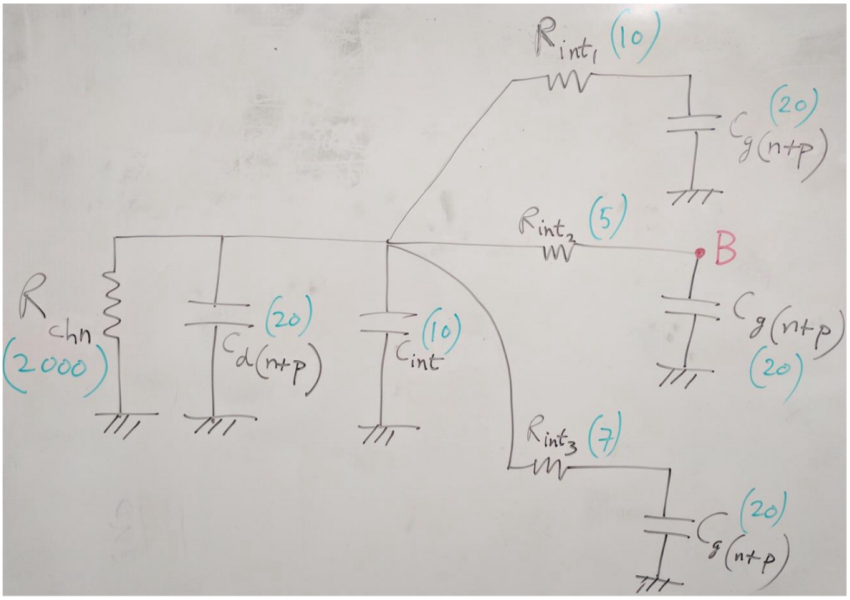
$$\frac{R_{chp}}{R_{chn}} = \frac{\beta_n}{\beta_p}$$

Note that interconnect **capacitance is lumped at the beginning**, so we don't need to consider it separately for the 3 wires.
Following is the circuit for falling delay at B:

Falling Elmore delay at B = $2000 \times 20 + 10 + 20 + 20 + 20 + 5 \times 20 = \mathbf{0.1801\ ns}$

For rising delay at B, the circuit is the same except that Rchn is replaced with Rchp and the leftmost Gnd
symbol is replaced with Vdd.

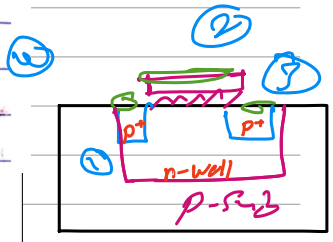
Rising Elmore delay at B = $8604 \times 20 + 10 + 20 + 20 + 20 + 5 \times 20 = \mathbf{0.77446\ ns}$



CMOS Manufacturing Process

Simplified Process Sequence:

- Define active regions
- Etch & fill trenches
- Implant well regions
- Deposit & pattern polysilicon layer
- Implant source and drain regions and substrate contacts
- Create contact & via windows, Deposit and pattern metal layer(s)



Photolithography

* Technique to selectively mask out a certain area on the chip to apply a certain processing step: oxidation/etching/metal & polysilicon deposition/ion implantation.

different operations in a photolithographic process

① oxidation (SiO2) → ② photoresist coating (photoresist) → ③ stepper exposure (mask)

④ spin, rinse, dry ← ⑤ acid etch ← ⑥ photoresist development (stepper exposure, photoresist)

⑦ Various process steps → ⑧ photoresist removal (ashing)

* ion implantation of drain/source/well
* metal deposition and etching

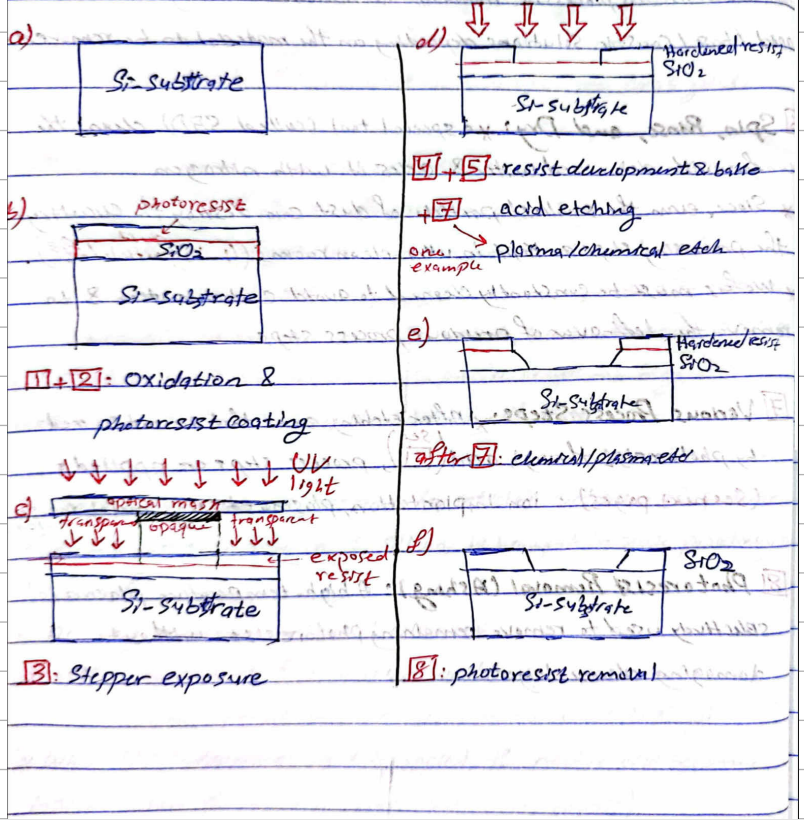
Photoresist Types:

① Negative Photoresist: originally soluble, but insoluble after exposure to UV light

② Positive Photoresist originally insoluble, but soluble after exposure to UV light

* Negative photoresist is assumed in the example.

Example: Process steps for patterning SiO_2 (using photolithography)

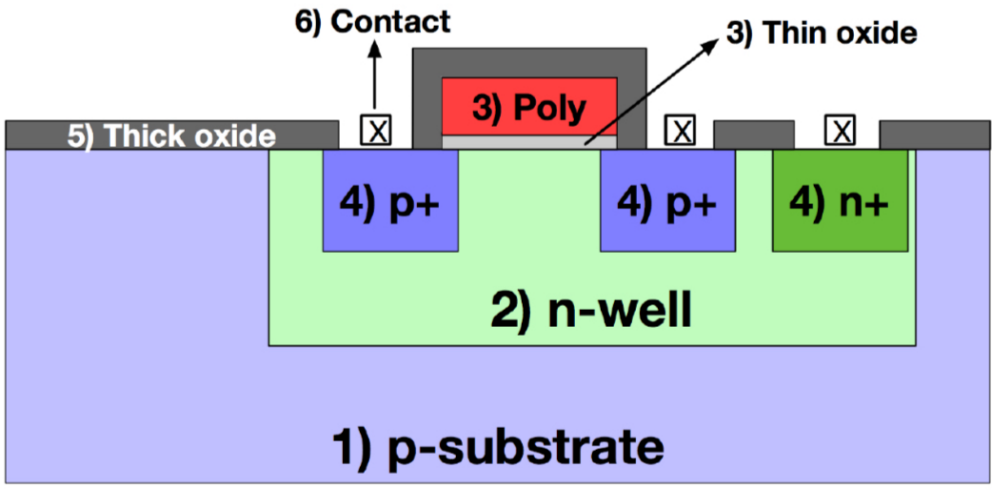


Q) List the steps required for creating a PMOS transistor. Draw a cross-section of the PMOS transistor, labelling each layer/feature in the order fabricated.

C. List the steps required for creating a PMOS transistor, and draw a cross-section of the PMOS transistor, labeling each layer/feature in the order fabricated. **(5 pts)**

The steps below assume that a p-type substrate and positive photoresist is used.

1. Expose the substrate to oxygen (and hydrogen) at very high temperatures to form silicon dioxide
(SiO_2) layer. This is thick oxide.
2. Deposit photoresist.
3. Cover the photoresist with a mask which exposes those areas where n-well is to be created.
4. Expose to UV light.
5. Remove the exposed photoresist by dissolving.
6. Etch the surface to remove the portions of SiO_2 not covered by photoresist.
7. Strip off remaining photoresist.
8. Use *n* ion implantation to form n-wells in the areas without SiO_2.
9. Cover the whole surface with thin oxide and polysilicon.
10. Selectively remove thin oxide and poly from everywhere except for transistor gates.
11. Use *p+* ion implantation to form sources and drains of PMOS transistors.
12. Use *n+* ion implantation to form ntaps.
13. Cover the whole surface with thick oxide.
14. Selectively remove thick oxide from the source, drain and body (n-tap). This forms contact cuts.



Question **4**

Complete

Mark 0.20 out of 1.00

Flag question

List the following interconnect fabrication steps in chronological order:

• Etch metal. • Expose photoresist using mask. • Remove all photoresist. • Deposit photoresist. • Deposit metal everywhere.

5) Deposit photoresist.

3) Remove all photoresist.

1) • Expose photoresist using mask.

4) Etch metal

2) Deposit metal everywhere

The correct answer is: 5) → Remove all photoresist., 3) → • Expose photoresist using mask., 1) → Deposit metal everywhere, 4) → Etch metal, 2) → Deposit photoresist.