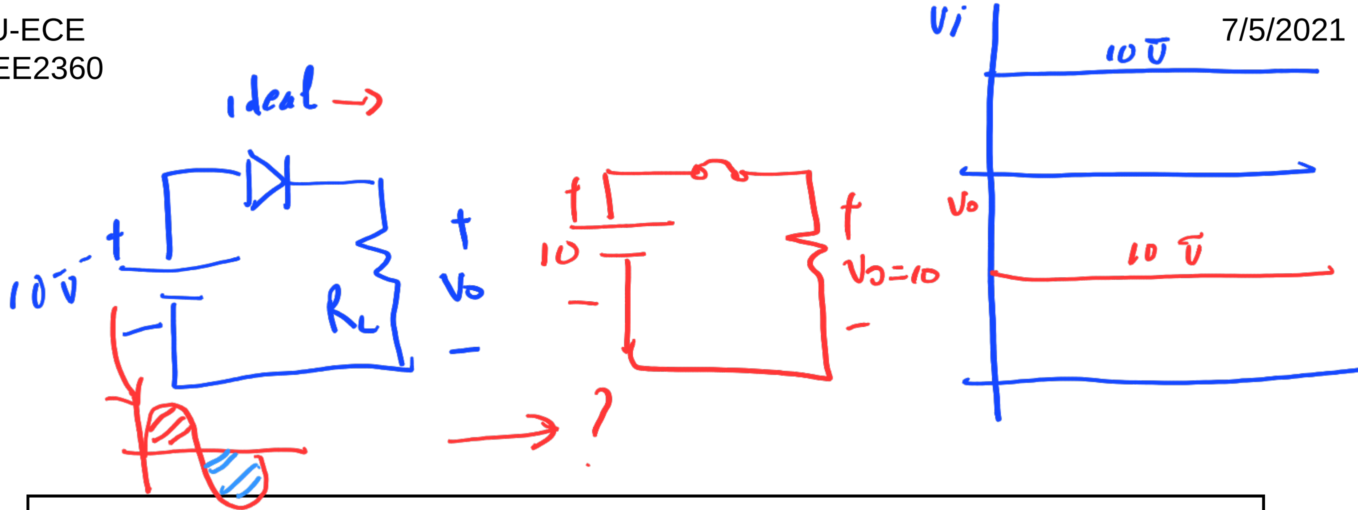
L4 - Part 2
13/7/2021

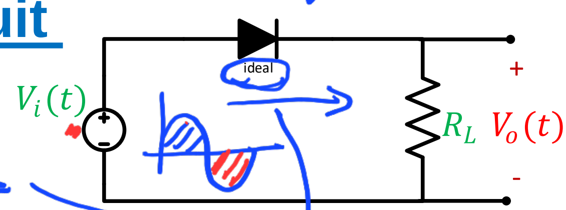
ENEE236
Analog Electronics

T3:
Diode Applications



Diode large – signal application

1) Diode clipper circuit



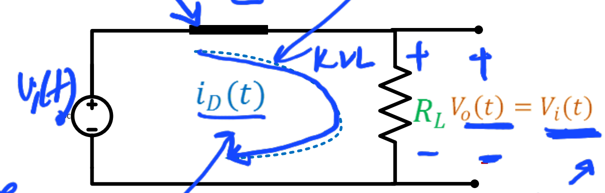
a) assume the diode is on

replace it with short circuit

$i_D(t) > 0$

$i_D(t) = \frac{V_i(t)}{R_L} > 0$

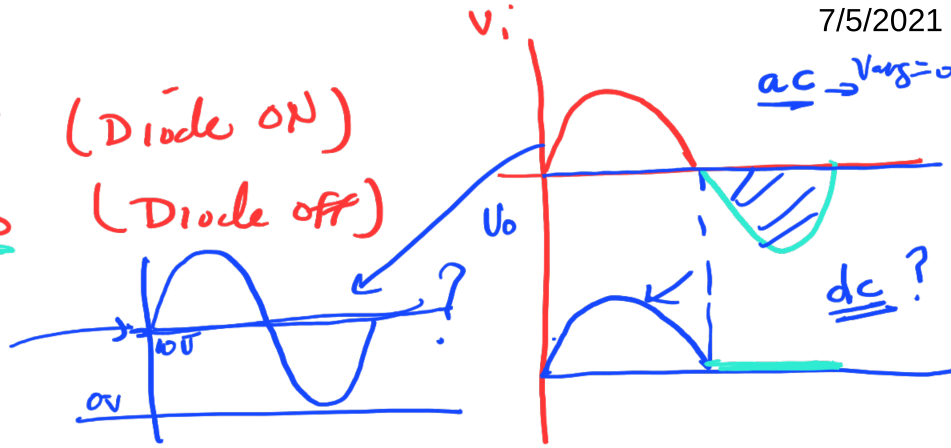
$\therefore\ V_i(t) > 0$



$\therefore$ when $V_i(t) > 0$, the diode is on and $V_O(t) = V_i(t)$

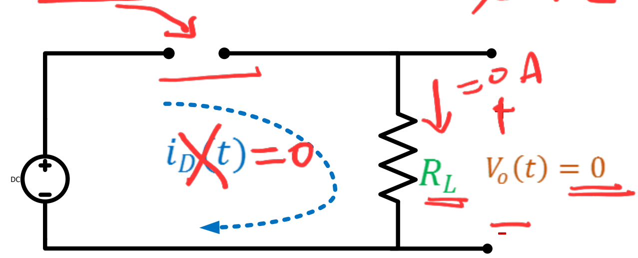
$V_i(t) > 0 \rightarrow V_o = V_i$ (Diode ON)

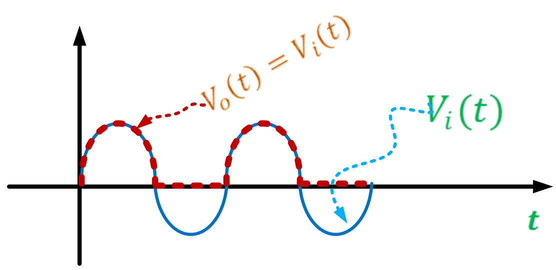
$V_i(t) < 0 \rightarrow V_o = 0$ (Diode off)



∴ when $V_i(t) < 0$, the diode is off and $V_O(t) = 0$. $= i_D \cdot R_L$

$V_O(t) = 0$.



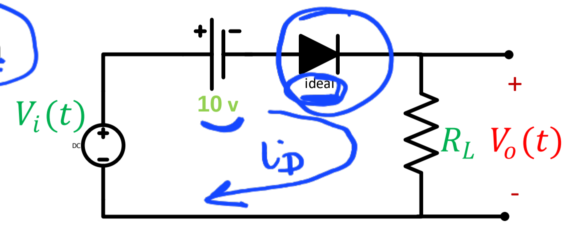


∴ the clipper circuit used to eliminate portion of the input signal .

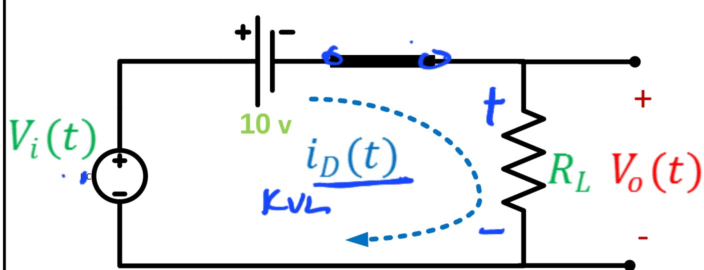
Example

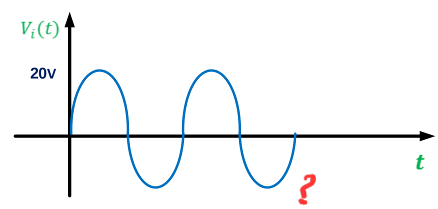
a) assume that the diode is on

➔ replace it with short circuit



$i_D > 0$





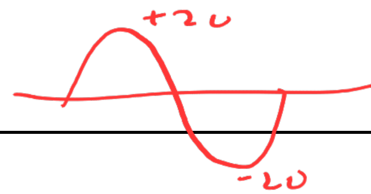
$V_i(t) - 10 - i_D(t) \cdot R_L = 0$

$i_D(t) \cdot R_L = V_o(t)$

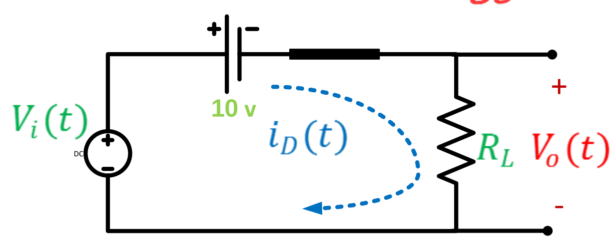
$$i_D(t) = \frac{V_i(t) - 10}{R_L} > 0$$

$V_i - 10 > 0$

$V_i > 10$ → Diode ON → $V_o = V_i(t) - 10$



$$i_D(t) = \frac{V_i(t) - 10}{R_L} > 0$$



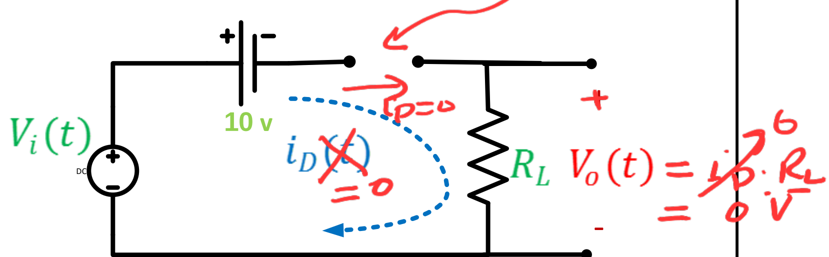
$$\therefore\ V_i(t) - 10 > 0$$

$$\therefore\ V_i(t) > 10$$

$\therefore$ when $V_i(t) > 10$ V , the diode is on and $V_O(t) = V_i - 10$

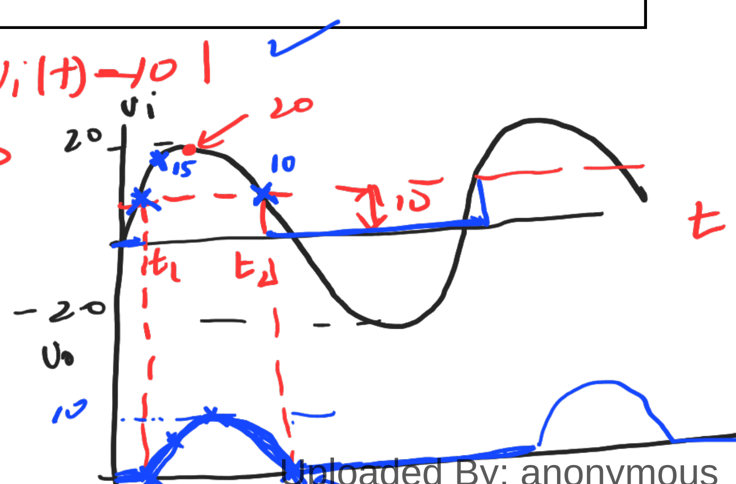
and also we can prove that when $V_i(t) < 10\ V$, the diode is off

$$\therefore\ V_O(t) = 0$$

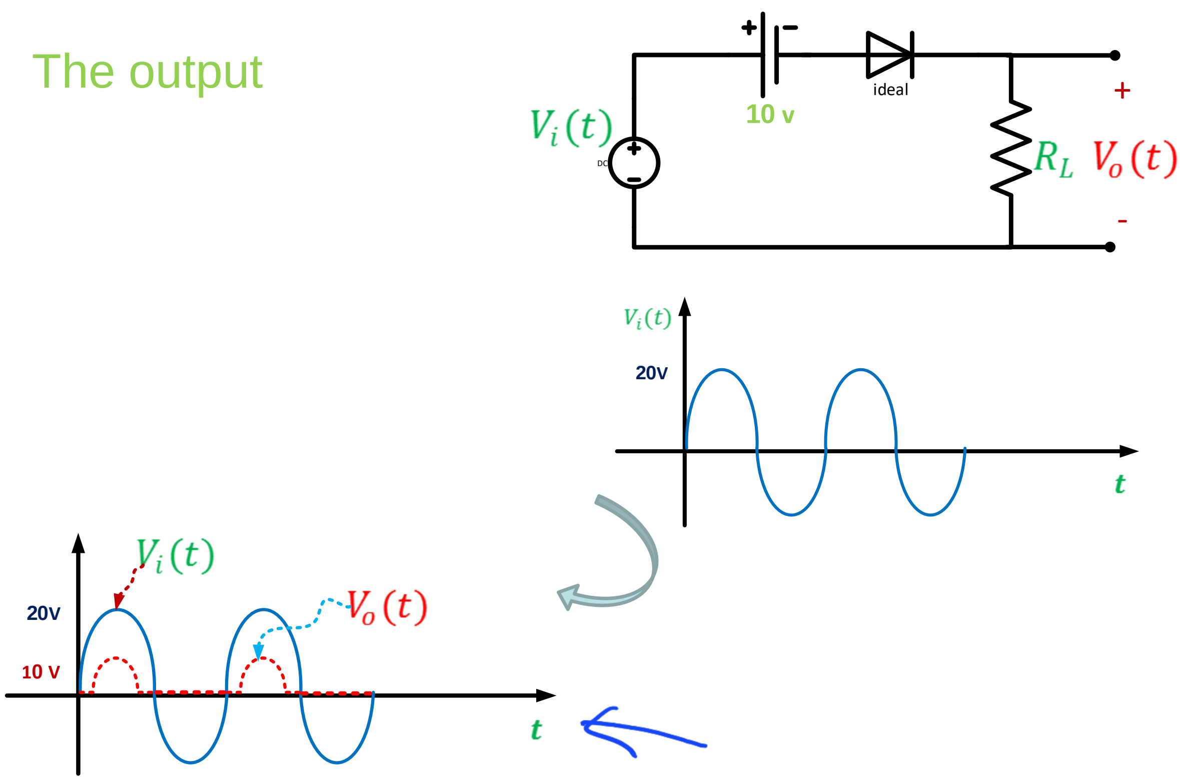


$V_i(t) > 10$ Diode ON → $V_o = V_i(t) - 10$

$V_i(t) < 10$ off → $V_o = 0$



The output



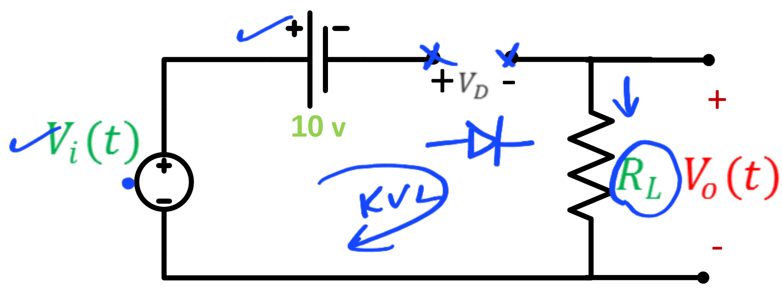
Second Method

assume that the diode is off ,replace it with open circuit

$V_D(t) < 0$

$V_D(t) = -10 + V_i$

$V_i(t) < 10$ V



$V_i - 10 - V_D = 0$

$V_D = V_i - 10$

$\therefore$ when $V_i(t) < 10$ V , the diode is off and $V_O(t) = 0$

≤ 10

$V_i > 10$, " ON

$V_o = V_i - 10$ ⟸ see previous solution

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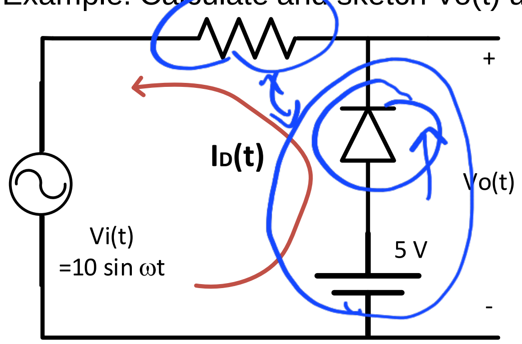
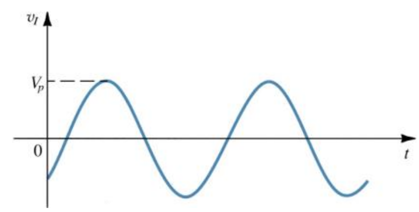
Limiters (=Clipping circuits) (1)

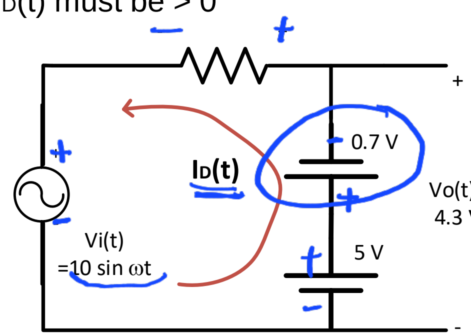
Example: Calculate and sketch Vo(t) using simplified diode model





$5 = 0.7 + i_D R + V_i(t)$

1) Assume diode is ON, so we replace it by 0.7 V and $i_D(t)$ must be > 0

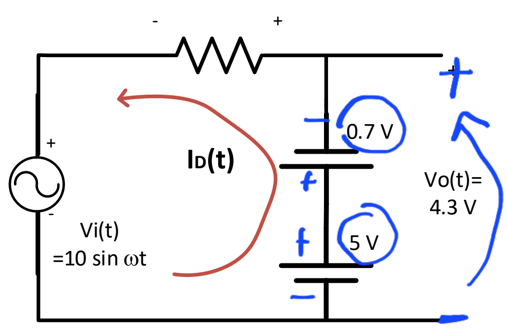


$$5V - 0.7V - i_D(t).R - Vi(t) = 0$$

$$i_D(t).R = 4.3V - Vi(t)$$

$$i_D(t) = \frac{4.3V - Vi(t)}{R} > 0$$

Limiters (=Clipping circuits) (2)



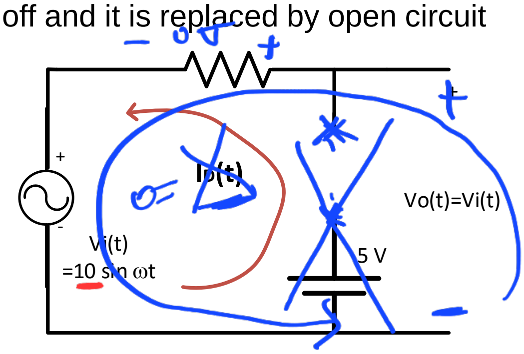
$\therefore \quad 4.3V - Vi(t) > 0$

$\Rightarrow Vi(t) < 4.3V$

when Vi(t) < 4.3 V diode is ON ar

Vo(t) = 4.3V

2) Otherwise, When Vi(t) is > 4.3 V, Diode will be off and it is replaced by open circuit

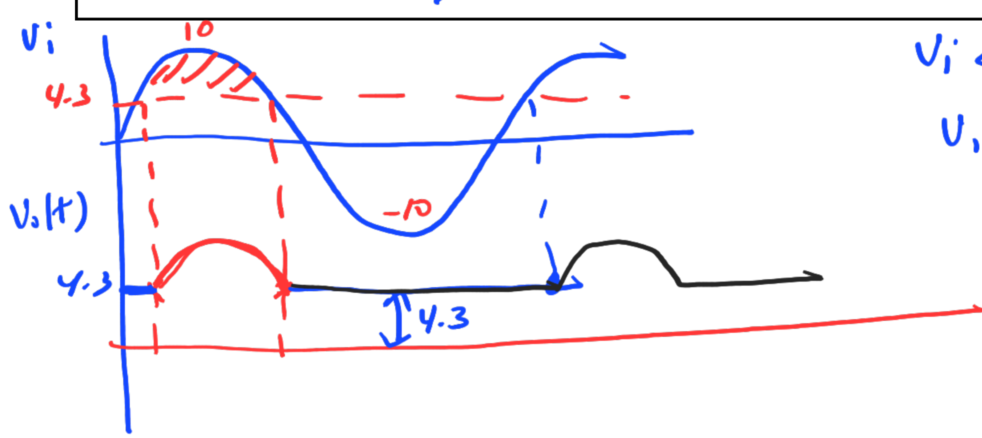


$\Rightarrow Vi(t) > 4.3V$

$Vo(t) = Vi(t)$

$V_o(t) - V_i(t) = 0$

$V_o(t) = V_i(t)$



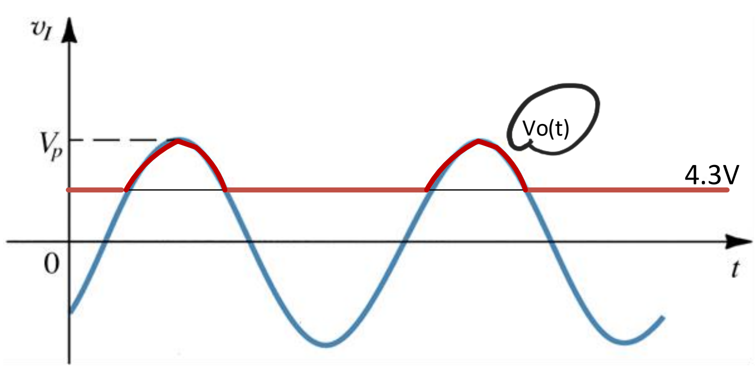
$V_i < 4.3 \rightarrow V_o = 4.3$

$V_i > 4.3 \rightarrow V_o = V_i$

Limiters (=Clipping circuits) (3)

when Vi(t) < 4.3V , diode is ON & Vo(t) = 4.3V
when Vi(t) > 4.3V , diode is off & Vo(t) = Vi(t)

Summary → sketch



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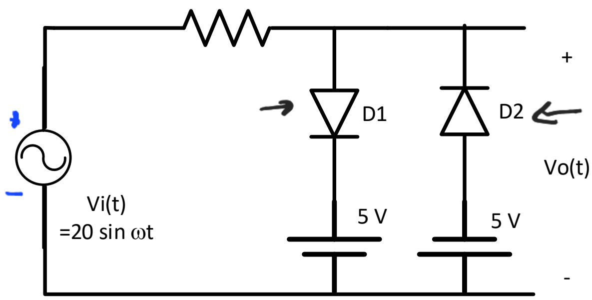
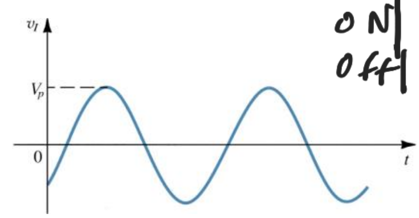
Circuit Containing Two diodes

Example: Calculate and sketch Vo(t) using ideal diode model





D1	D2
ON	OFF
OFF	ON
ON	ON
OFF	OFF

Since the circuit contains two diodes, each of them can be either On or Off,
➔ then there is 4 possible combinations for the states of D1 and D2

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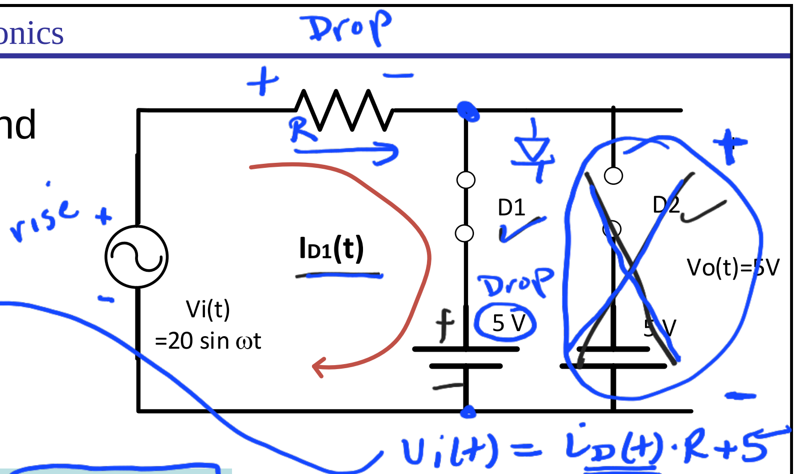
1) Assume D1 is ON and D2 is OFF

$i_{D1}(t) > 0$



$$i_{D1}(t) = \frac{Vi(t) - 5}{R} > 0$$

when $Vi(t) > 5\,V$, $Vo(t) = 5V$

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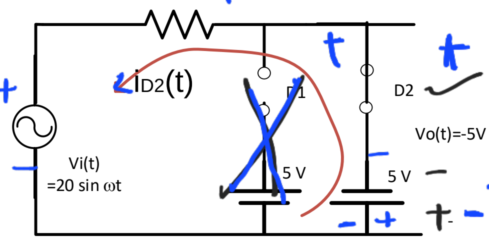
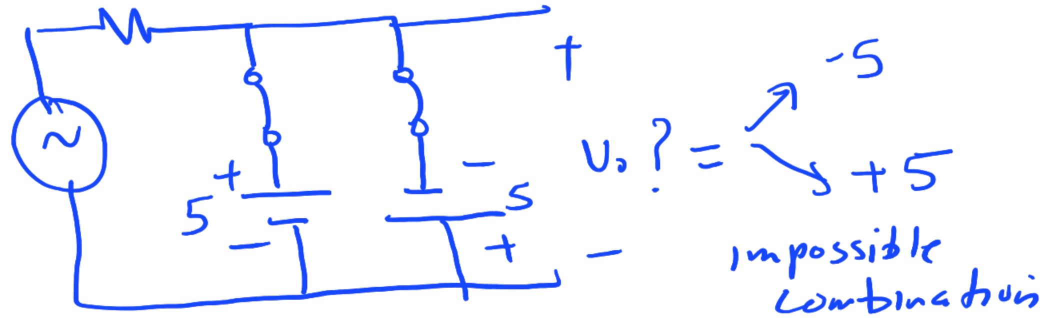
2) Assume D2 is ON and D1 is OFF

$i_{D2}(t) > 0$



$$i_{D2}(t) = \frac{-Vi(t) - 5}{R} > 0$$

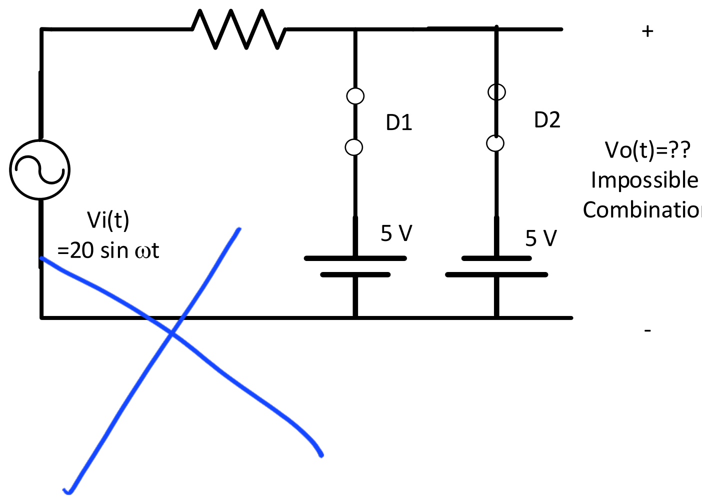
when $Vi(t) < -5\,V$, $Vo(t) = -5V$



3) Assume D1 & D2 are ON

Vo=+5V ??
Vo=-5V ??

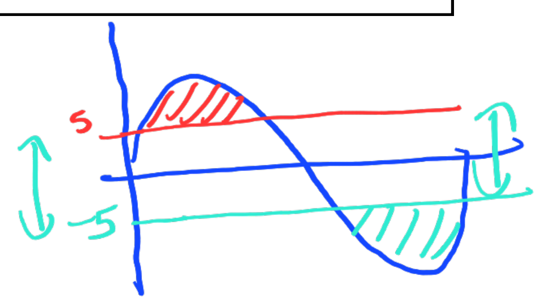
This is invalid configuration and impossible to occur

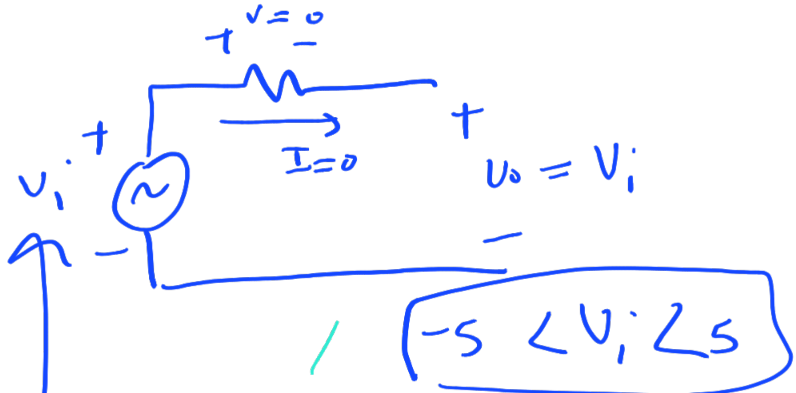


$V_i > 5 \rightarrow V_o = 5$

$V_i < -5 \rightarrow V_o = -5$

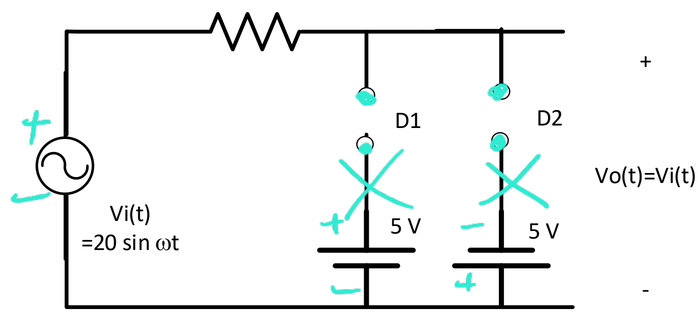
? $-5 < V_i < 5$?





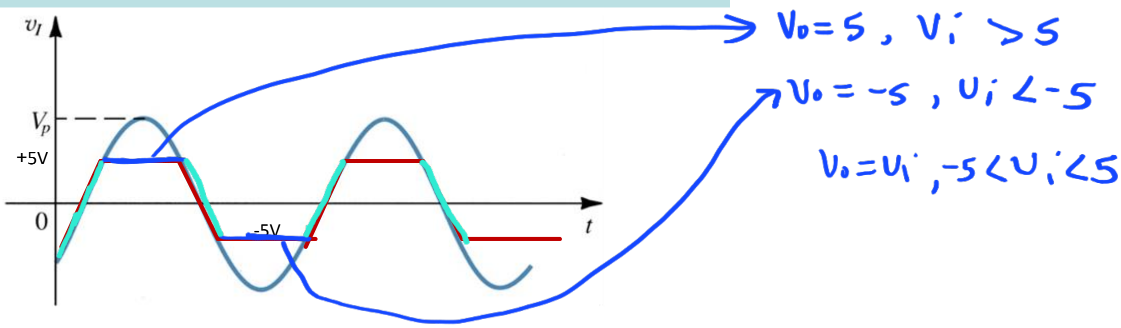
4) Assume D1 & D2 are both OFF

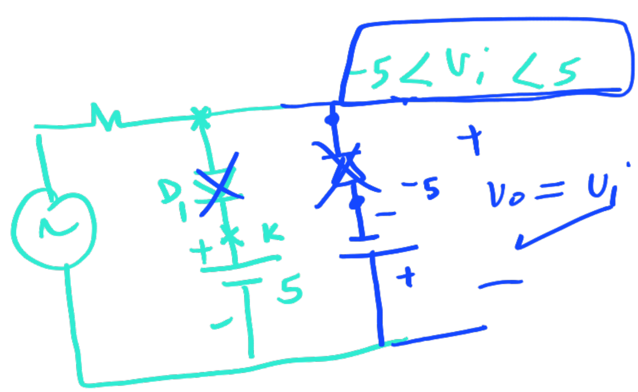
Vo(t) = Vi(t)



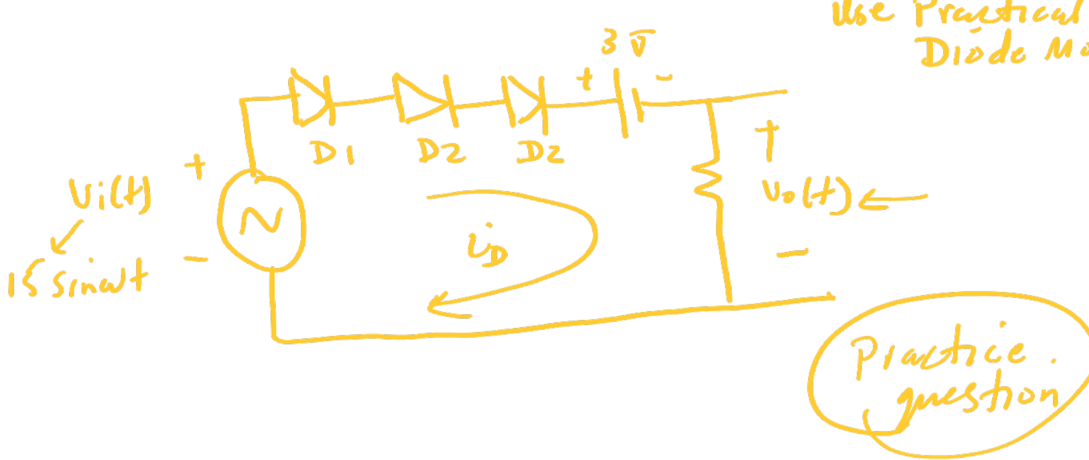
This occures for the remaining part of the input voltage waveform:

$-5V < Vi(t) < 5V$



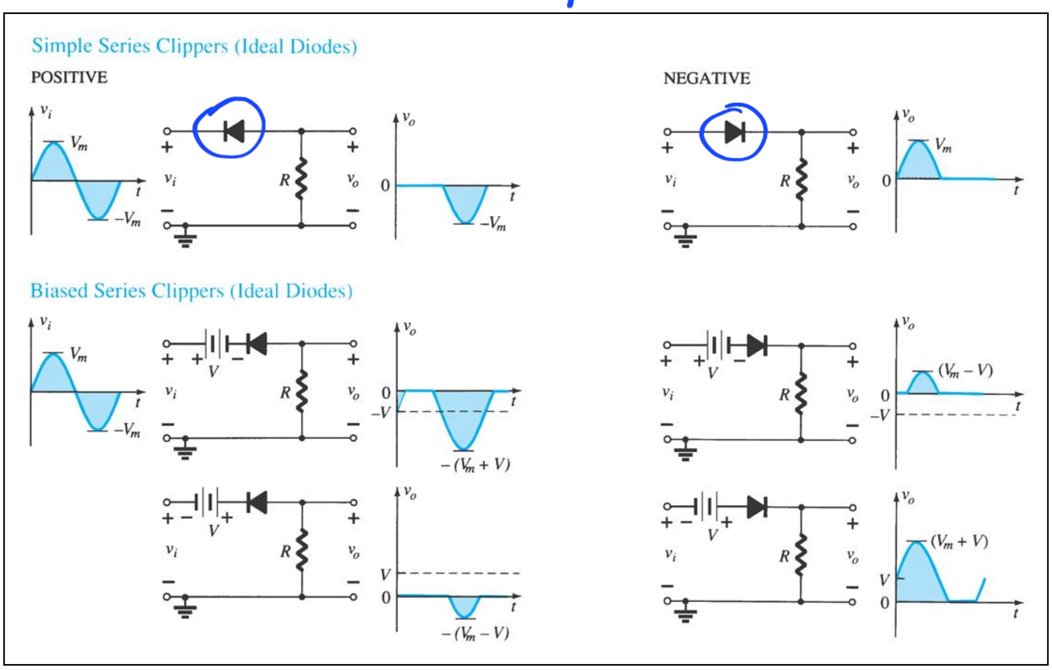


Use Practical Diode Models?



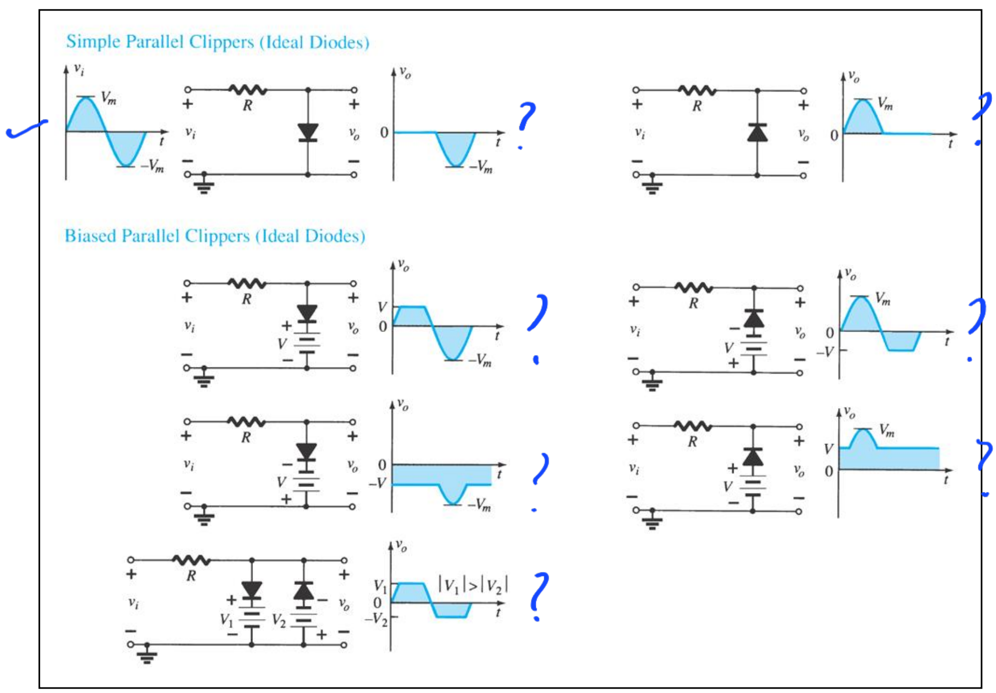
Summary of Clipper Circuits

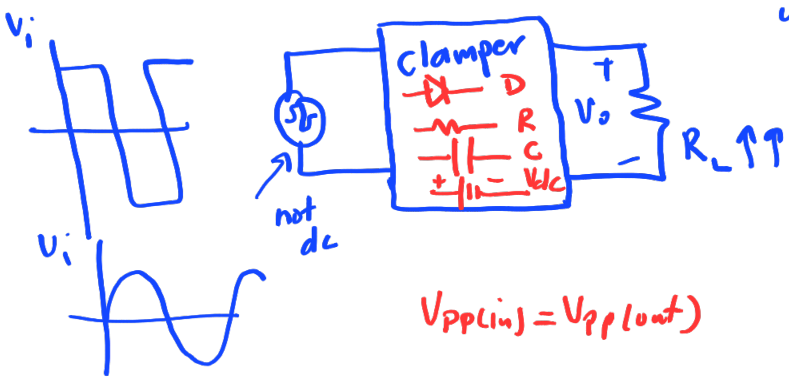
HW for Practice

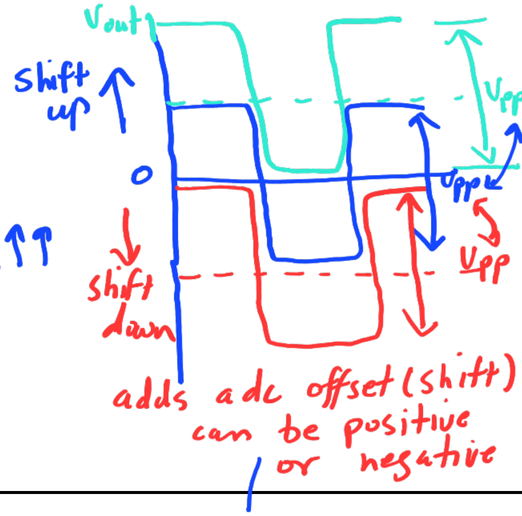


Summary of Clipper Circuits

HW for Practice



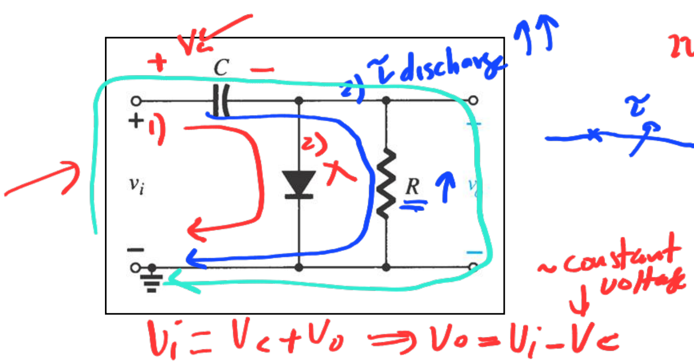


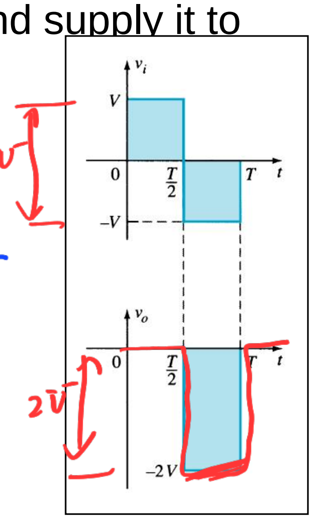


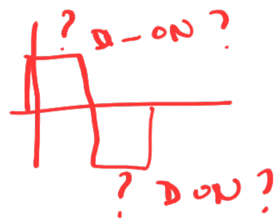
Clampers

Function: A Clamper shifts the input waveform up or down (adds a dc offset) while keeping its shape and peak to peak value unchanged.

It consists of a diode and capacitor (and maybe a series dc source) that can be combined to “clamp” an AC signal to a specific DC level and supply it to the load R







Steps for Clamper Circuit Analysis

1) Start analysis by examining the portion of input that will forward bias the diode

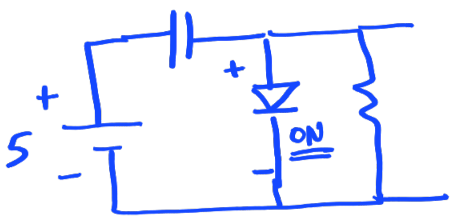
2) During diode On period, assume that the cap is charged instantaneously to a voltage level defined by surrounding network

3) During OFF period, assume the cap holds the established voltage level (i.e. it behaves as constant dc voltage source)

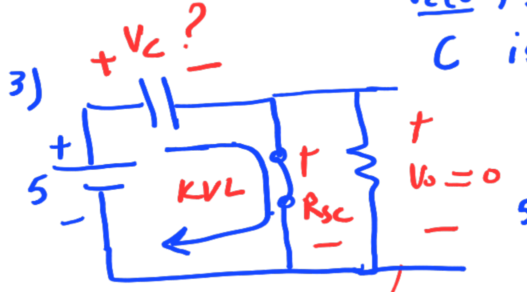
4) Consider value and polarity of Vo

5) Check that total swing (peak to peak) of output equal swing of input.

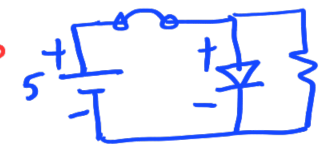
2) $0 - t_1$



3)



1) $V_c(0^-) = 0 \rightarrow$ C is equivalent to short



$5 - V_c = 0 \rightarrow V_c = 5V$

$\tau_{charge} = C \cdot R_{sc} \leftarrow$ very small

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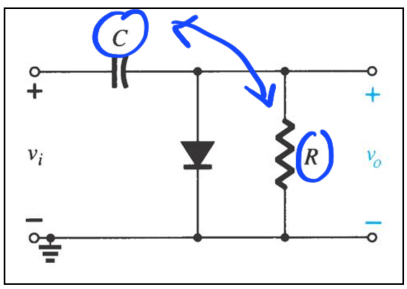
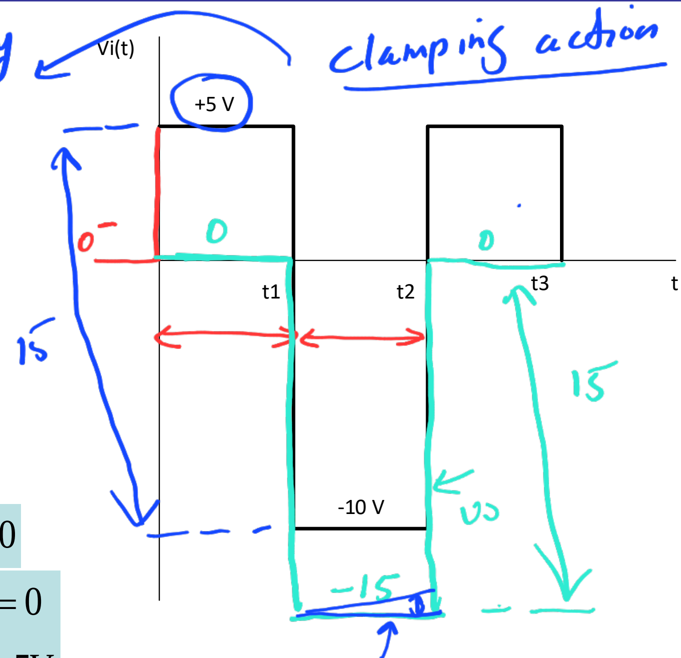
Example

Find and sketch Vo(t)?

in steady state

clamping action





1) For $t < 0$ $(t = 0^-)$ $V_C(0^-) = 0$

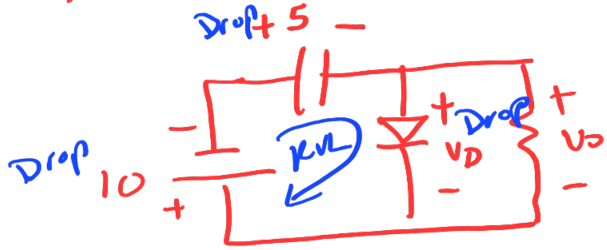
2) For $t > 0$ $(t = 0+)$ $V_C(0^+) = 0$

$Vi(0^+) = 5V$

$\Rightarrow D1$ is ON and it is replaced by short circuit

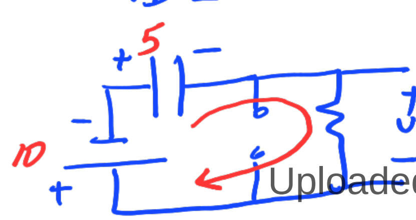
3) for $0^+ < t < t_1$ equivalent circuit is $\Rightarrow$ see next page

4) $t_1 - t_2 \rightarrow V_i = -10$, $V_c = 5V$, Diode ??



$10 + 5 + V_D = 0$

$V_D = -15 < 0 \rightarrow$ D is off



$V_o = -15$

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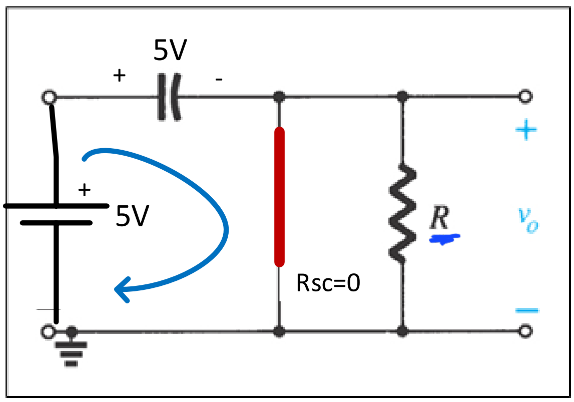

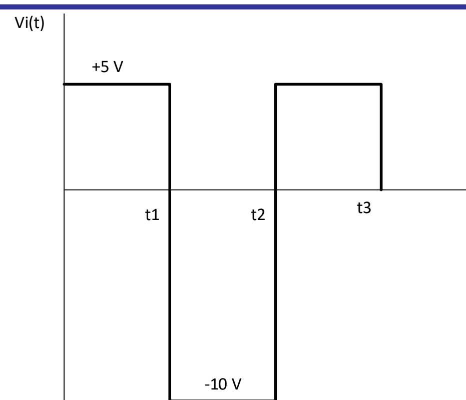

$\Rightarrow D1$ is ON, Cap charges instantously to +5V with shown polarity since $\tau_{\text{charge}} = R_{sc}.C \cong 0$ and Vo(t) = 0 V

4) for $t_1 < t < t_2$ voltage source reverses polarity, Vi(t) = -10V while Cap keeps its charge Vc = 5V since $\tau_{\text{discharge}} = R.C$ is large

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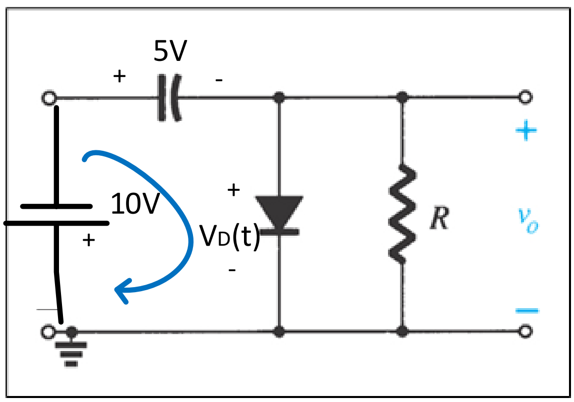
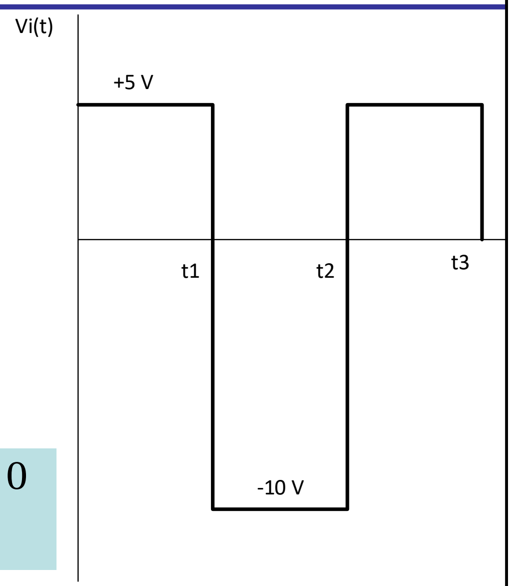
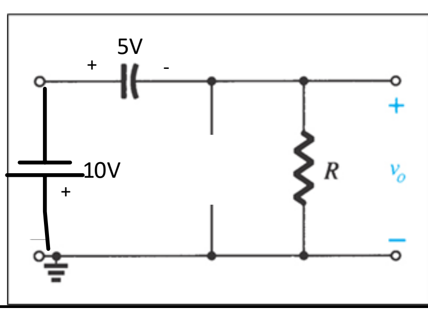




$$\text{KVL around the loop: } -10 - 5 - V_D(t) = 0$$
$$\Rightarrow V_D(t) = -15\text{ V} < 0, \therefore \text{diode is OFF}$$

$$Vo(t) = V_D(t) = -15\text{ V}$$



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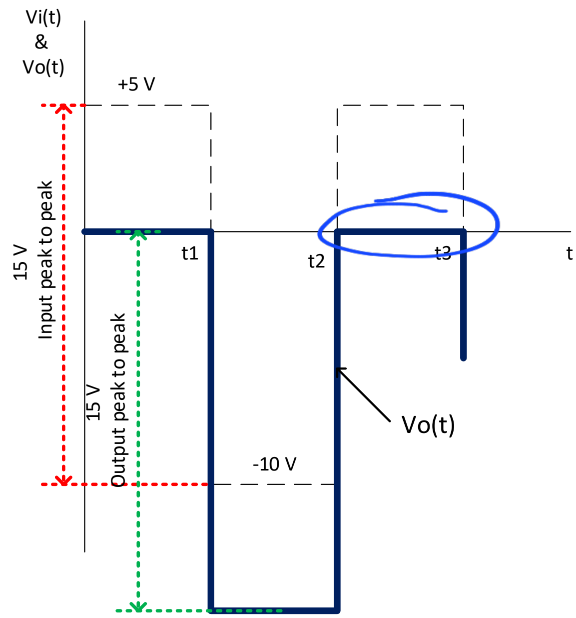
5) for $t_2 < t < t_3$, $Vi(t) = 5V$

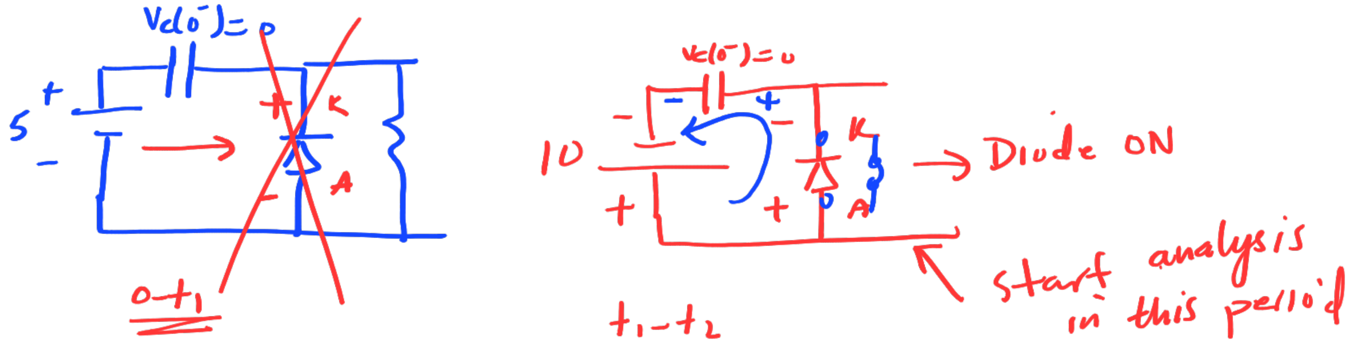
while $Vc = 5V$

$V_D(t) = 5 - 5 = 0$

Diode is OFF and it will remain always off no matter what happens to Vi(t)

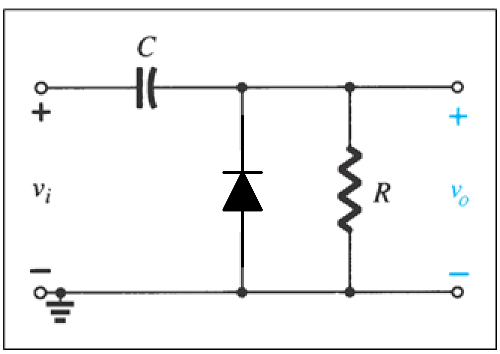
$Vo(t) = V_D(t) = Vi(t) - 5$

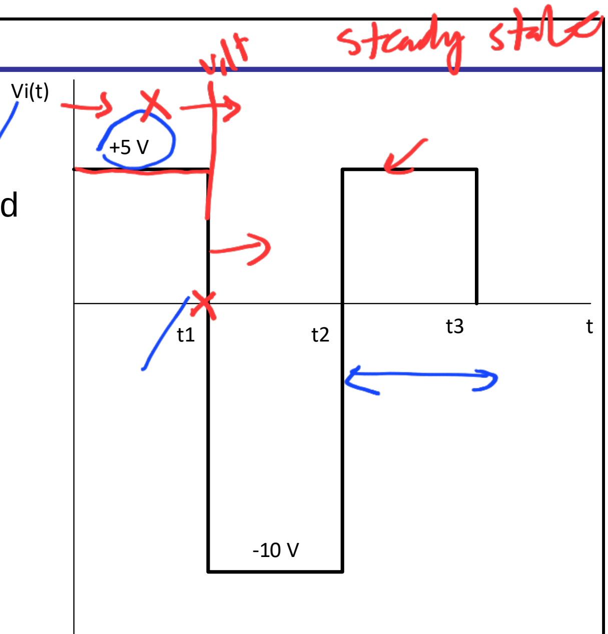




Example

What happens if the diode was inversed

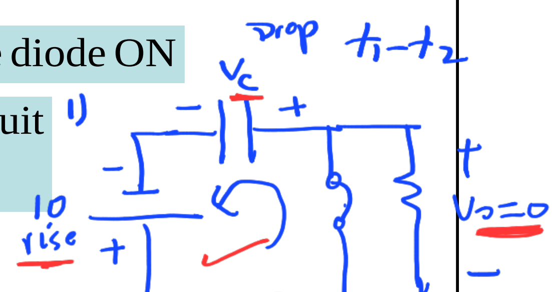


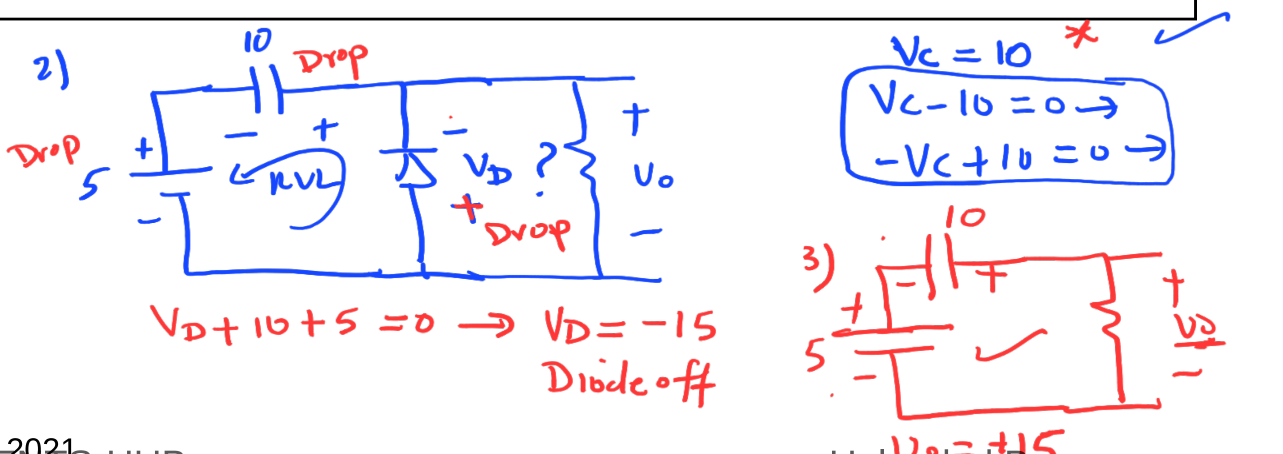


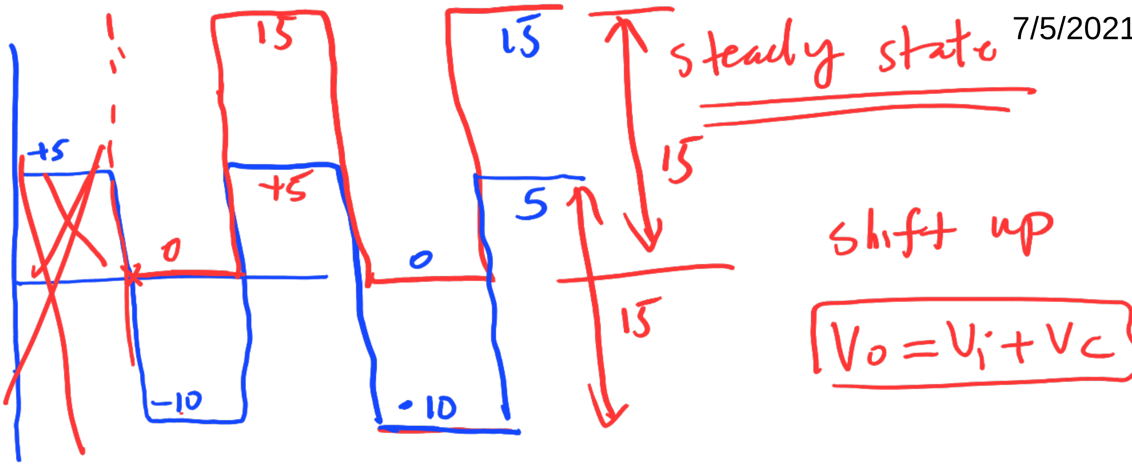
1) Consider $t_1 < t < t_2$ which makes the diode ON

$\Rightarrow$ *D* is ON and it is replaced by short circuit

$Vo(t) = 0V$







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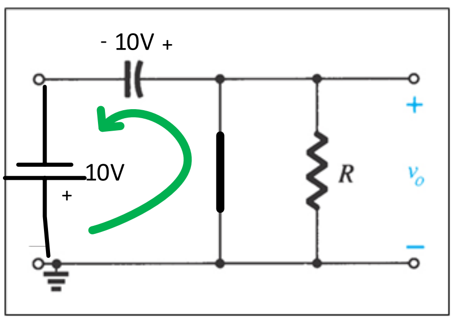
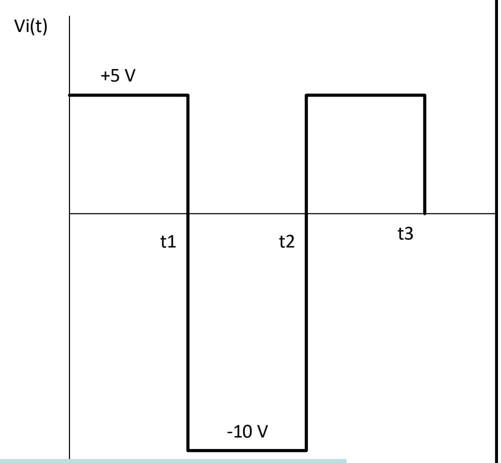
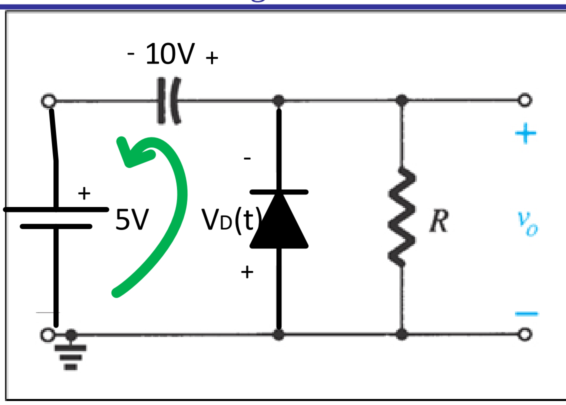
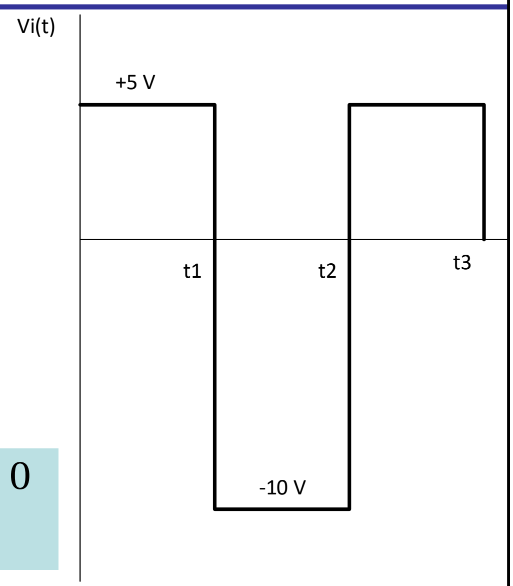
Cap is charged to 10V with shown polarity due to diode forward current Vo(t) = 0 V



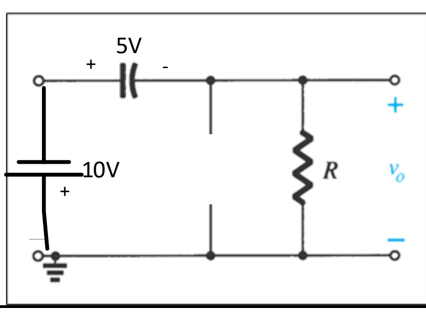


2) for $t_2 < t < t_3$ voltage source reverses polarity, Vi(t) = +5V while Cap keeps its charge Vc = 10V





$$\text{KVL around the loop}: \quad 10 + 5 + V_D(t) = 0$$
$$\Rightarrow V_D(t) = -15\text{ V} < 0, \therefore \text{diode is OFF}$$



$$Vo(t) = -V_D(t) = 15\text{ V}$$

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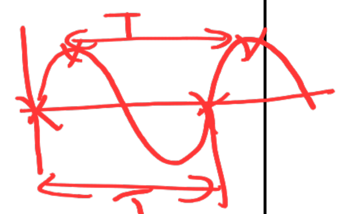
Afterwords for any value of the given Vi(t) diode remains OFF and $Vo(t) = Vi(t) + 10$

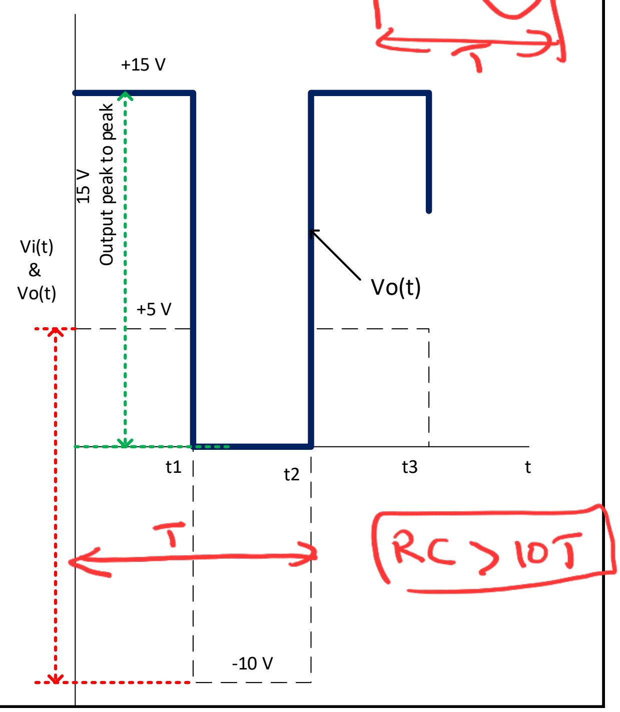


$\therefore$ the clamper charges a cap and uses this charge to add up to the input to shift it up or down (i.e. add dc offset)

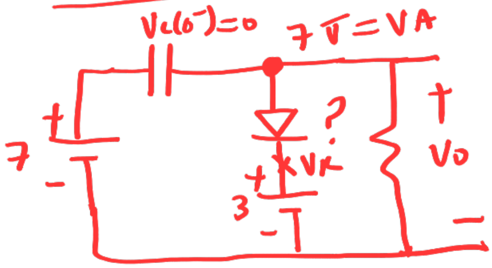
Important Note *

For Proper Clamping action, $\tau_{discharge}$ must be large enough (at least 10 times the period of the input waveform)

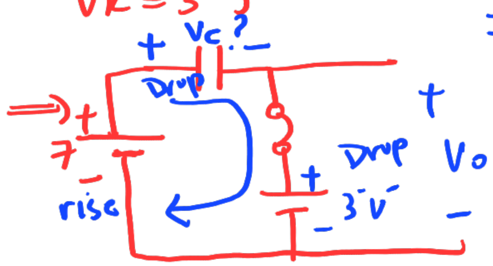
$$\tau_{discharge} = R.C > 10\,(t_1 + t_2)$$



$0 - t_1 \rightarrow V_i = +7$



VA = 7, VK = 3 } Diode ON 1)



$7 = V_c + 3$

$\therefore V_c = 4\ V$

$V_o = 3\ V$

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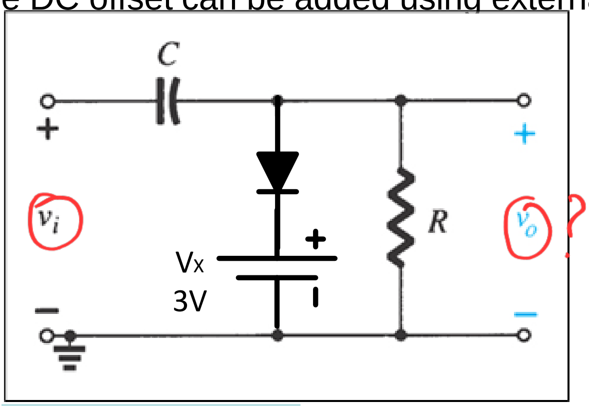
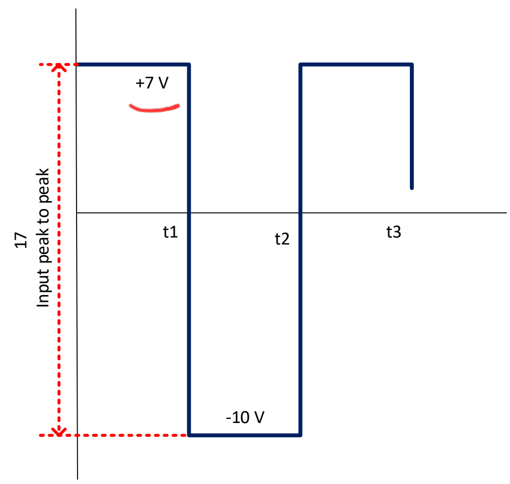
More DC offset can be added using external voltage source





1) When $Vi = +7\ V$

$7 - Vc(t) - Vx = 0$

$\therefore Vc(t) = 7 - 3 = 4\ V$

$\Rightarrow Vo(t) = Vx = 3\ V$

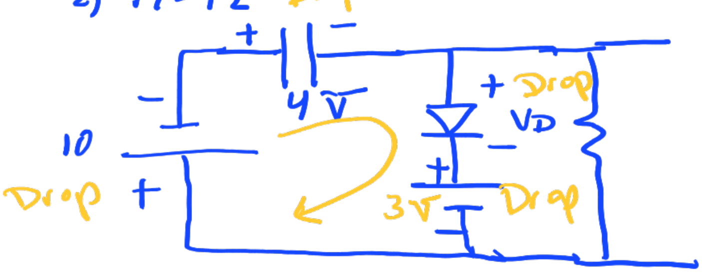
2) for $Vi = -10V$

$-10 - 4 - V_D(t) - 3 = 0$

$\Rightarrow V_D(t) = -17\ V \ < 0$ and diode is OFF

$$\Rightarrow Vo(t) = Vi(t) - V_C(t)$$
$$= Vi(t) - 4$$
$$= -10 - 4 = -14V$$

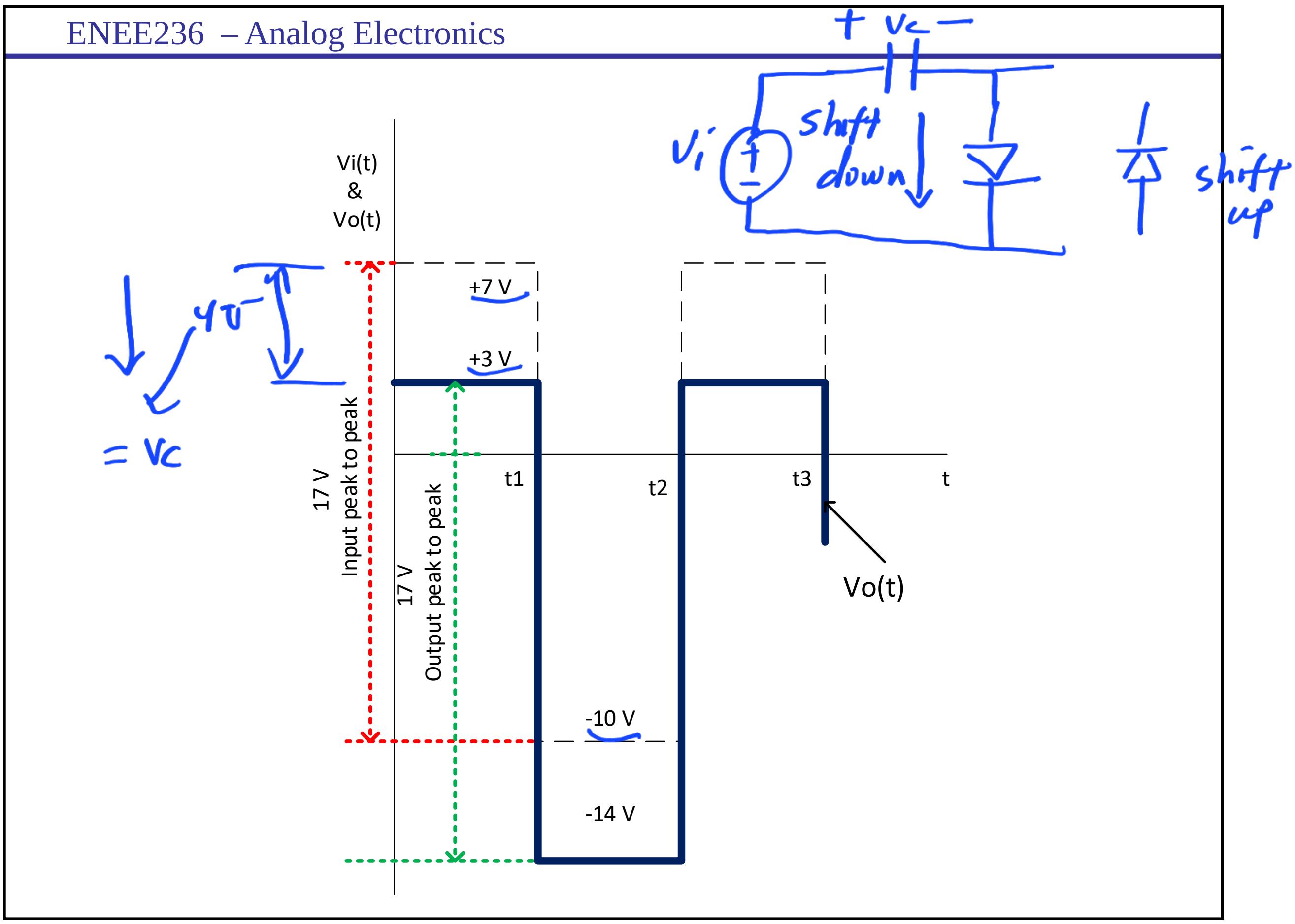
2) $t_1 - t_2$



$10 + 4 + V_D + 3 = 0$

$\therefore V_D = -17\ V < 0$

Diode off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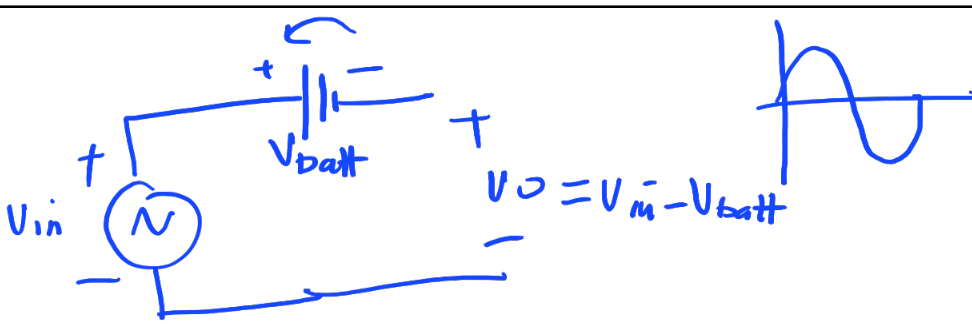
Vi(t)
&
Vo(t)
+7 V
+3 V
t1
t2
t3
t
17 V
Input peak to peak
17 V
Output peak to peak
-10 V
-14 V
Vo(t)
+ Vc −
Vi
shift
down
shift
up
4V
= Vc


+
−
Vbatt
+
Vin
−
+
Vo = Vin − Vbatt
−

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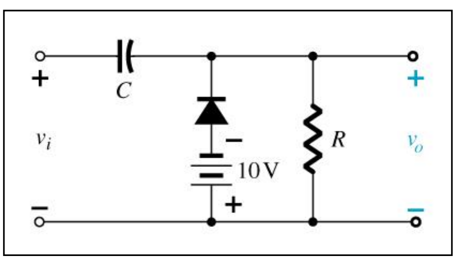
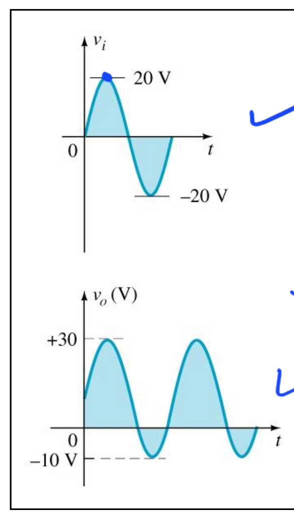
For Self study

Biased Clamper Circuits

The input signal can be any type of waveform such as a sine, square, or triangle wave.



The DC source lets you adjust the DC clamping level.



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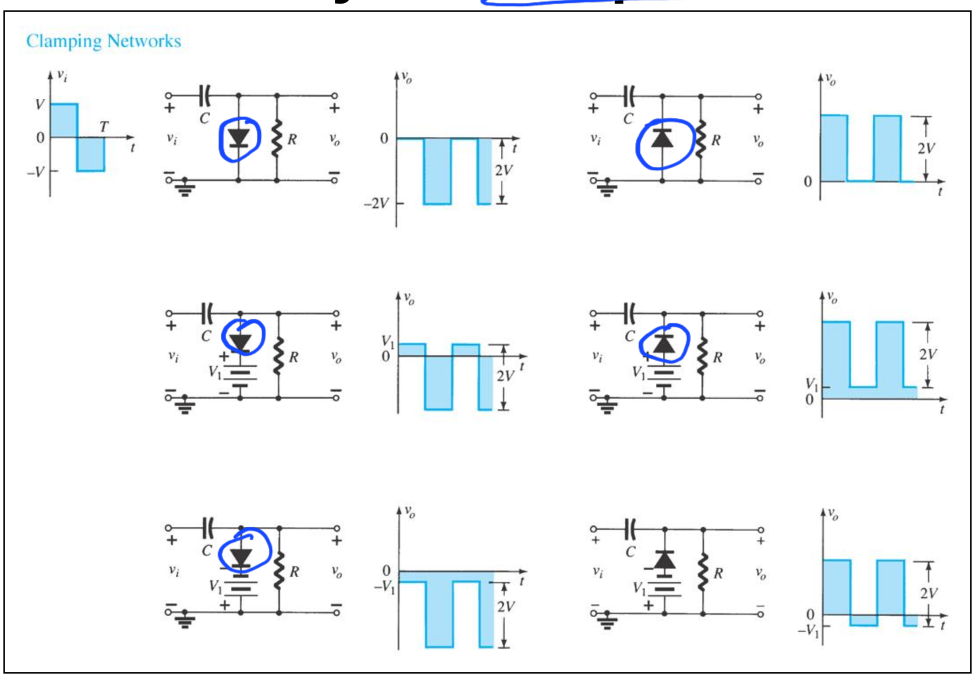
Practice
solve

Summary of Clamper Circuits



End of L5
End of T3

مادة الكويز لغاية هنا
يوم السبت