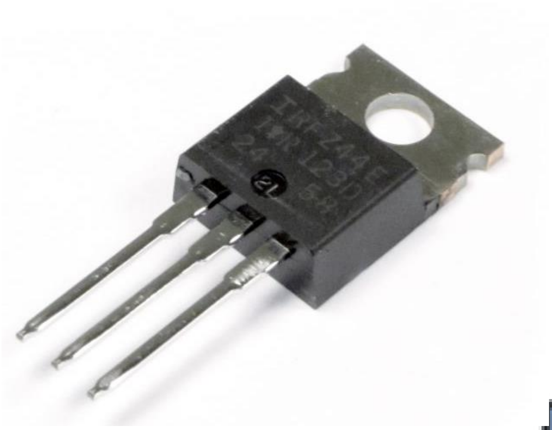
Field Effect Transistor- FET

FET Vs conventional Transistors

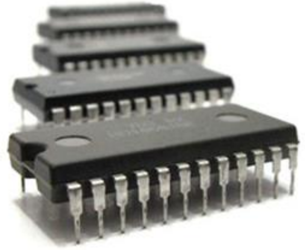


Advantages

1- High input impedance ; 100 M Ω

2- fewer steps in manufacturing process.

3- more devices can be package into smaller area for integrated circuit IC

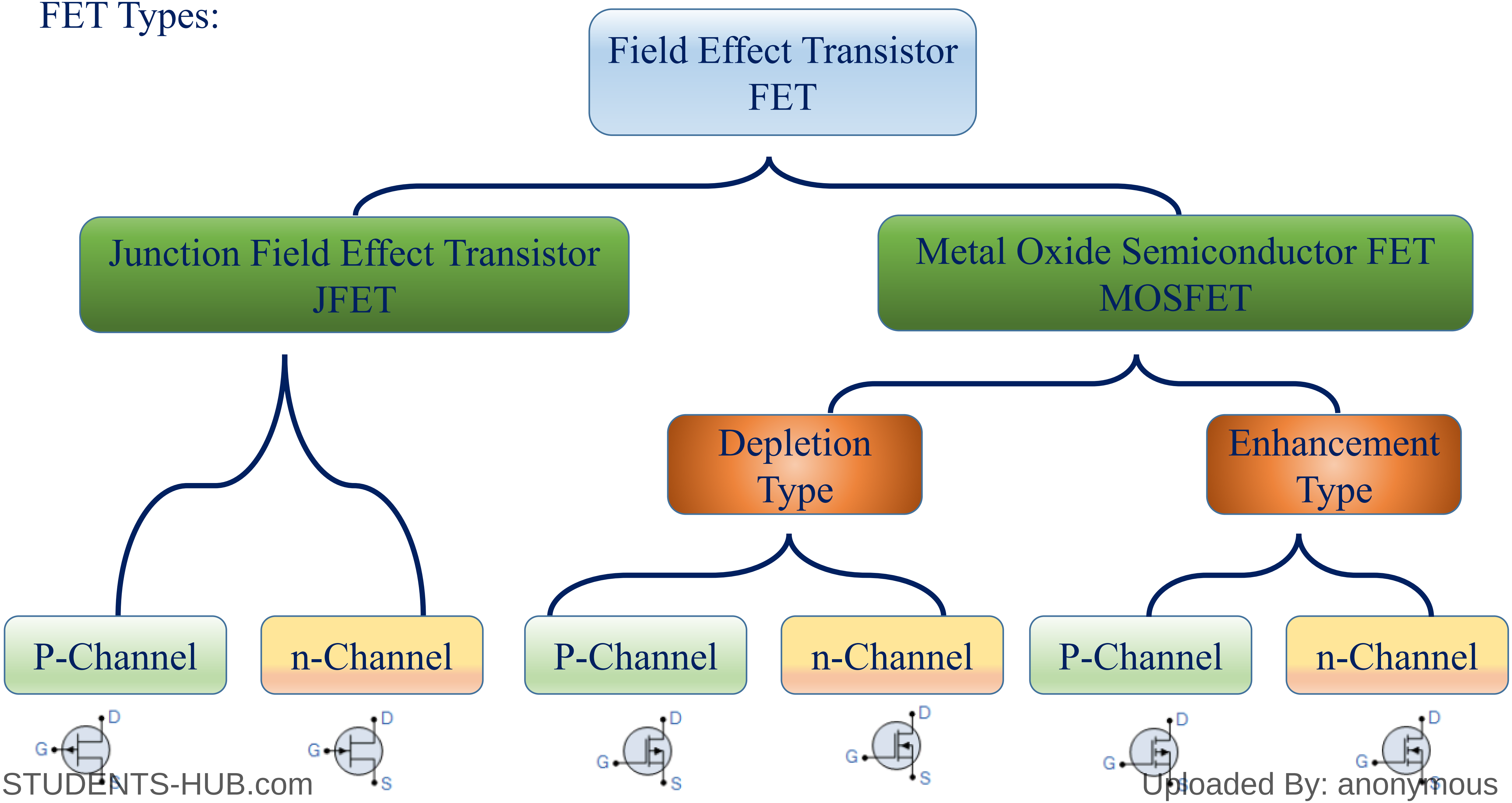


Disadvantages

1- Low values of voltage gain.

2- Poor high frequency performance.

FET Types:

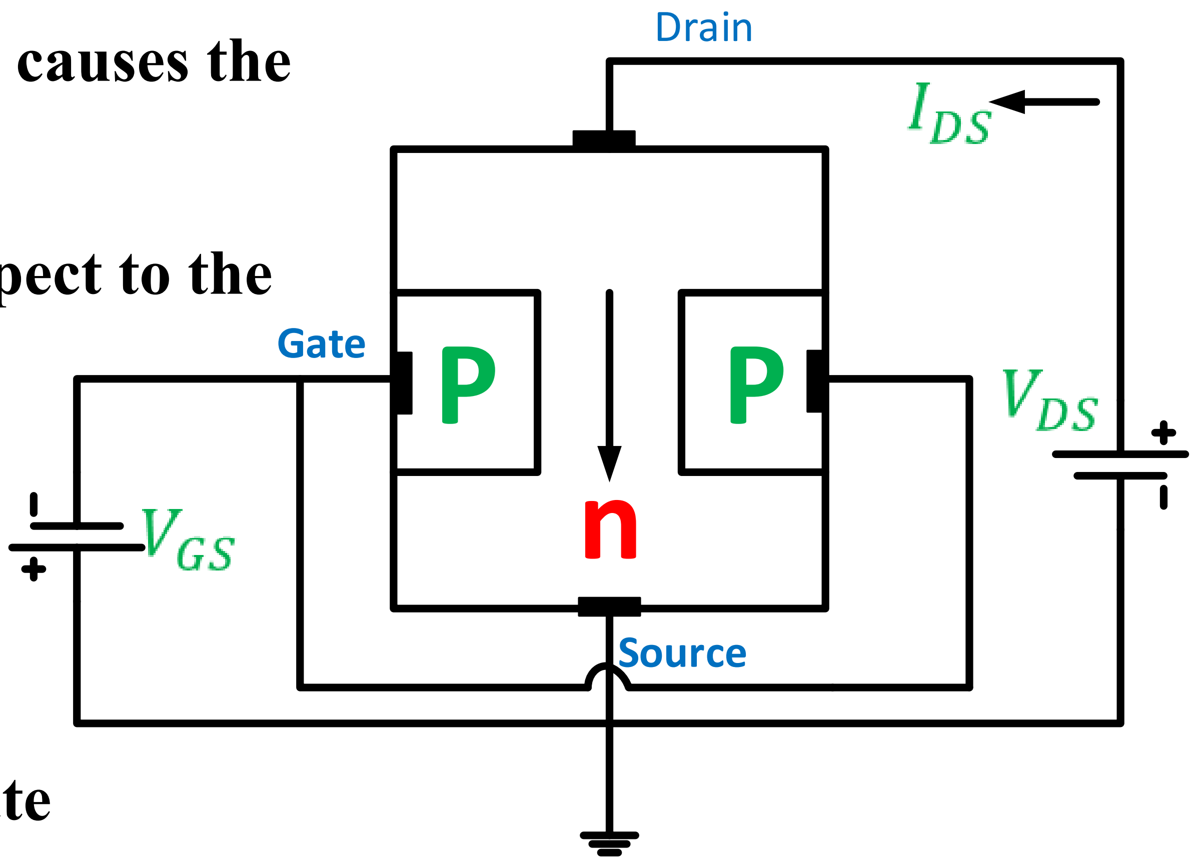

Field Effect Transistor
FET
Junction Field Effect Transistor
JFET
Metal Oxide Semiconductor FET
MOSFET
Depletion
Type
Enhancement
Type
P-Channel
n-Channel
P-Channel
n-Channel
P-Channel
n-Channel
G
D
S

Junction Field Effect Transistor JFET

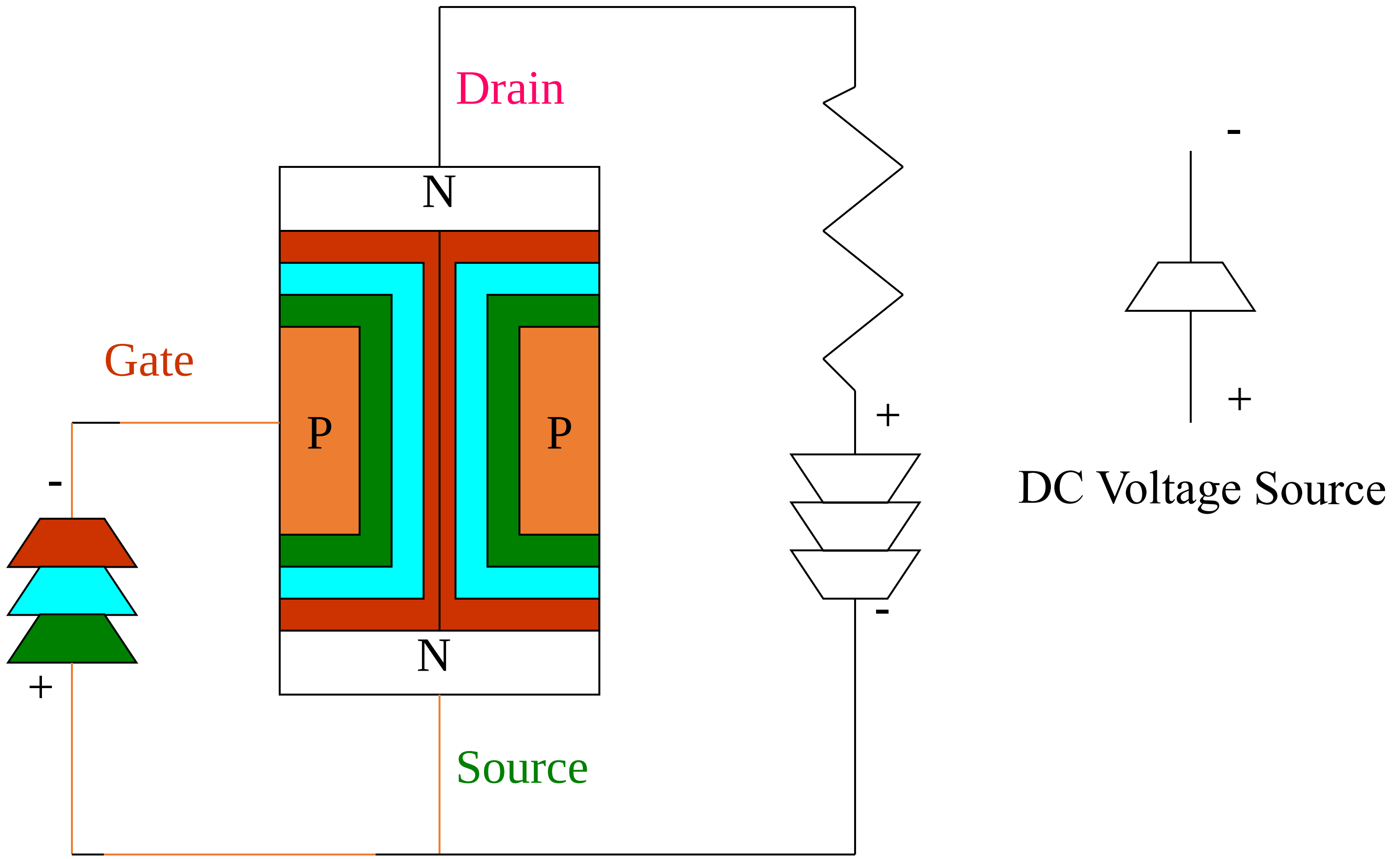
JFET construction:

- ✓ Revers biasing the gate to source junctions causes the formation of the depletion region
- ✓ The drain has the proper polarity with respect to the source to establish the drain current I_{DS}
- ✓ The value of I_{DS} depends on the width of the channel.
- ✓ The width of the channel is controlled by revers biasing the pn-junctions between gate and source .
- ✓ If the channel width increases I_{DS} increases .

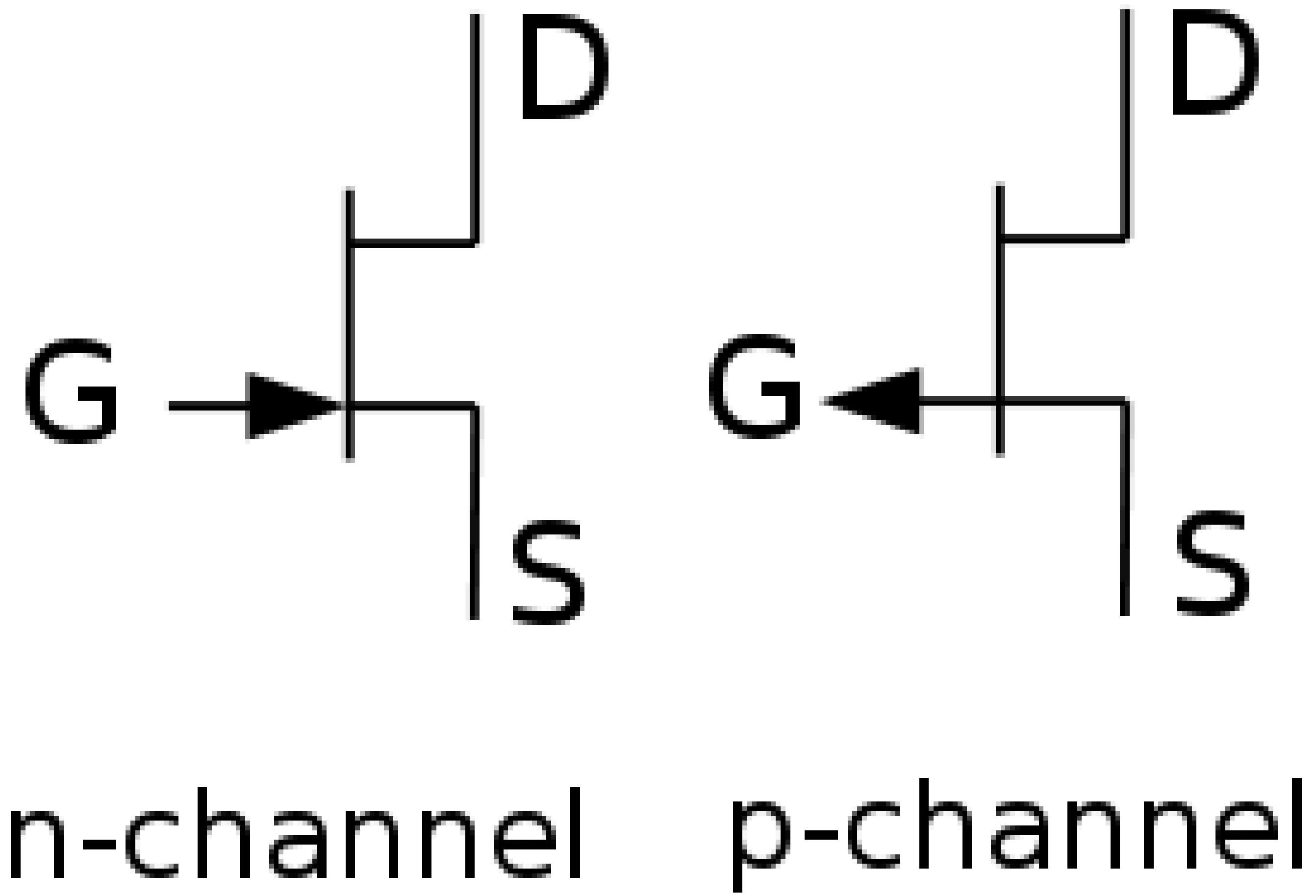
n-channel JFET



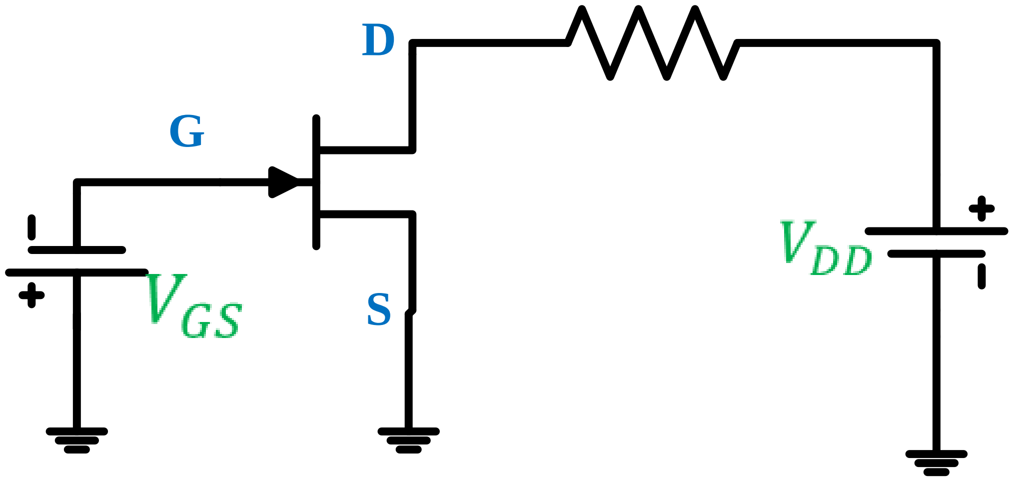
Operation of a JFET

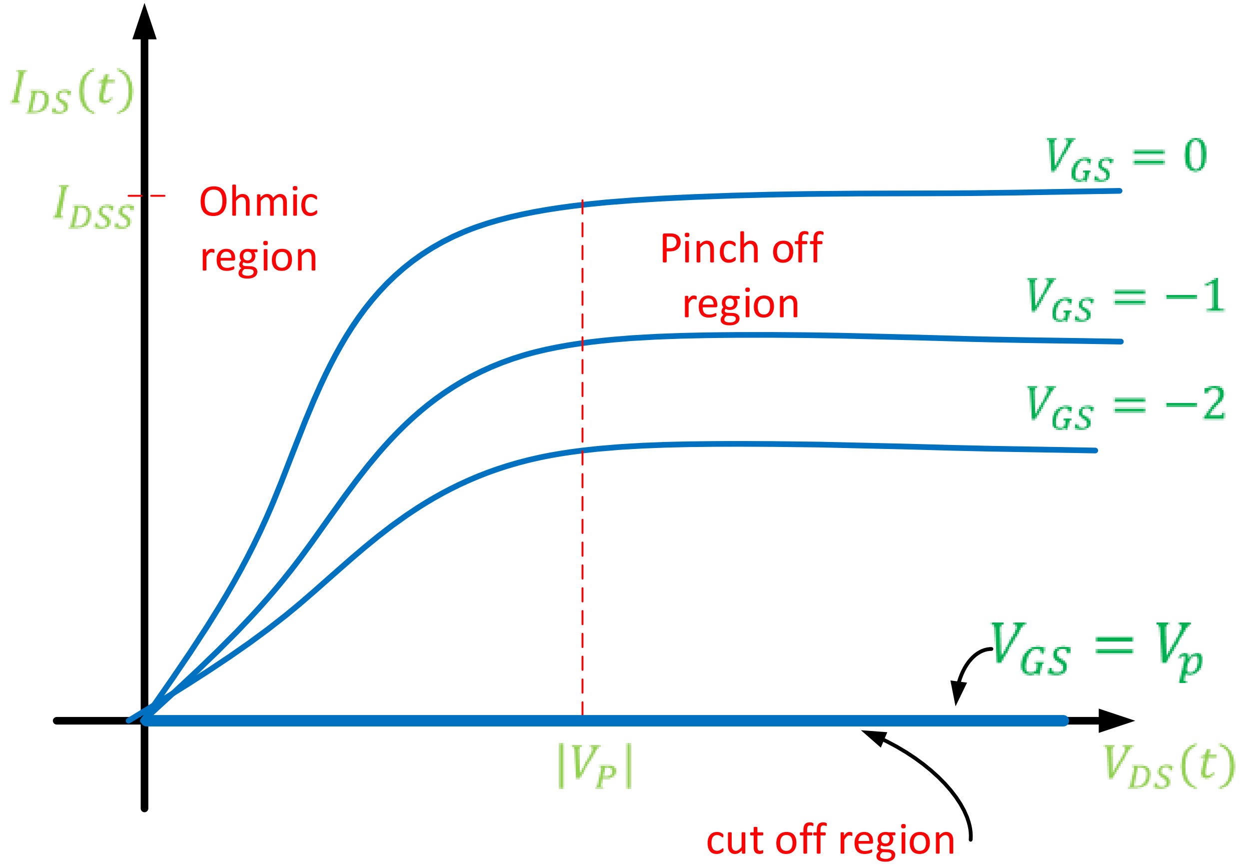


JFET Circuit Symbol:



JFET output characteristic:

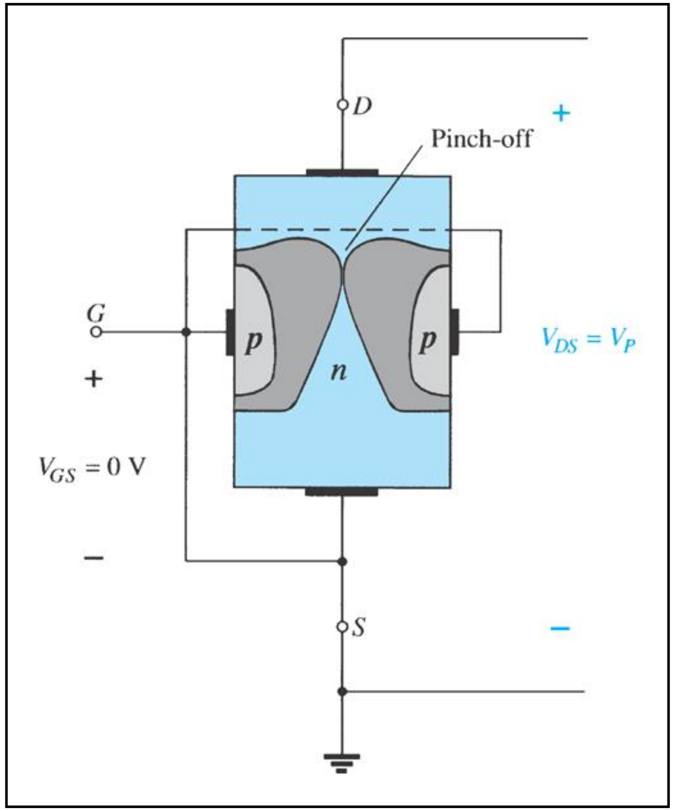




JFET Characteristics: Pinch Off

- If V_{GS} = 0 V and V_{DS} continually increases to a more positive voltage, a point is reached where the depletion region gets so large that it pinches off the channel.

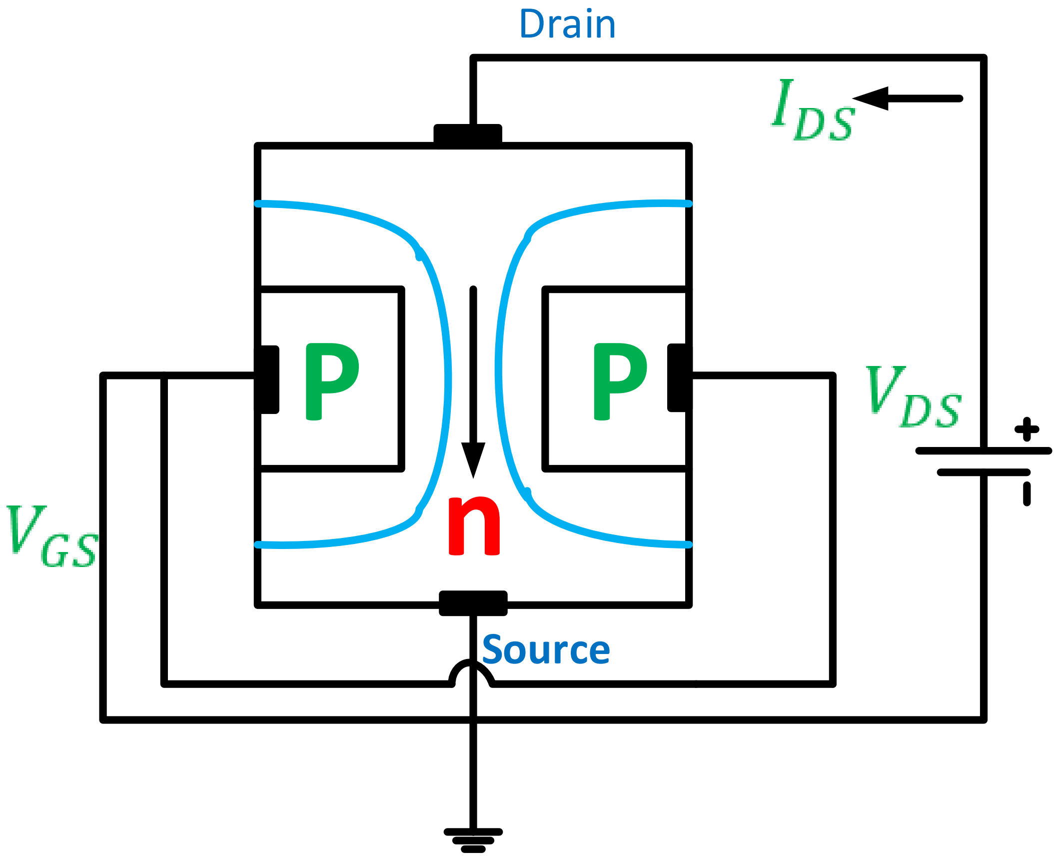
  - This suggests that the current in channel (I_D) drops to 0 A, but it does not: As V_{DS} increases, so does I_D. However, once pinch off occurs, further increases in V_{DS} do not cause I_D to increase.



Pinch of voltage V_P:

For $V_{GS} = 0$,the value of V_{DS} at witch I_{DS} becomes essentially constant
Is the absolute of the pinch of voltage
$V_{DS} = |V_P|$

$$V_P = \begin{cases} negative\ value\ for\ n\_channel \\ positive\ value\ for\ p\_channel \end{cases}$$



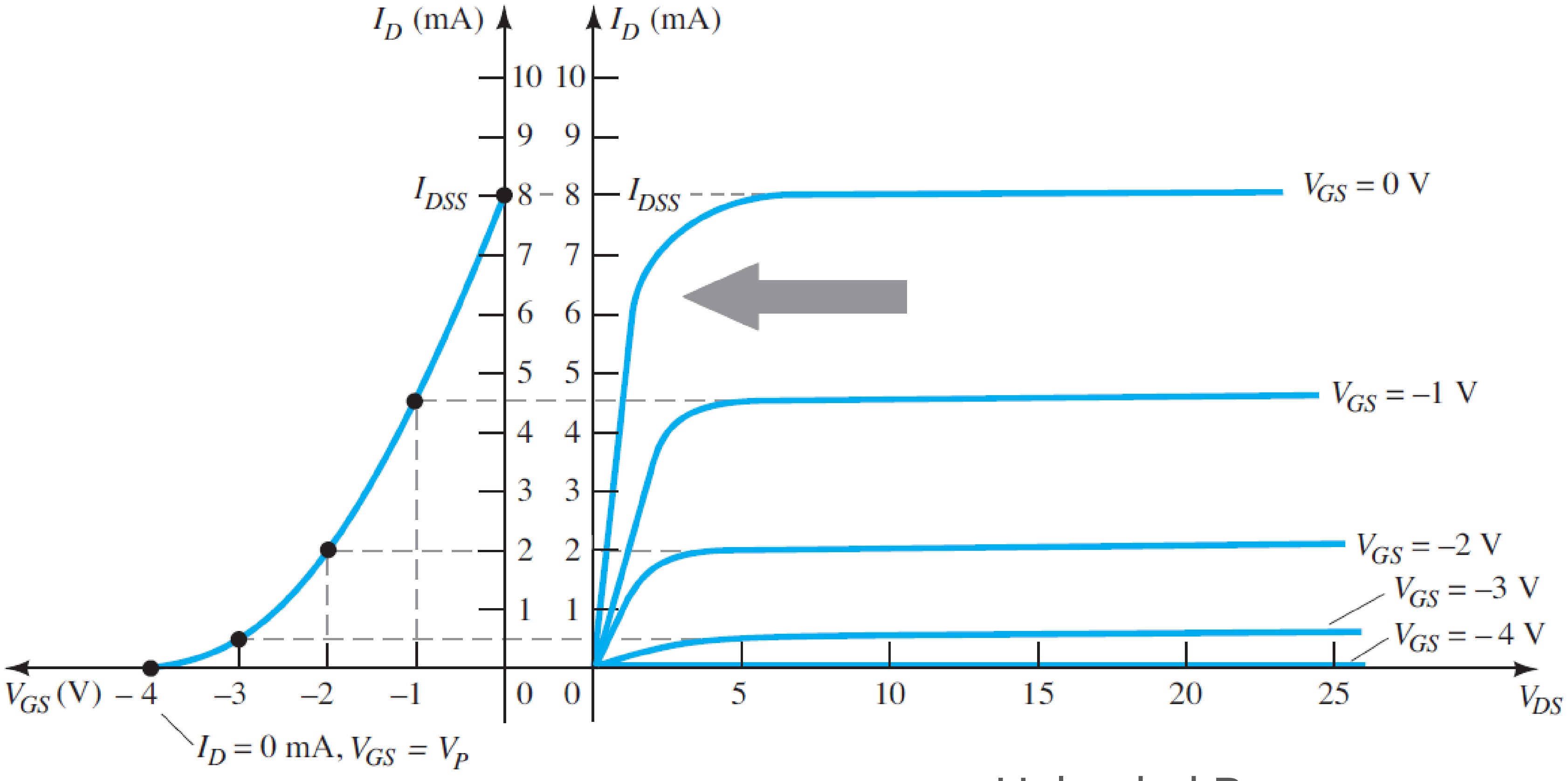
JFET Transfer characteristic curve:

$$I_{DS}(\mathrm{t}) = I_{DSS}\left(1 - \frac{V_{GS}(t)}{V_P}\right)^2$$

In pinch off region:

$$V_P < V_{GS} \leq 0$$

$$|V_{DS}| > |V_P| - |V_{GS}|$$



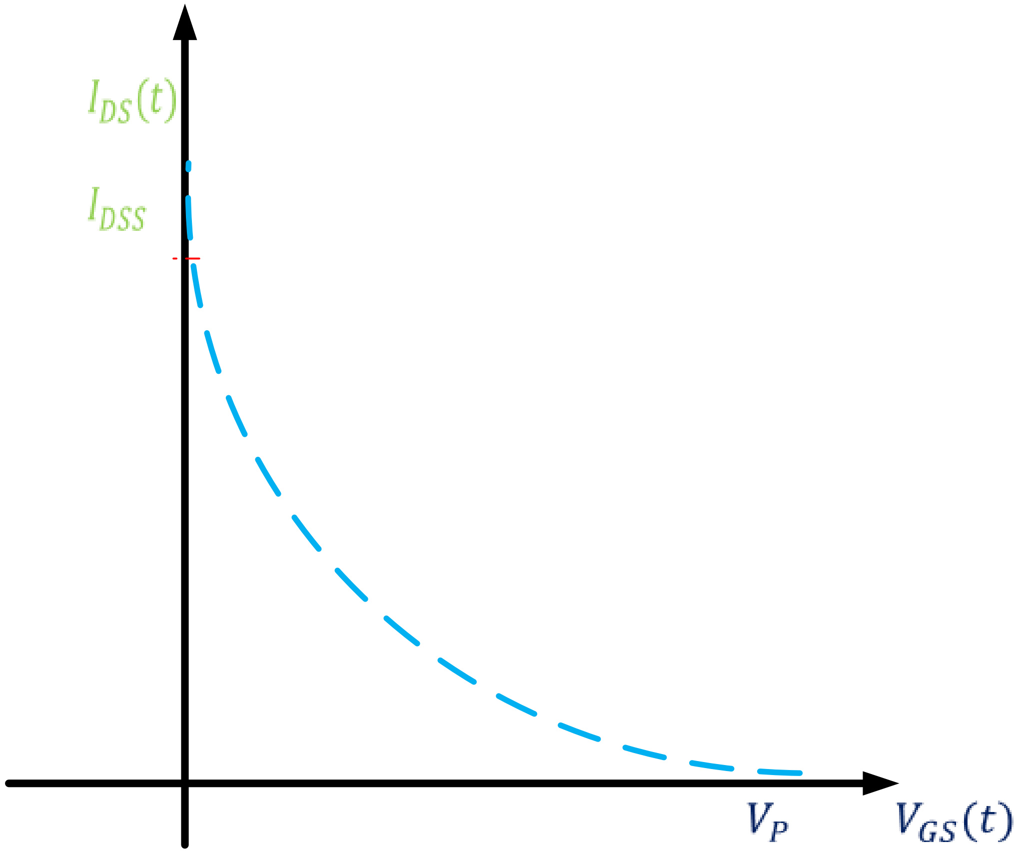
P-channel JFET

$$I_{DS}(t) = I_{DSS}\left(1 - \frac{V_{GS}(t)}{V_P}\right)^2$$

In pinch off region:

$$|V_{DS}| > |V_P| - |V_{GS}|$$

$$V_P > V_{GS} \geq 0$$



Summary

Pinch off voltage:

- ✓ The voltage that cusses the depletion region to touch and close the channel is called pinch off voltage

- ✓ For the n-channel JFET to be in the pinch off region:

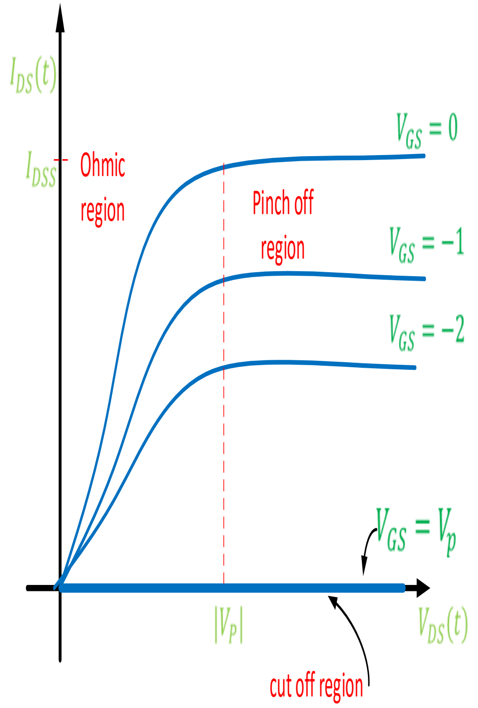
$$V_P < V_{GS} \le 0$$

$$|V_{DS}| > |V_P| - |V_{GS}|$$

- ✓ For the p-channel JFET to be in the pinch off region:

$$|V_{DS}| > |V_P| - |V_{GS}|$$

$$V_P > V_{GS} \ge 0$$

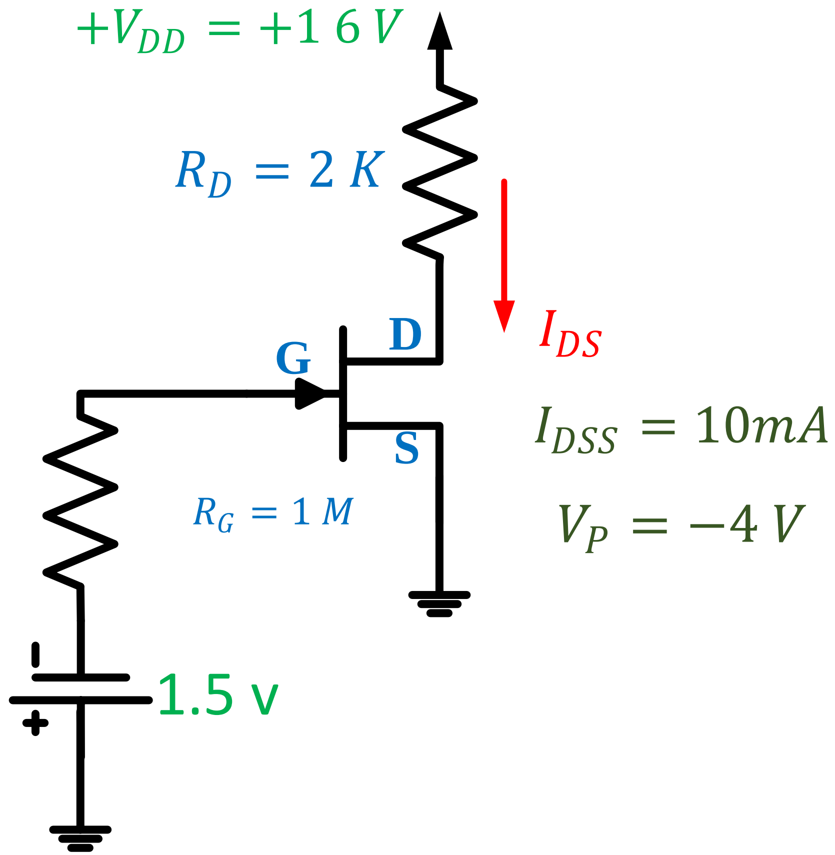


JFET Biasing Circuit

1) Fixed bias circuit

Find Q_{point}

Since V_{GS} = -1.5 V , the JFET could be either in the ohmic or pinch off region



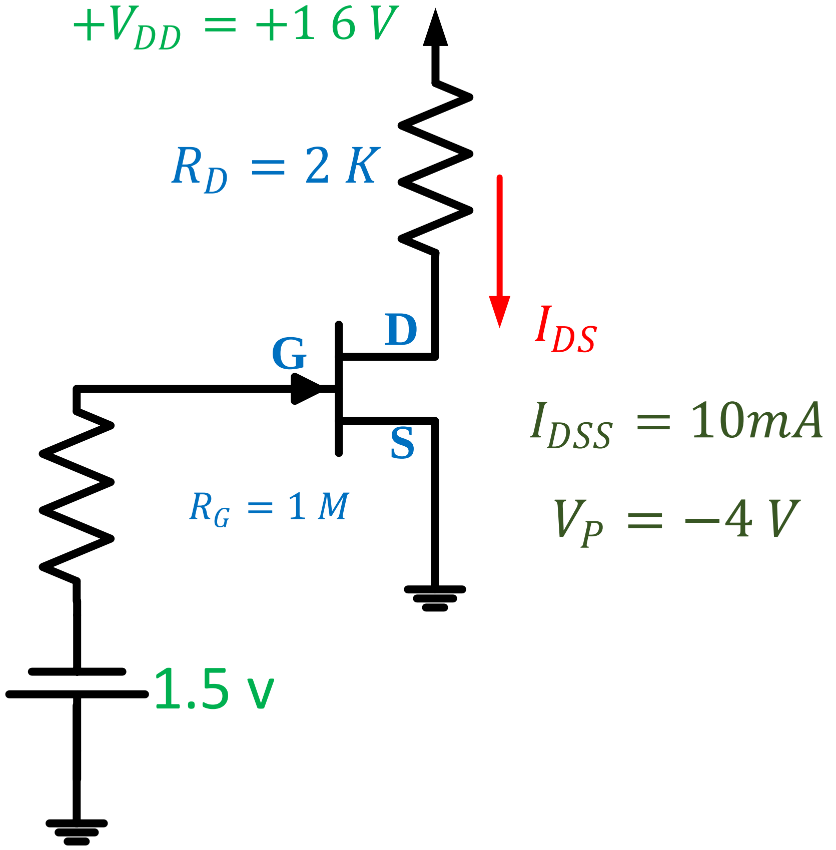
Assume that the JFET is in the pinch off region

$$\therefore\ I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$V_{GS} = V_G - V_S$$

VGS = -1.5 – 0 = -1.5 V

$$\therefore\ I_{DS} = 3.9mA$$



KVL:

$$V_{DD} = R_D I_{DS} + V_{DS}$$

$$\therefore V_{DS} = 8.2\text{ V}$$

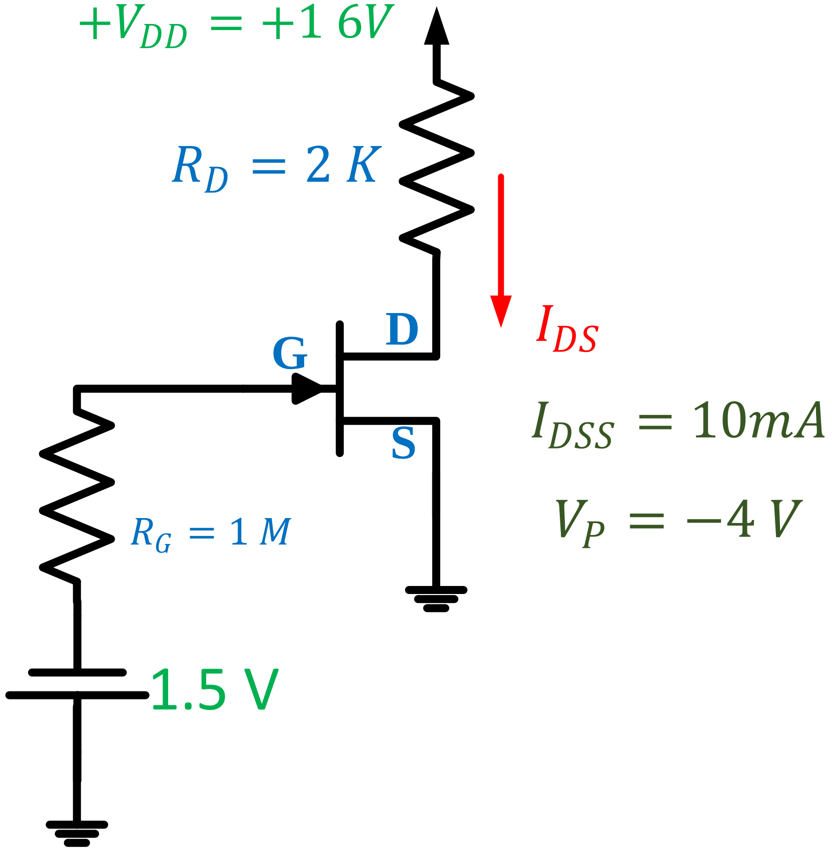
For the JFET is in the pinch off region

$$|V_{DS}| > |V_P| - |V_{GS}|$$

$$> |-4| - |-1.5|$$

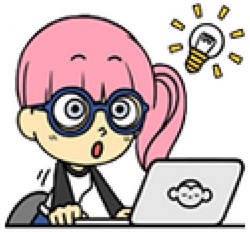
$$|V_{DS}| > 2.5\text{ V}$$

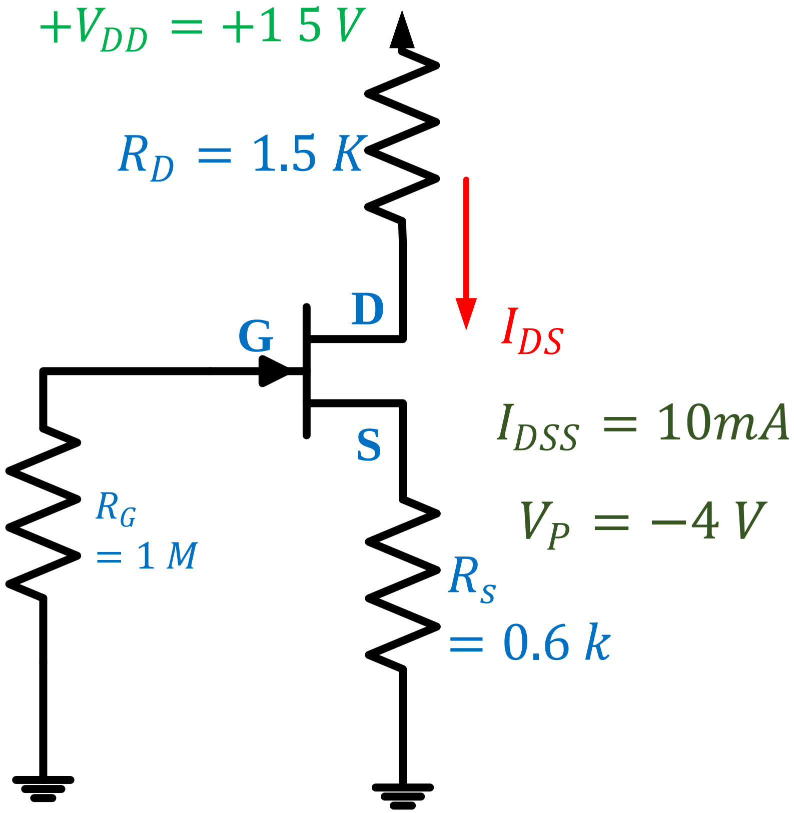
since V_{DS} >2.5 V ; $\therefore$ our assumption is ok



2) Self – bias circuit

- **Assume that the JFET is in the pinch off region**





$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$V_{GS} = V_G - V_S$$

$$V_{GS} = -(0.6K)\, I_{DS}$$

Sub 2 into 1

$$\therefore\ I_{DS} = 10\ x10^{-3}\left(1- \frac{-0.6KI_{DS}}{-4}\right)^2$$

I_{DS} = 14.77 mA , 3mA

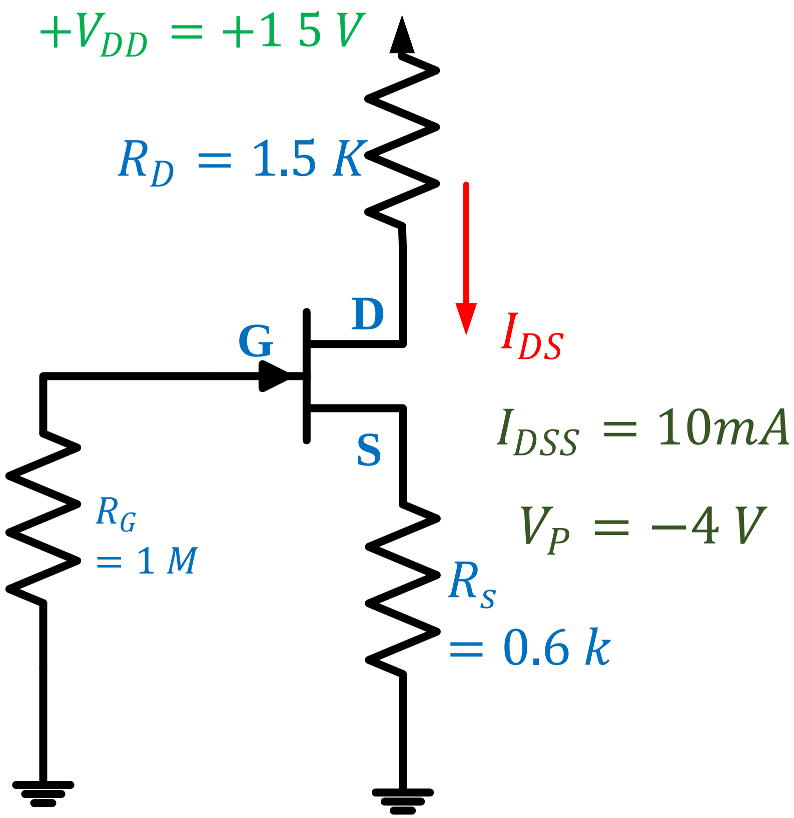
Since I_{DS} = 14.77mA $> I_{DSS}$

$\therefore\ I_{DS}$ = 3mA

V_{GS} = -1.8 V

$V_{DD} = R_D I_{DS} + V_{DS} + R_S I_{DS}$

V_{DS} = 8.7 V



For the JFET to be in the pinch off

- $|V_{DS}| > |V_P|$-$|V_{GS}|$
  $>$ |-4| - |-1.8|
  $|V_{DS}|$ $>$2.2 V

- Since $|V_{DS}| > 2.2$ V , the JFET is in the pinch off region and our

  assumption is ok and

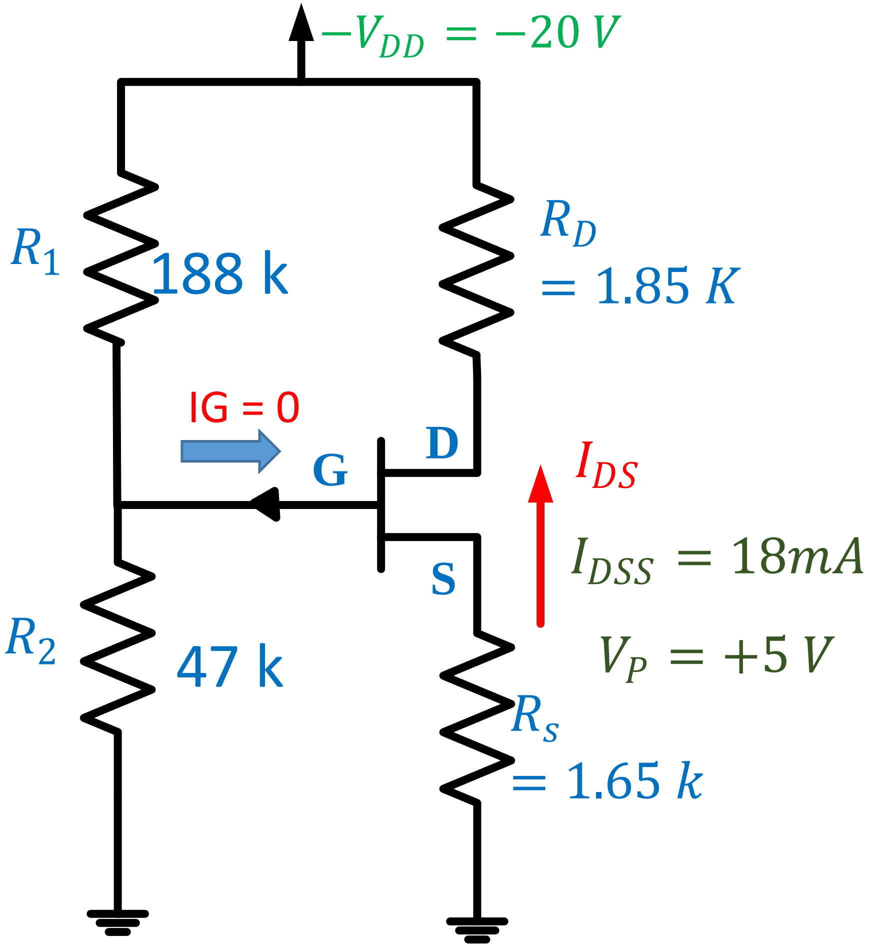
- I_{DS} = 3.0 mA

  V_{DS} = 8.7 V

  V_{GS} = -1.8 V

3) Voltage Divider bias circuit

$\boldsymbol{I_{DS}} = \boldsymbol{I_{DSS}}(1 - \frac{\boldsymbol{V_{GS}}}{\boldsymbol{V_P}})^{2}$ 1



$\boldsymbol{V_{GS}} = \boldsymbol{V_G} - \boldsymbol{V_S}$

$\boldsymbol{V_G} = \frac{47K}{47K+188K}(-20) = -4$ V

$\boldsymbol{V_S} = -\boldsymbol{R_S I_{DS}} = -(1.65\text{K})\ \boldsymbol{I_{DS}}$

KVL:

$\boldsymbol{V_{GS}} = -4 + (1.56\text{K})\ \boldsymbol{I_{DS}}$............2

sub 2 into 1 , we obtain

$$\boldsymbol{I_{DS}} = \begin{cases} \boldsymbol{4.02mA} & \surd \\ \boldsymbol{7.4\ mA} & \boldsymbol{X} \end{cases}$$

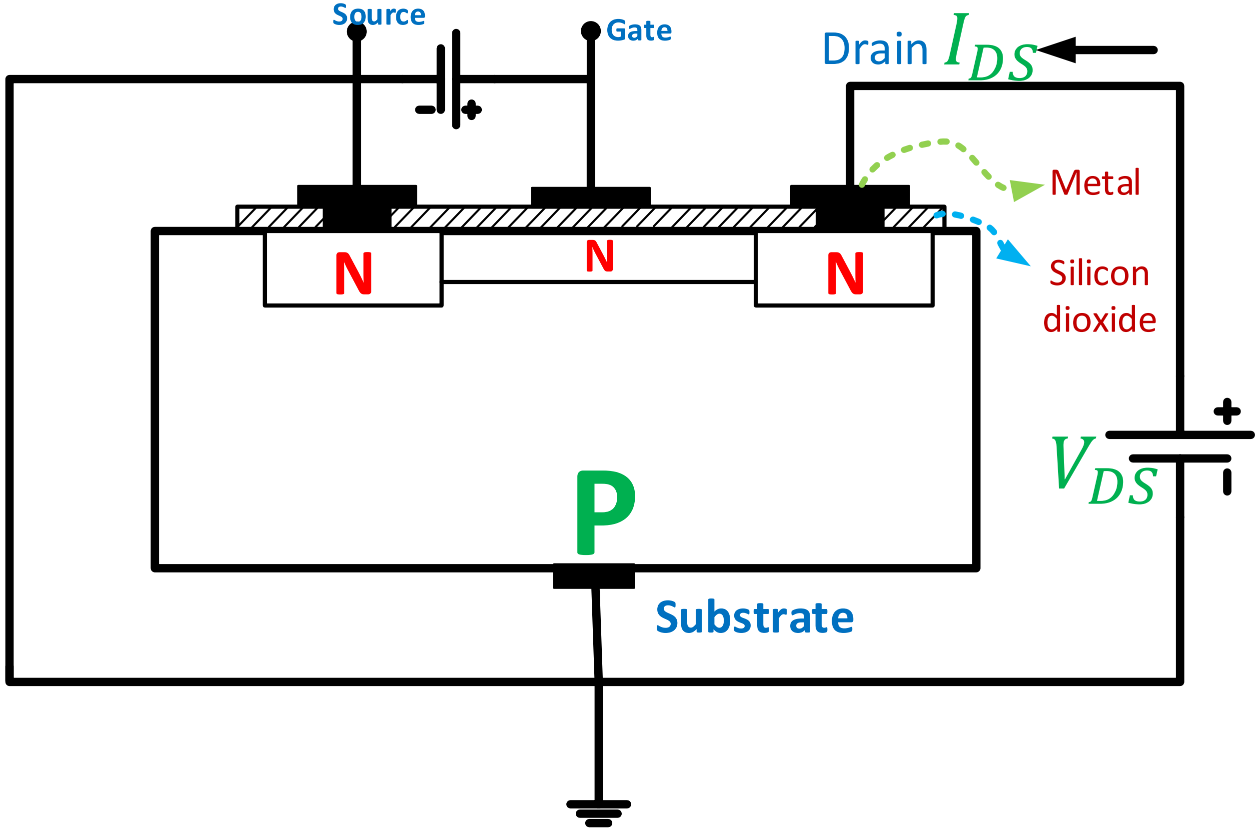
$\boldsymbol{V_{DS}} = -5.93$ V

Metal Oxide Semiconductor Field Effect Transistor MOSFET

- **1) Depletion type MOSFET: DMOSFET**
- **2) Enhancement type MOSFET: EMOSFET**
- **The MOSFET differs from the JFET in that it has no pn junction structure; instead, the gate of the MOSFET in insulated from the channel by a silicon dioxide (S_iO_2) large.**
- **Due to this the input resistance of MOSFET is greater than JFET.**

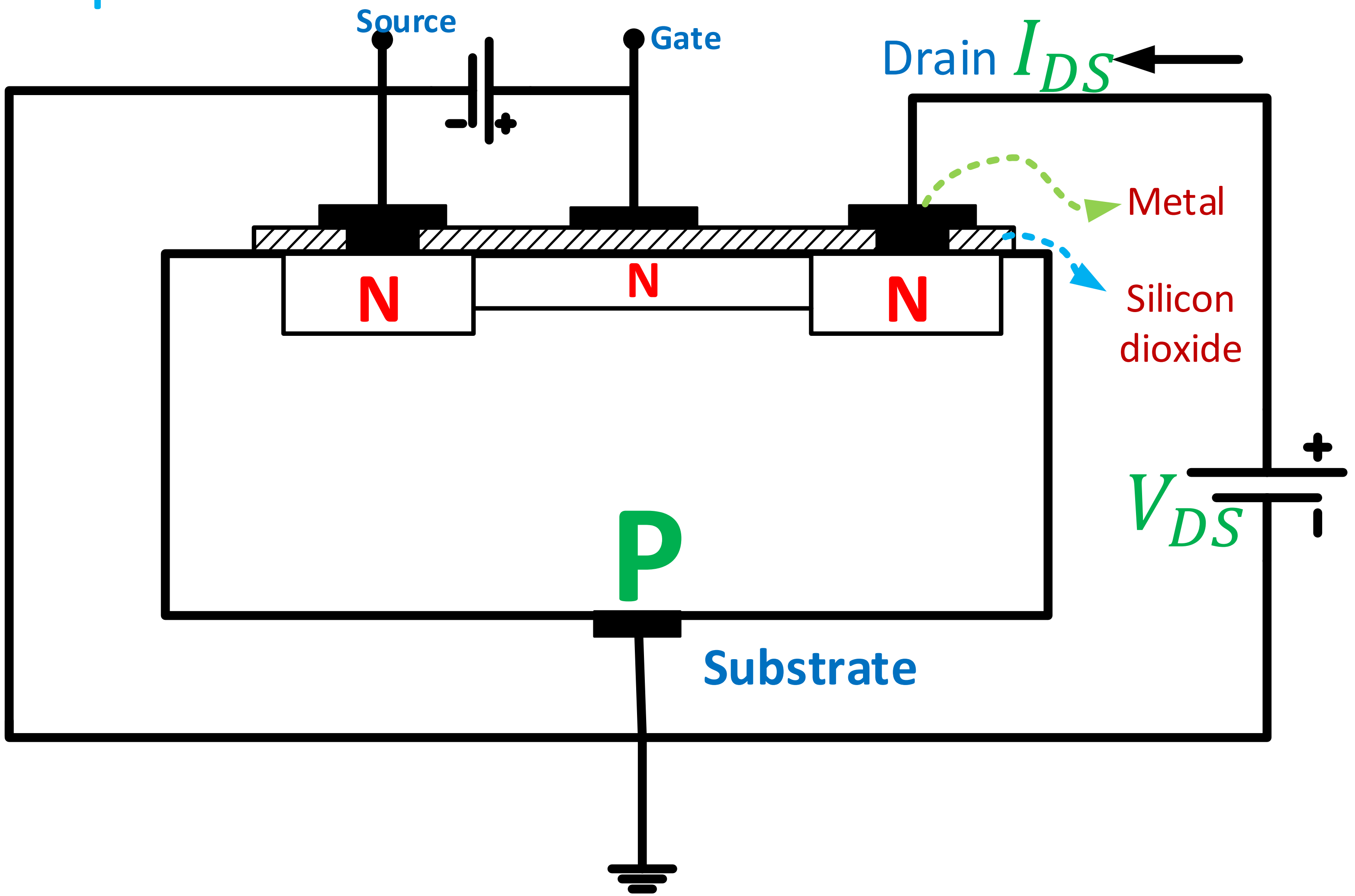
Depletion type MOSFET:

- **Construction of n-channel DMOSFET:**

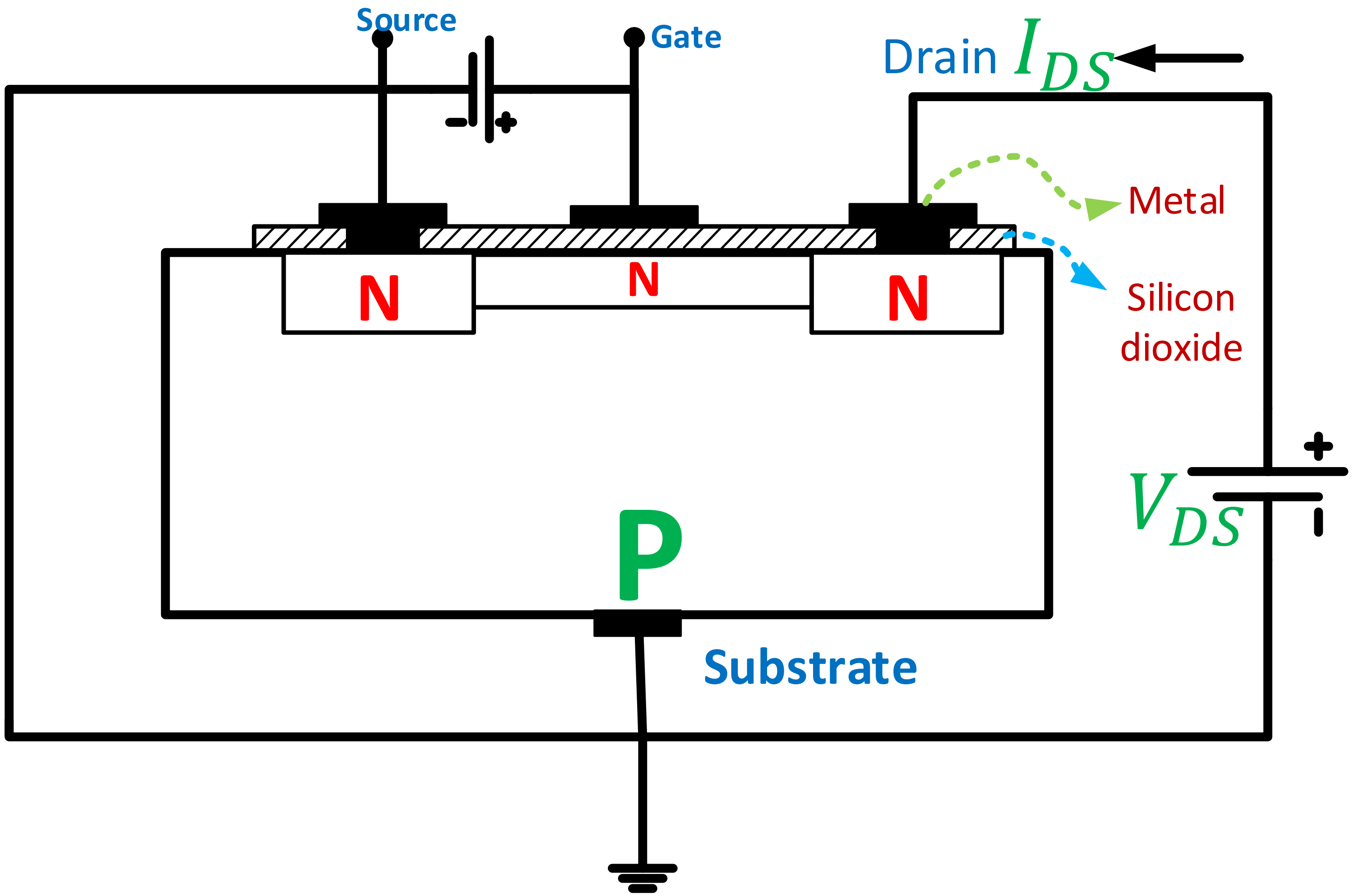


Operation , characteristic and parameters of DMOSFET

♦ **n-channel DMOSFET**



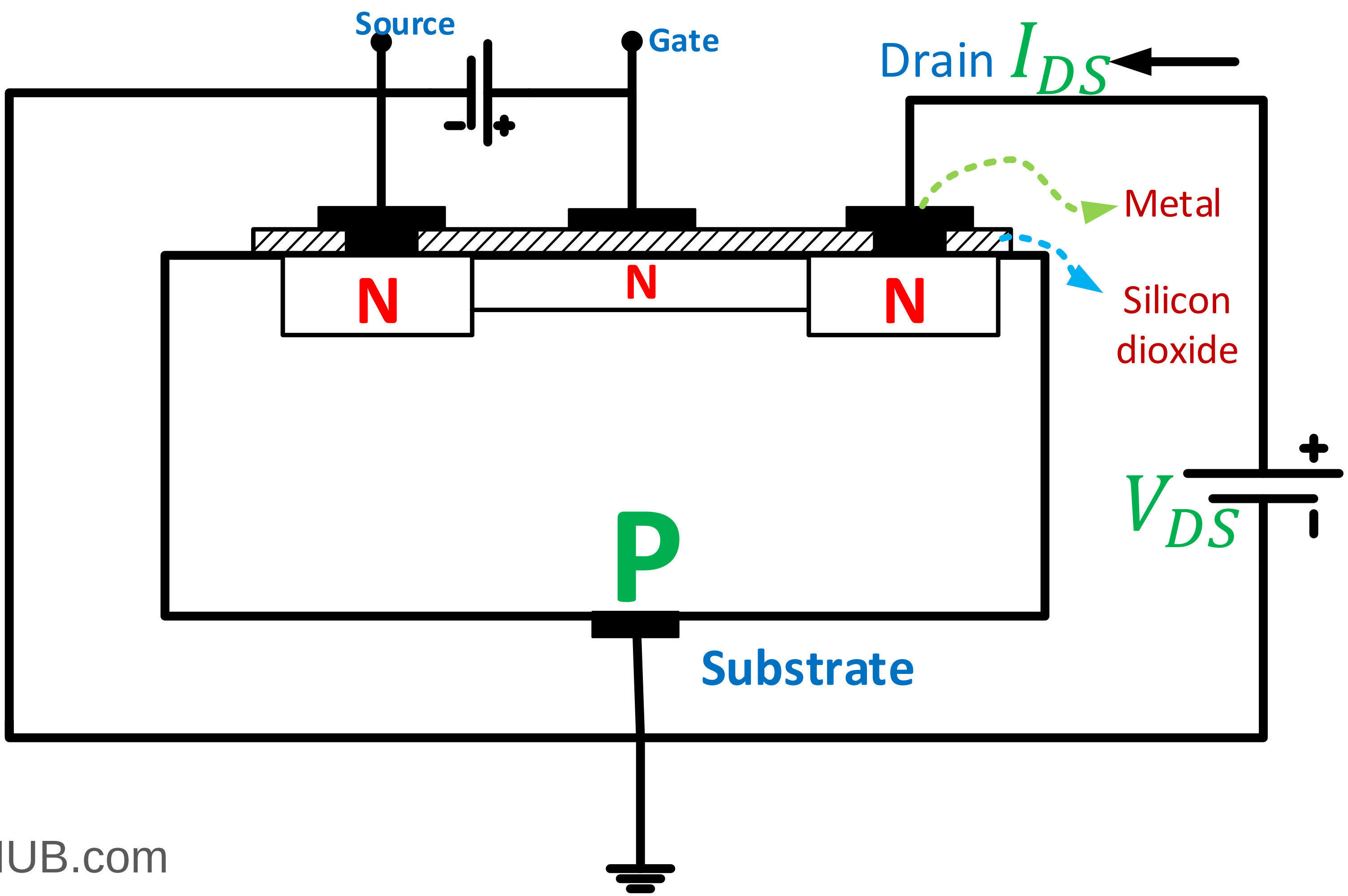
- **On the application of V_{DS} and keeping V_{GS} = 0 electrons from the n-channel are attracted towards positive potential of the drain terminal .**
- **This establishes current through the channel to be denotes as I_{DSS} at V_{GS} = 0 .**

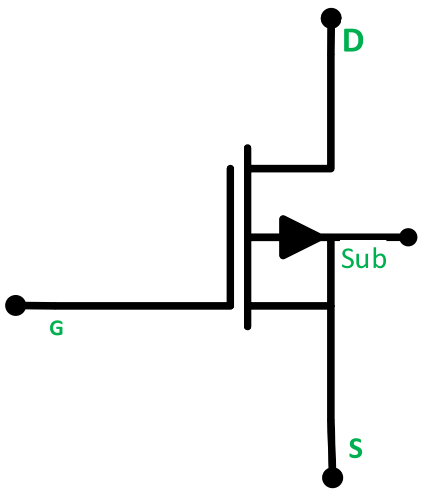


- If we apply negative gate voltage $(V_{GS} < 0)$ the negative charge on the gate repel electrons from the channel . The number of repelled electrons depends on the magnitude of the negative voltage V_{GS}.

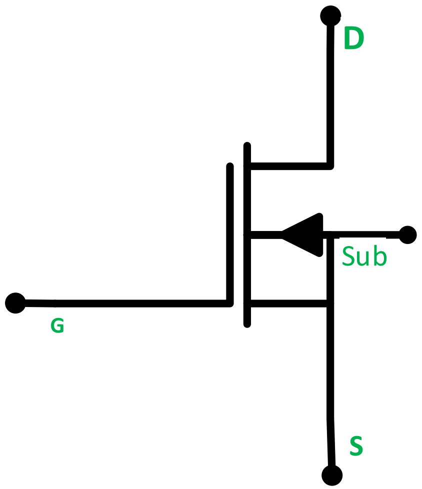
- The grater the negative voltage applied at the gate , the level of drain current will reduces until it reaches zero ; $V_{GS} = V_P$.

- For positive value of V_{GS}, the positive gate will draw additional electrons from the p-type substrate and the drain current increases .



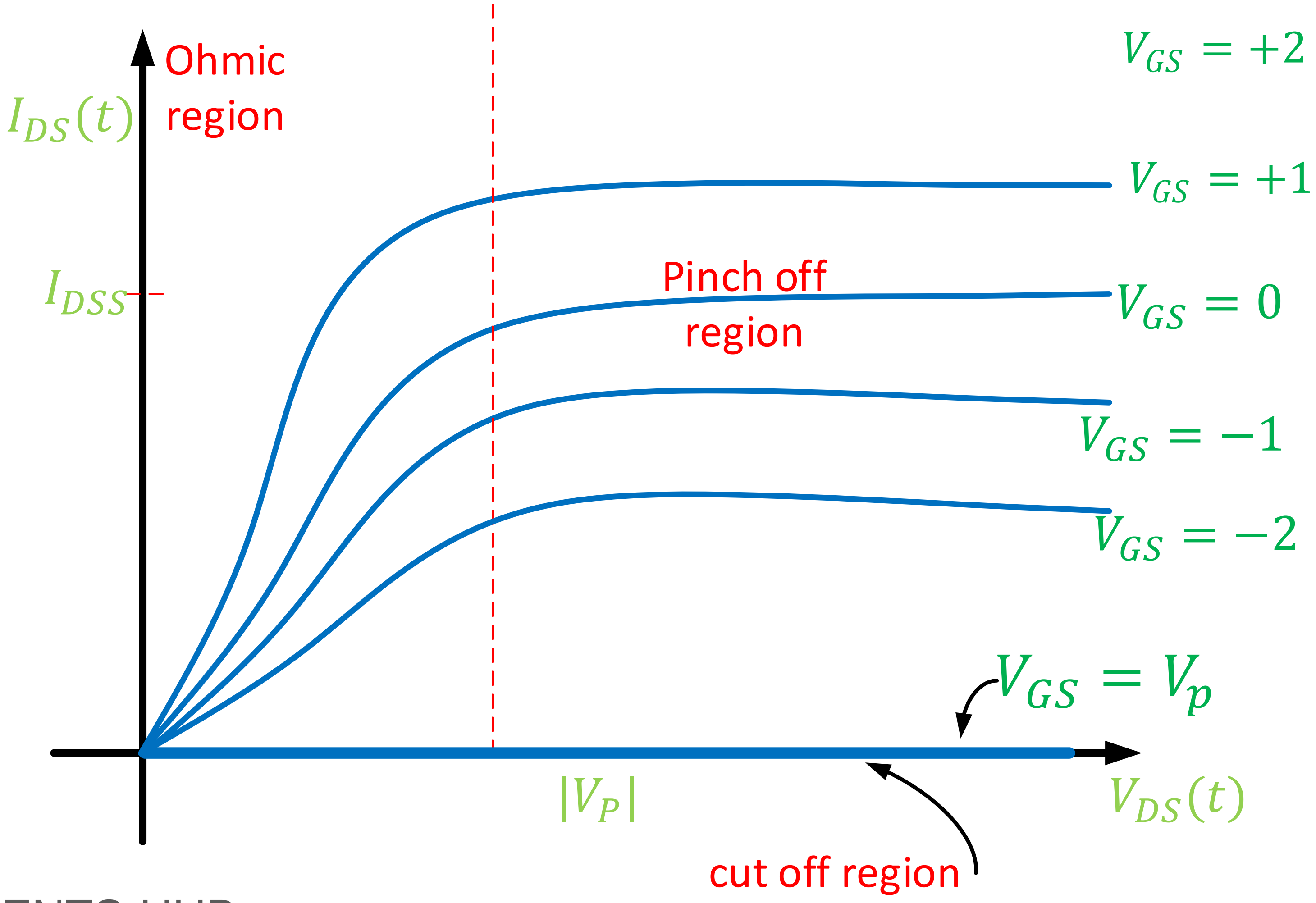


P-channel
DMOSFET

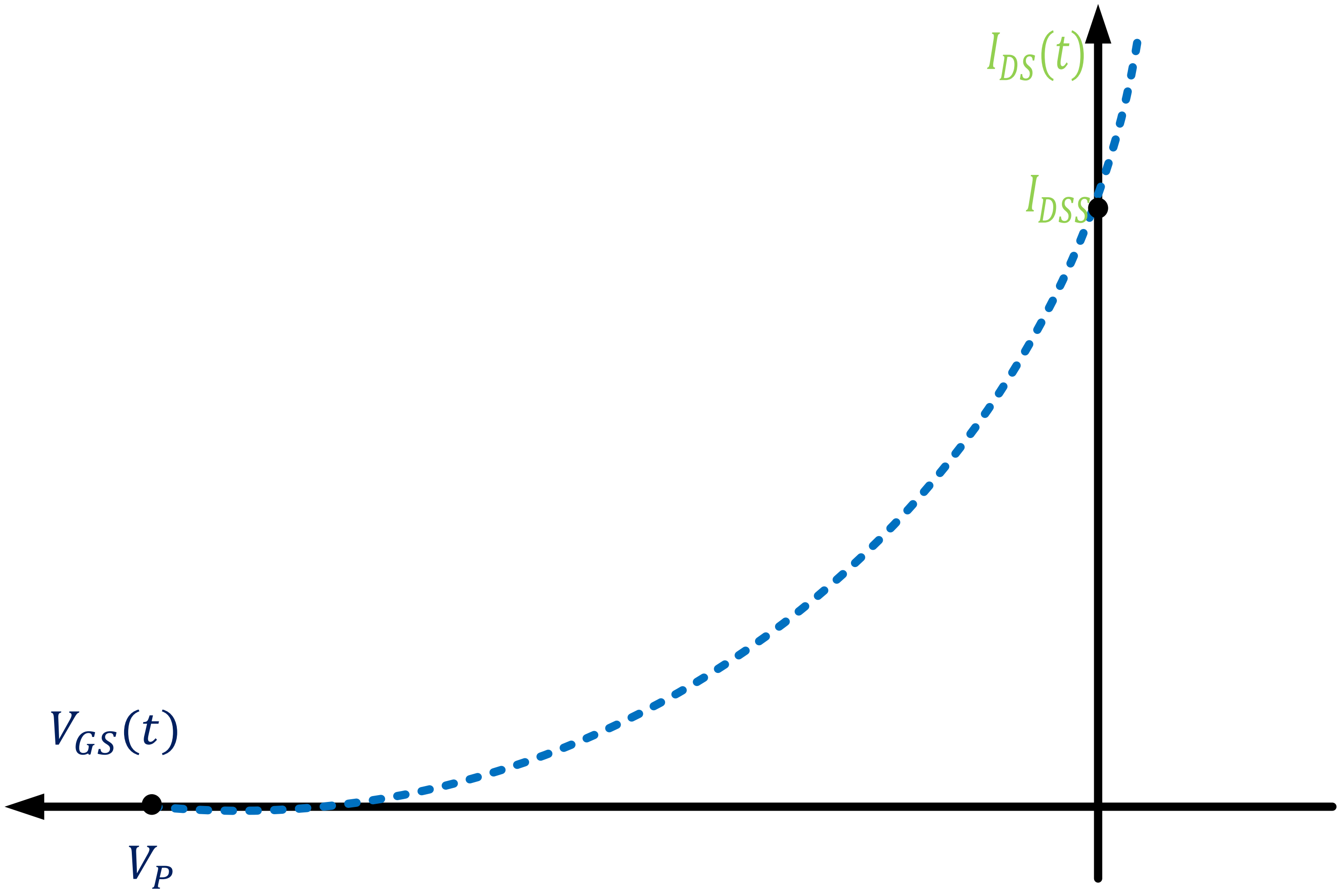


n-channel
DMOSFET

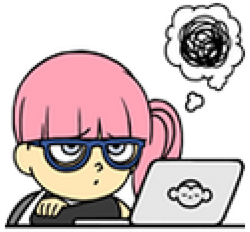
Drain characteristics for an n-channel DMOSFET



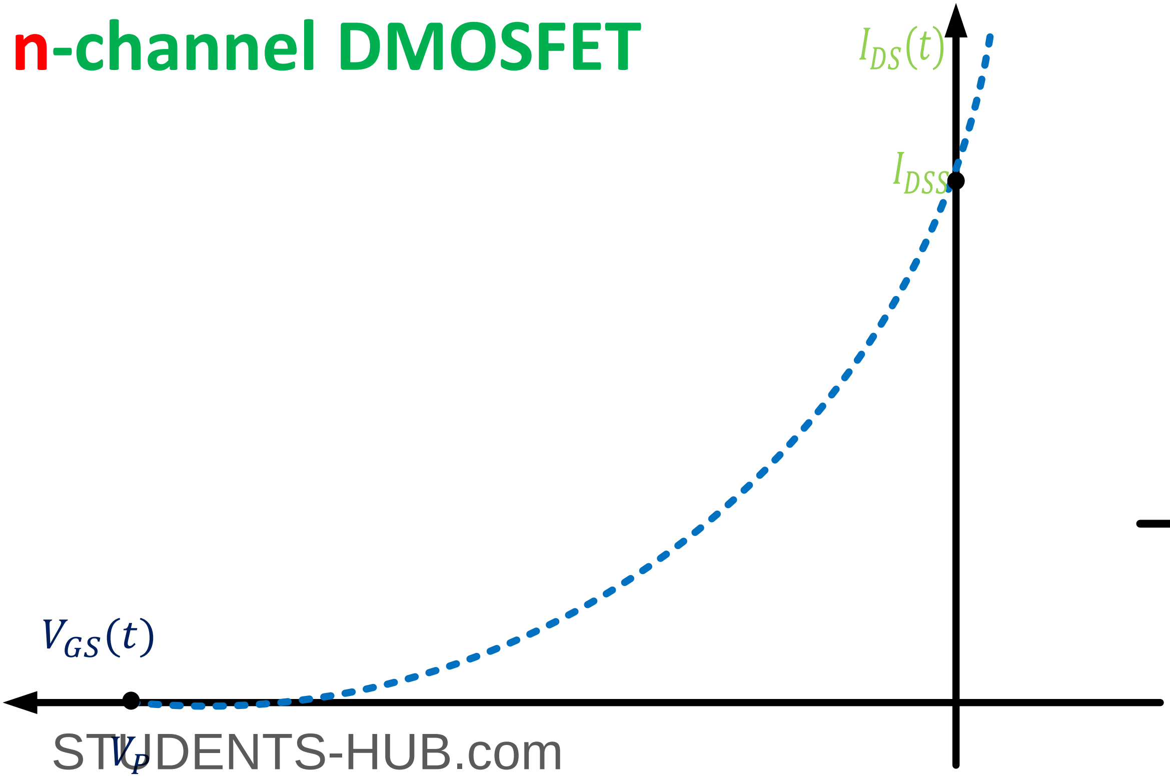
Transfer characteristics for an n-channel DMOSFET

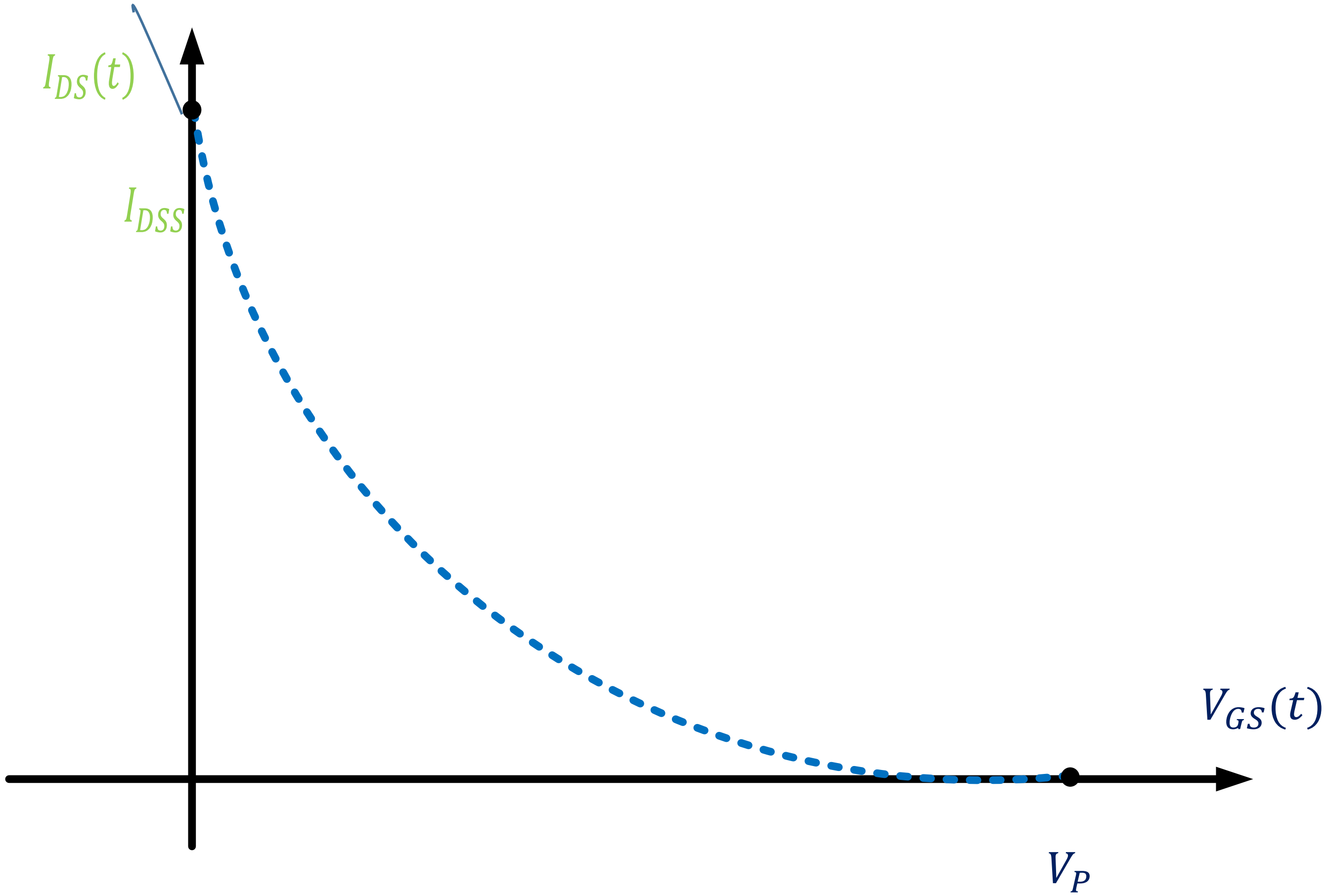


Transfer characteristics for an p-channel DMOSFET



n-channel DMOSFET





In the pinch off region

$$i_{DS}(t) = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

♦ For the n- channel

$V_{GS} > V_P$ (negative)

$V_{DS} > V_{GS} - V_P$

♦ For the p- channel

$V_{GS} < V_P$ (positive)

$V_{DS} < V_{GS} - V_P$

Example

Suppose that the DMOSFET is in the pinch off region

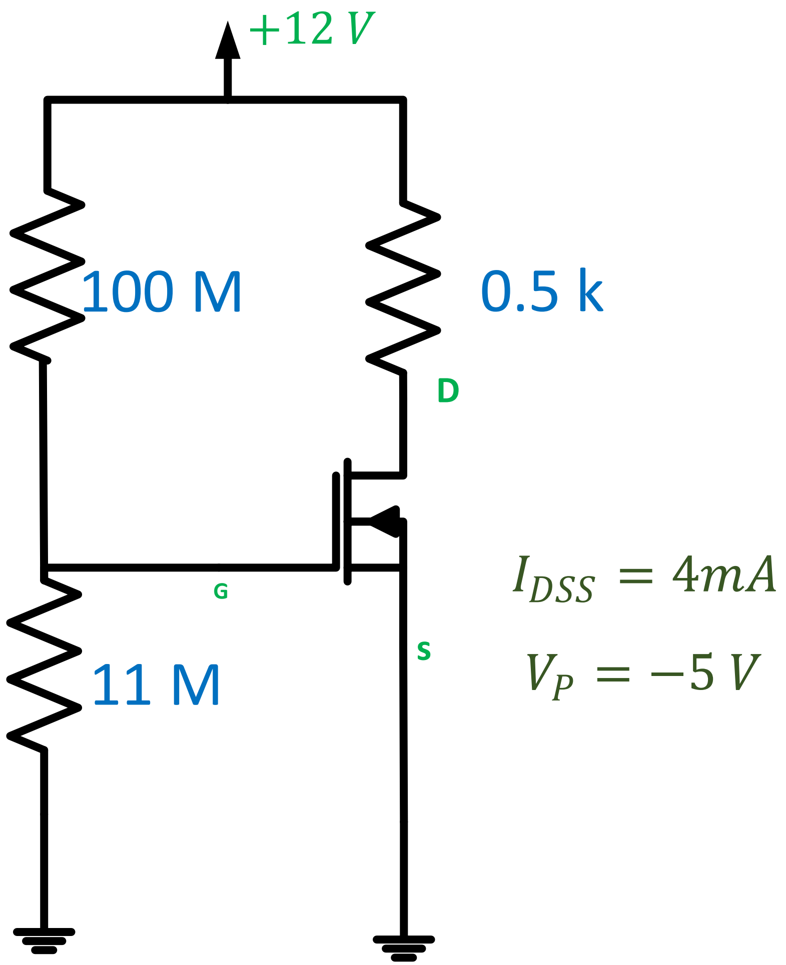
$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \text{............1}$$

$$V_{GS} = V_G - V_S = V_G$$

$$V_G = \frac{11M}{11M+100M}(12) = 1.19\text{ V} \quad \text{...........2}$$

sub 2 into 1 , we obtain

$$I_{DS} = 6.13\text{mA} > I_{DSS} \quad !!$$

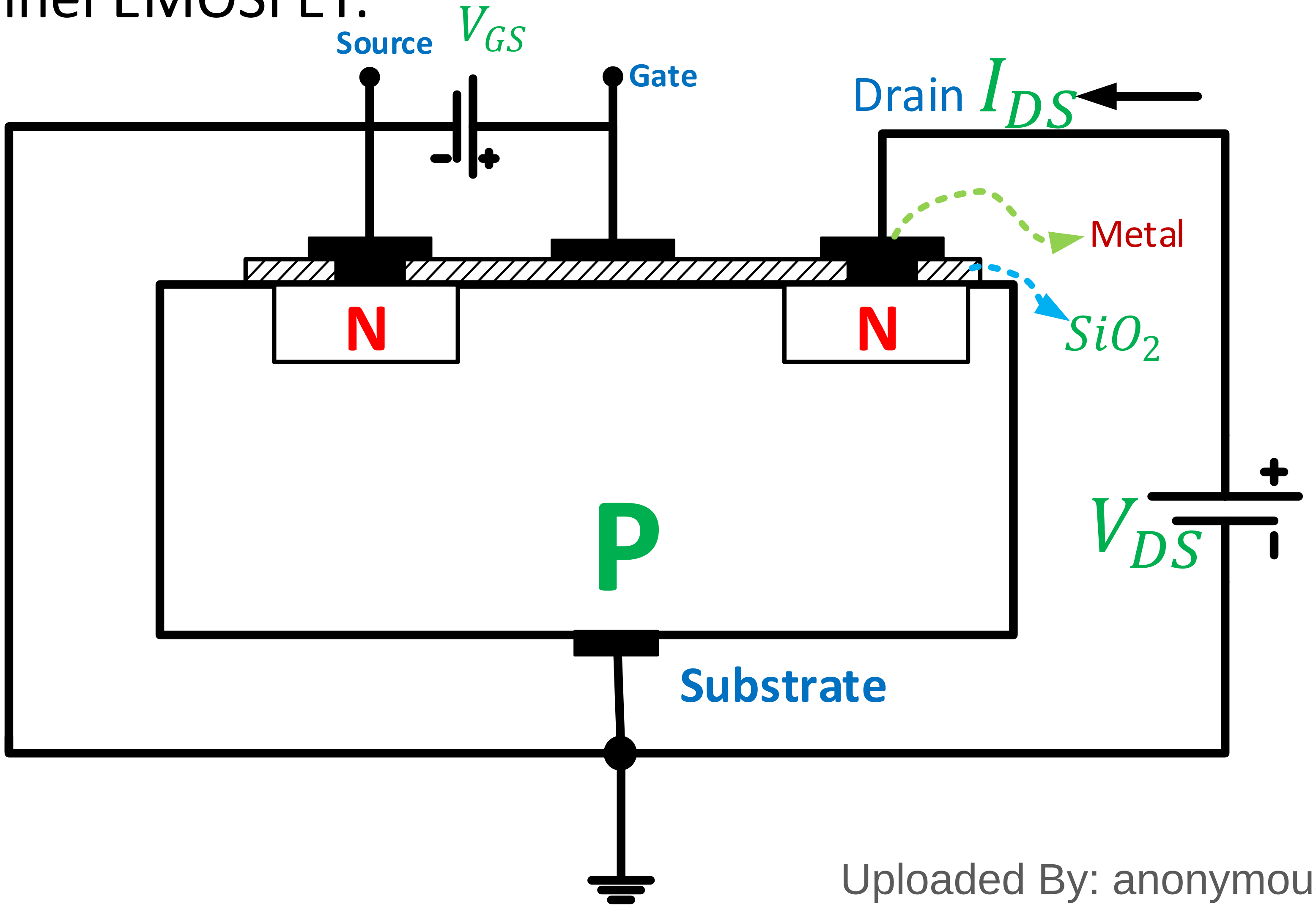


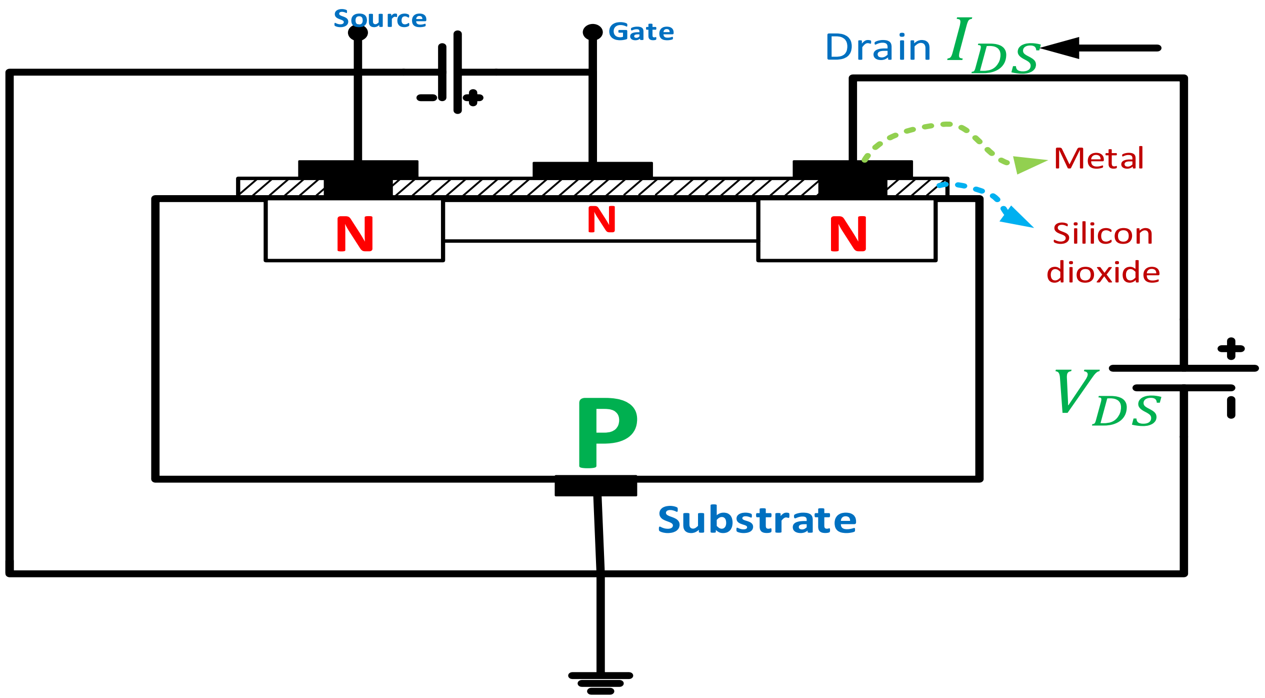
$$V_{DS} = V_{DD} - 0.5K\ I_{DS} = 8.93\text{ V}$$

$$V_{DS} \overset{?}{>} V_{GS} - V_P = 6.19\text{ V}$$

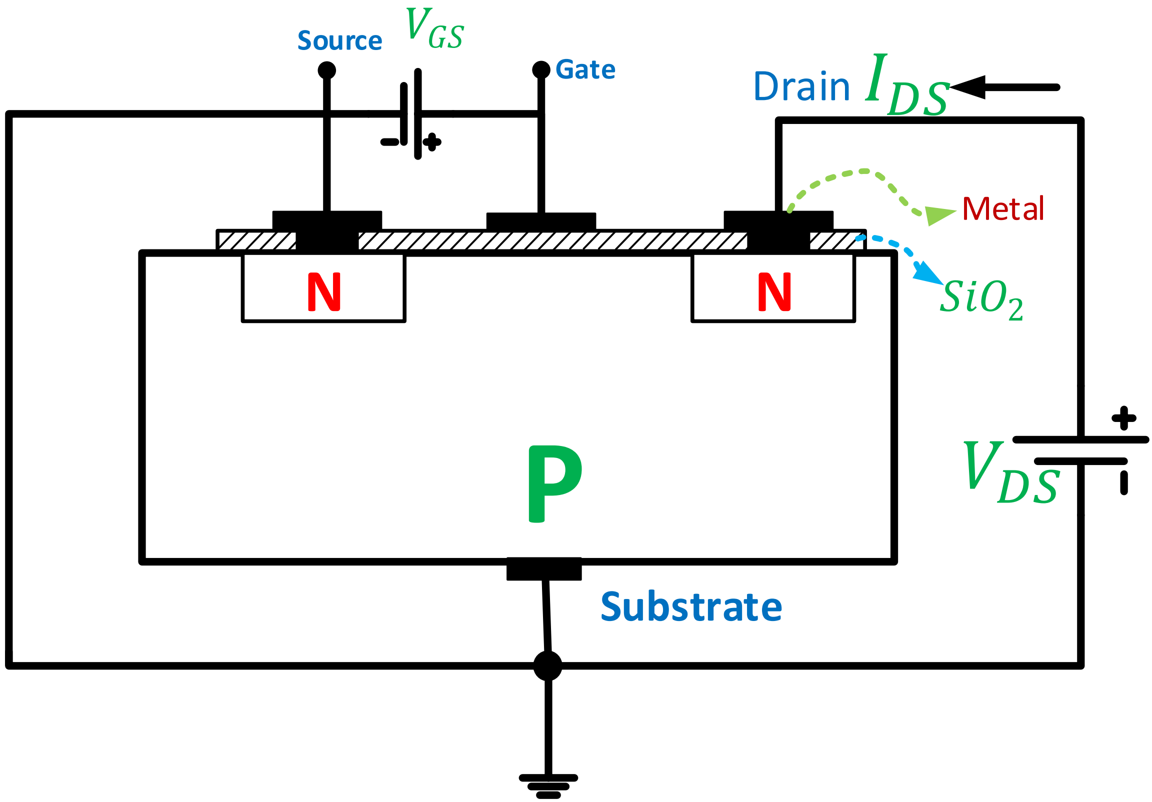
Enhancement type MOSFET

- Construction of n-channel EMOSFET:





Construction of n-channel DMOSFET



Construction of n-channel EMOSFET

Operation , characteristic and parameters of EMOSFET

- **On the application of $V_{DS}$and keeping V_{GS}=0 practically zero current flows .**

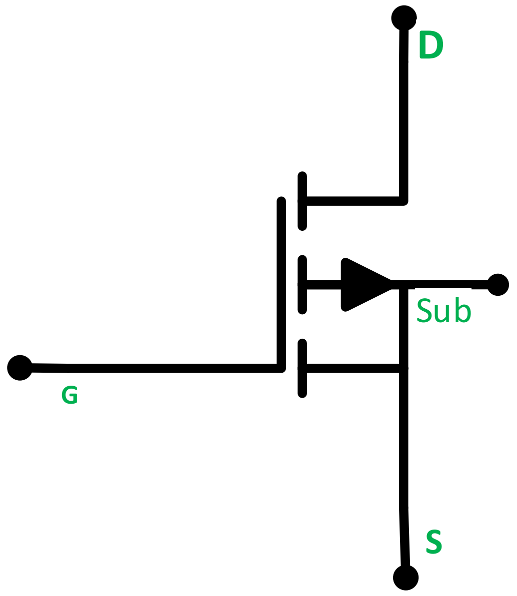
- **If we increase V_{GS} in the positive direction the concentration of electrons near the SiO_2 surface increases ,**

- **At particular value of V_{GS} there is a measurable current flow between drain and source ; I_{DS} .**

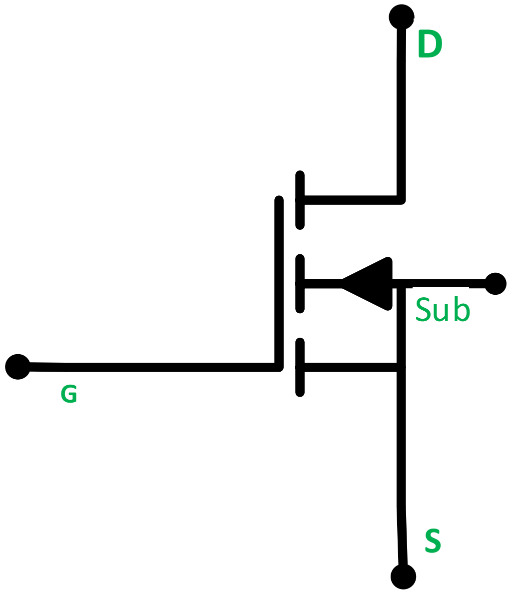
- **This value of V_{GS} is called threshold voltage denoted by V_T**

- **A positive V_{GS} above V_T induce a channel and hence the drain current (I_{DS}) by creating a thin layer of negative charges (electrons) in the substrait adjacent to the SiO_2 large .**

The conductivity of the channel is enhanced by increasing V_{GS} and thus pulling more electrons into the channel .

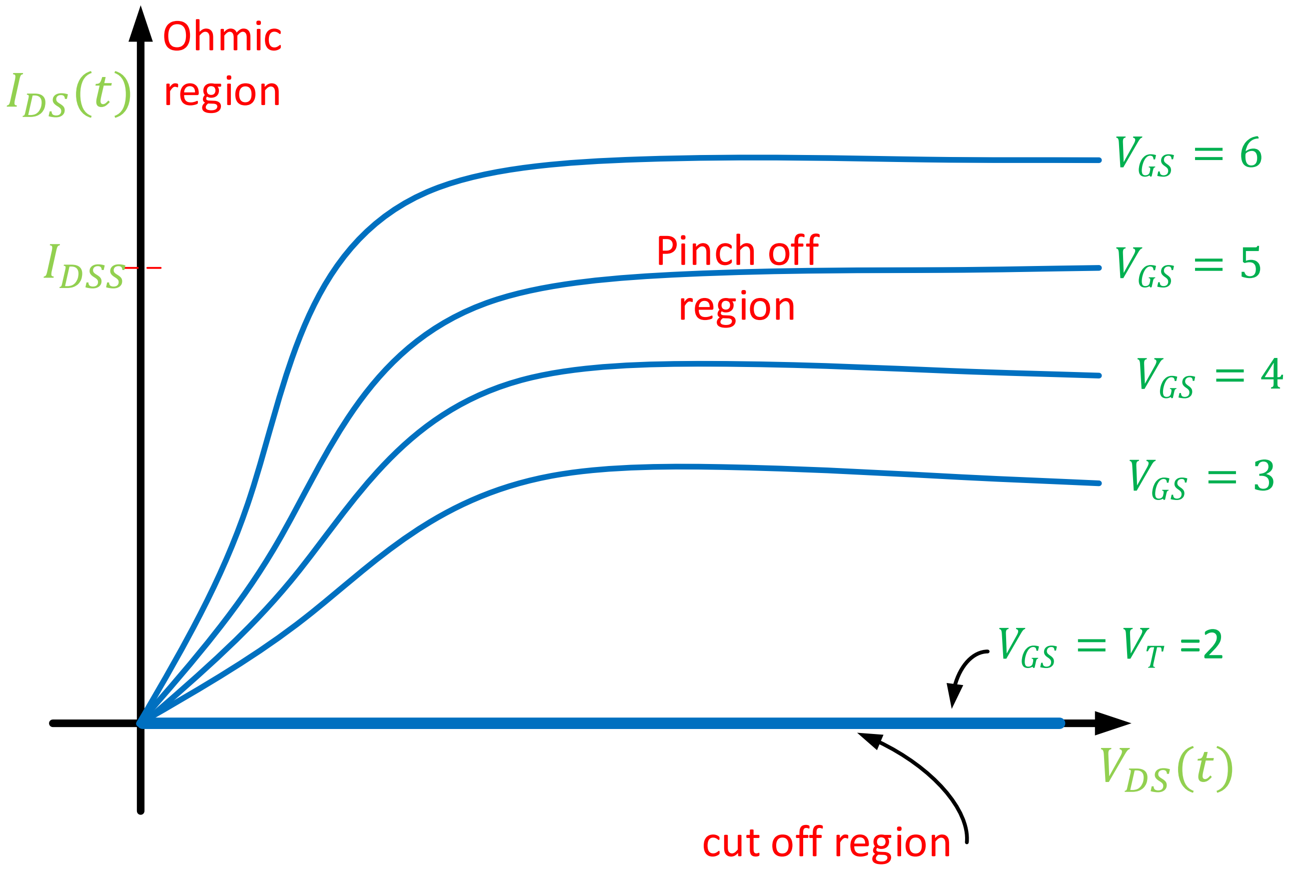


P-channel
EMOSFET

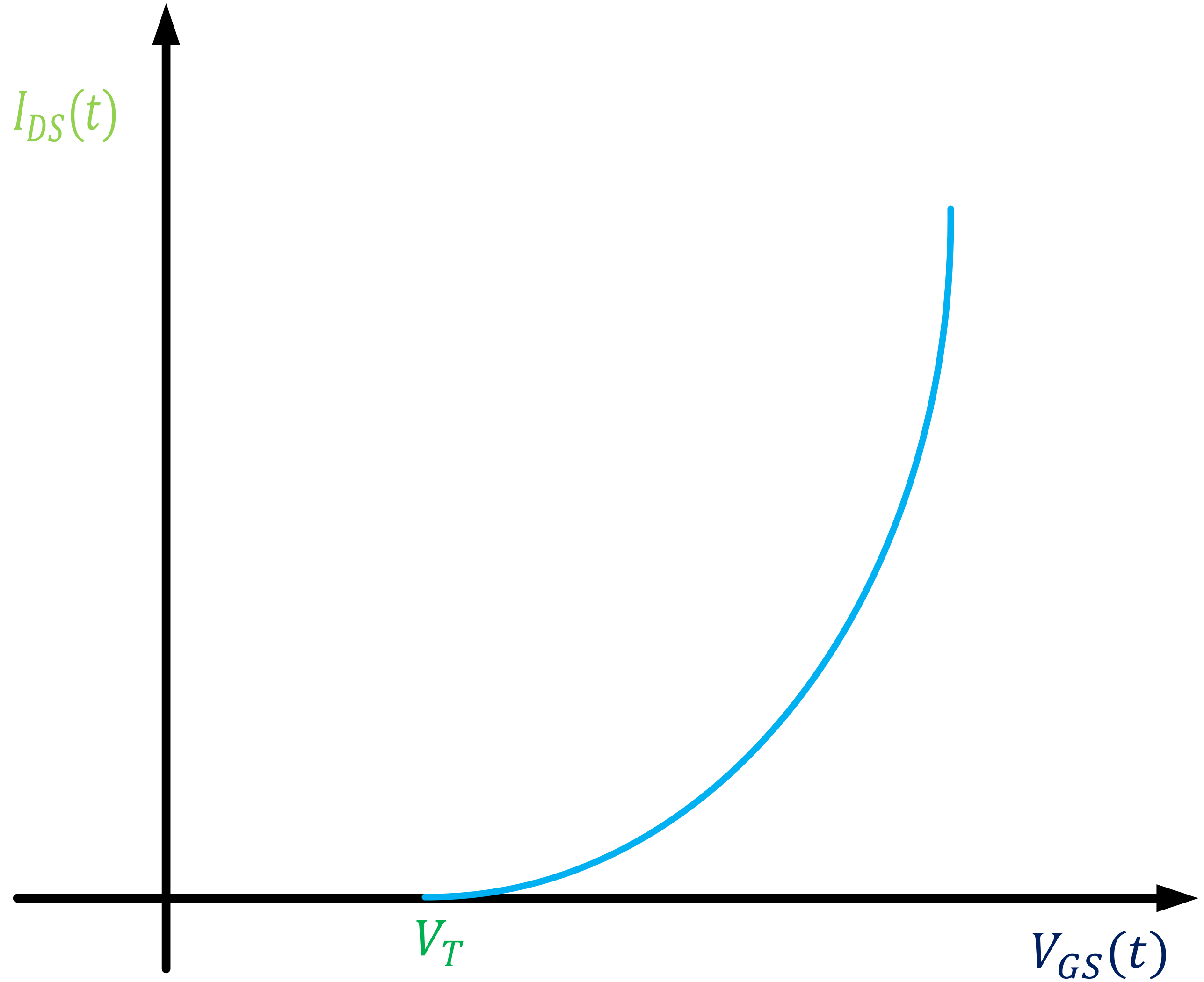


n-channel
EMOSFET

Drain characteristics for an n-channel EMOSFET

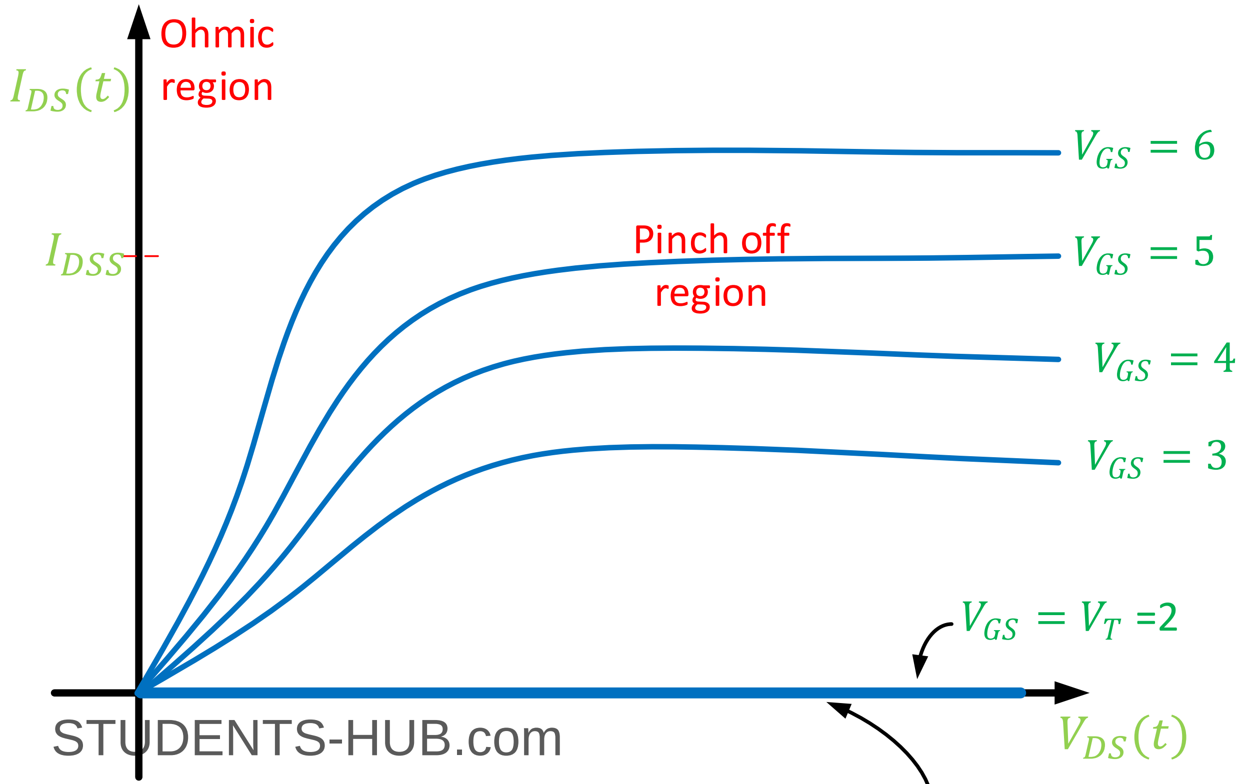


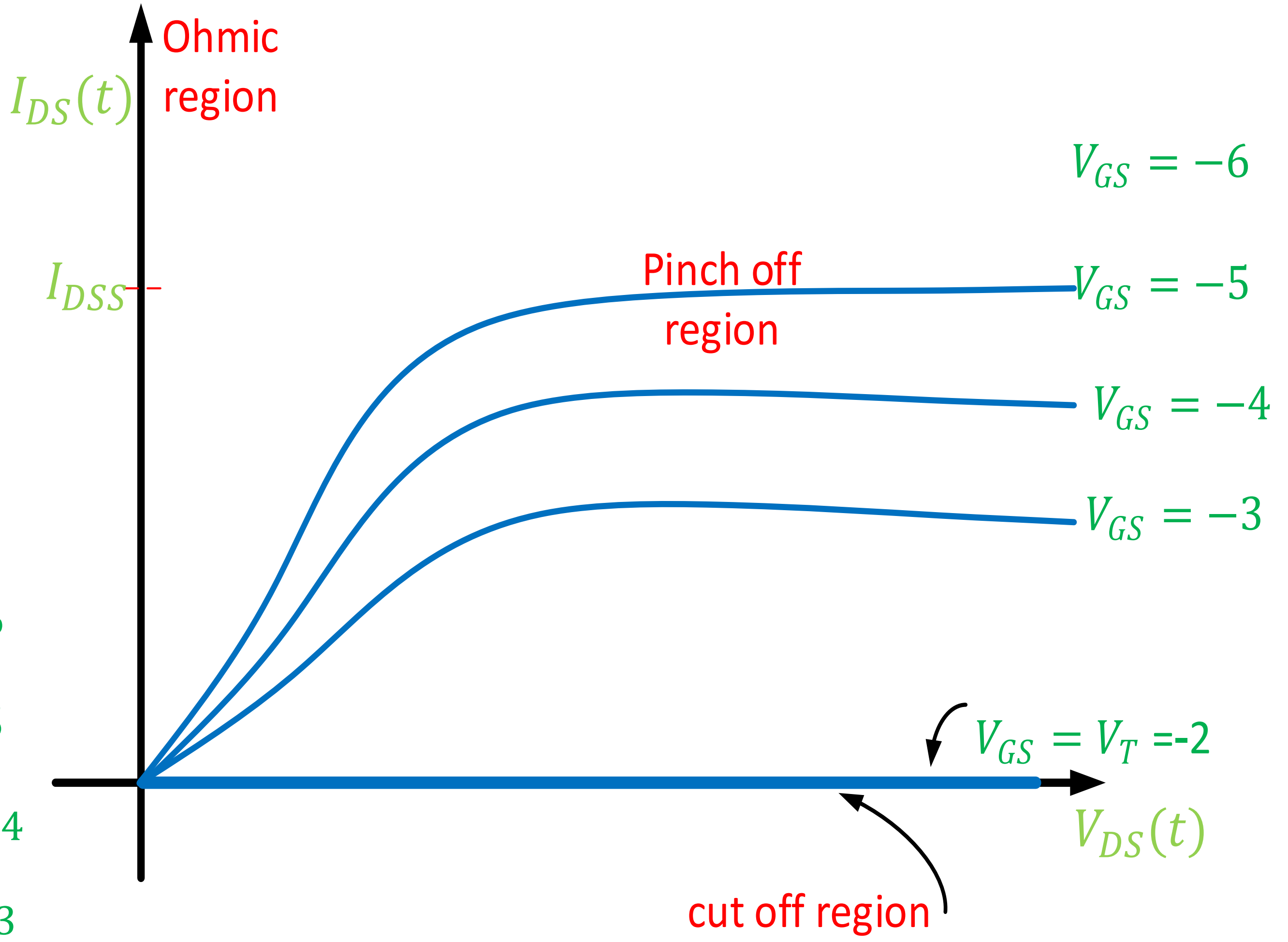
Transfer characteristics for an n-channel EMOSFET



Drain characteristics for an p-channel EMOSFET

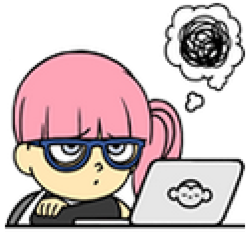
n-channel

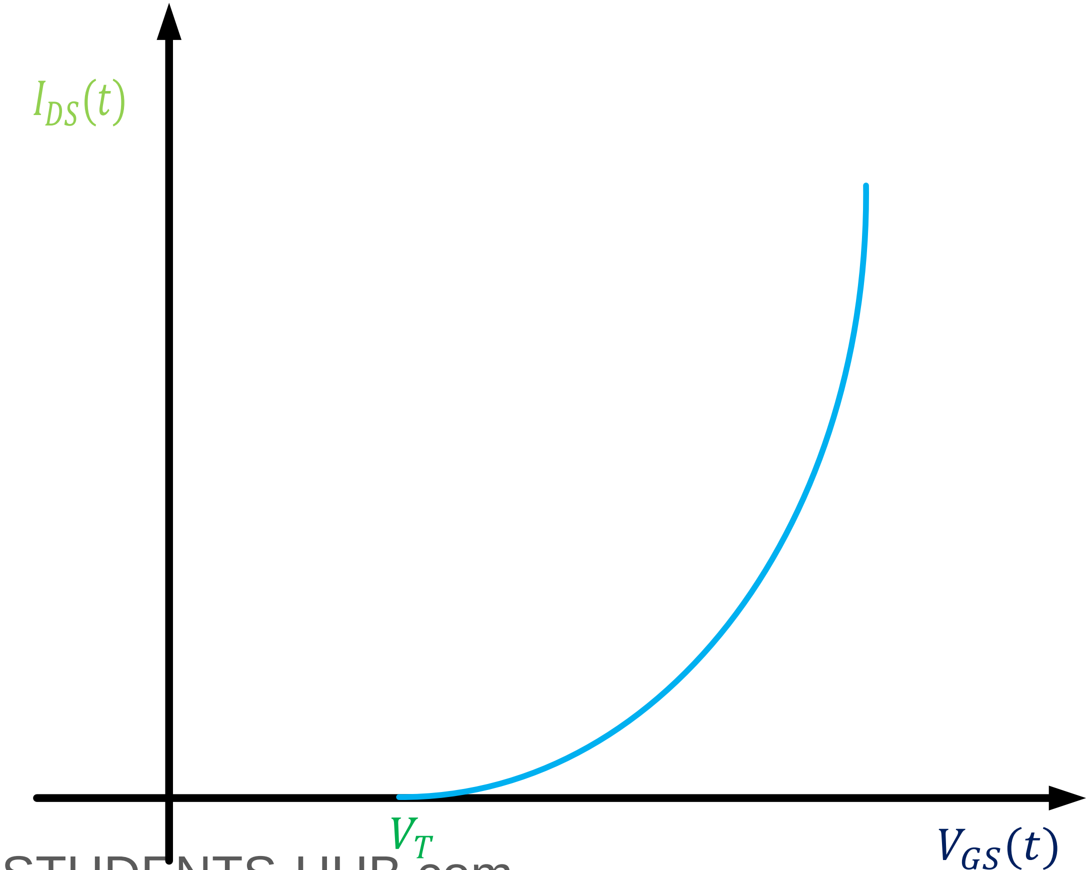


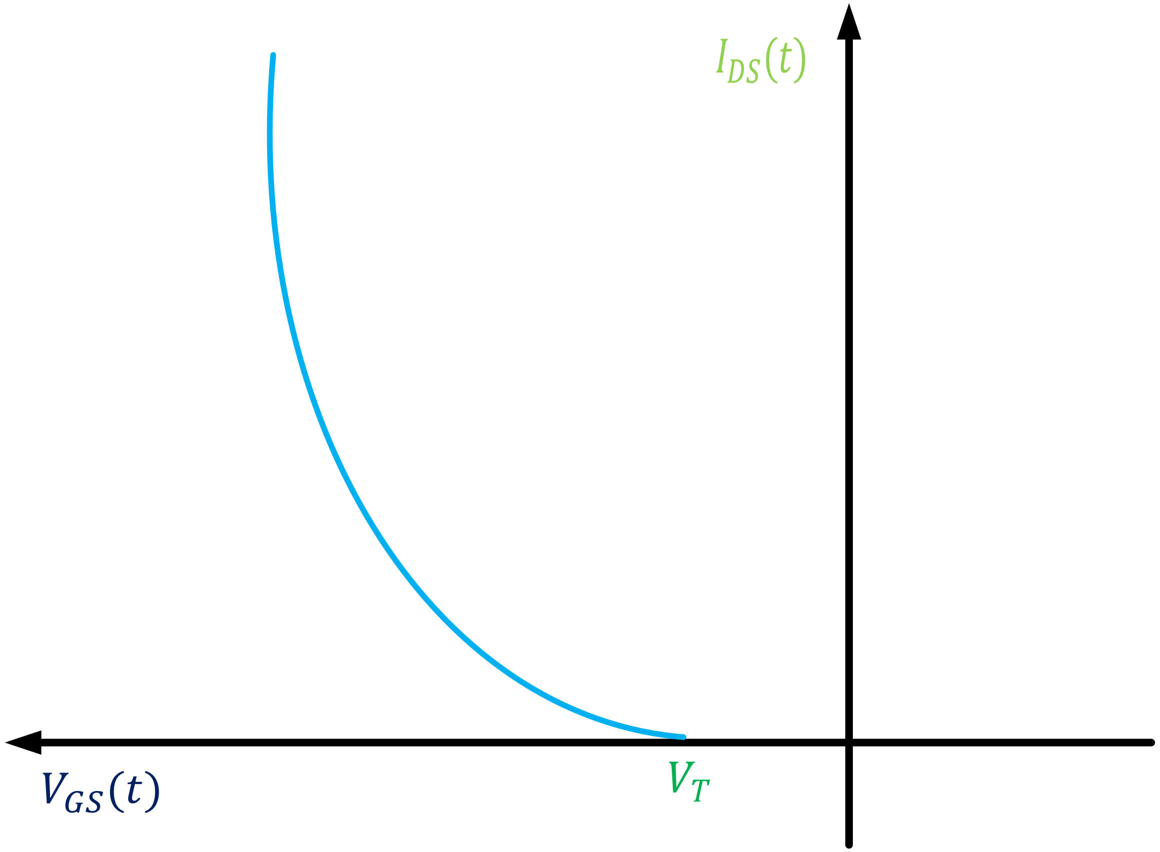


Transfer characteristics for an p-channel EMOSFET

n-channel







In the pinch off region

$$i_{DS}(t) = K_n(V_{GS}(t) - V_T)^{\,2}$$

$$K_n = \frac{1}{2} K`_n \frac{W}{L}$$

$$K`_n = \mu_n C_{ox}$$

$$|V_{DS}| > |V_{GS} - V_T|$$

$V_{GS}>V_T$; n- channel

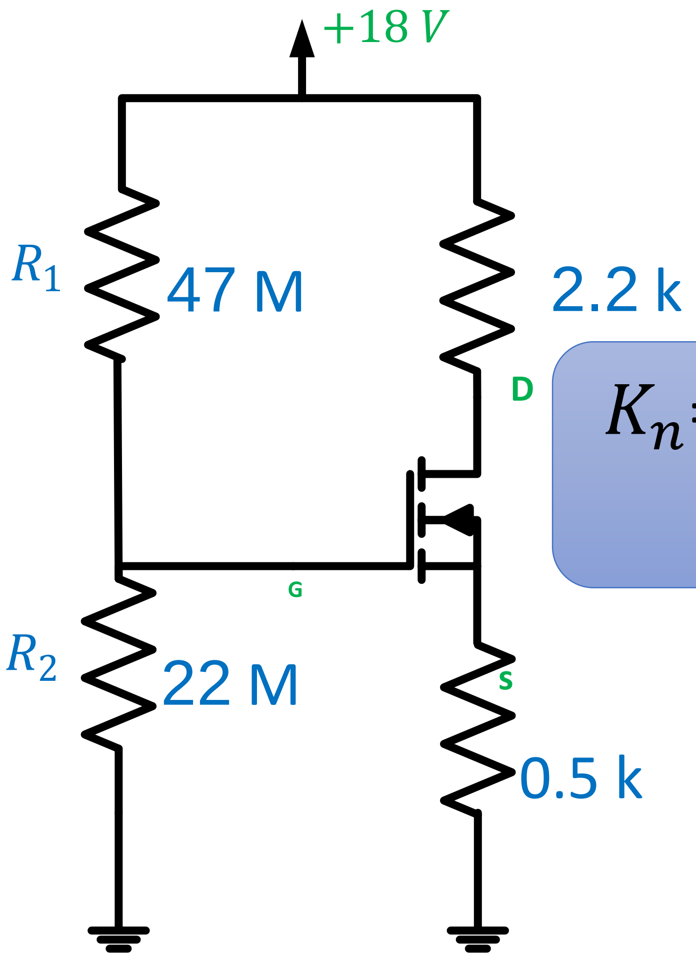
$V_{GS}<V_T$; p- channel

Example

$$I_{DS} = K_n(V_{GS} - V_T)^2 \text{ ....1}$$

$$V_{GS} = V_G - V_S$$

$$V_G = \frac{22M}{22M+47M}(18) = 5.74V$$



$K_n = 0.25X10^{-3} A/V^2$

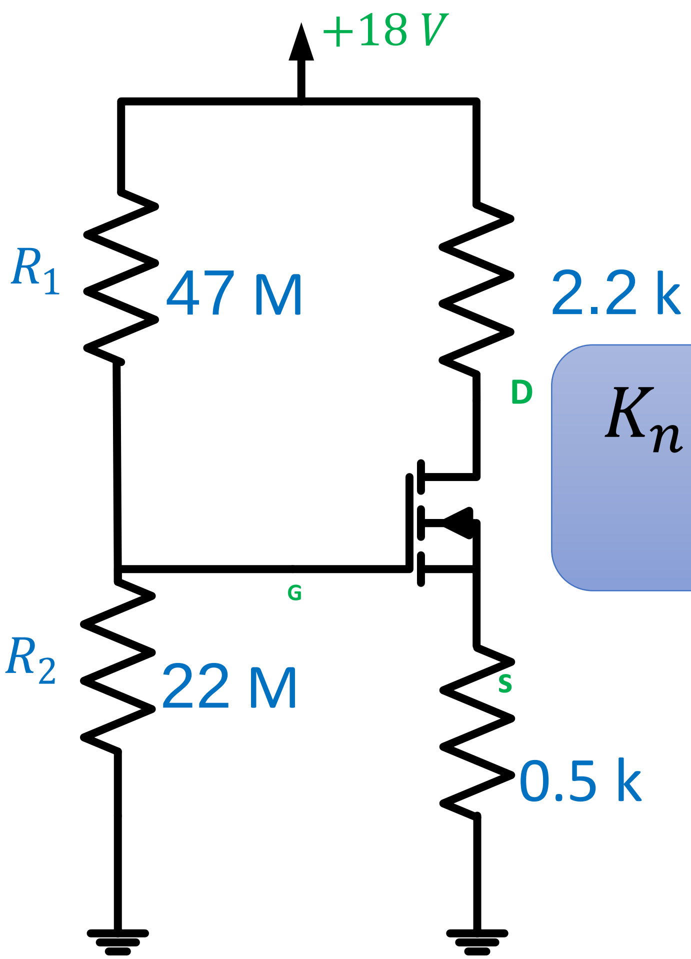
$V_T = 2$ V

V_S = (0.5K) I_{DS}

V_{GS} = 5.74 - (0.5K) I_{DS}............2

solving for V_{GS}:

V_{GS} = 4.78V √
= -8.78V X



K_n= 0.25X10^{-3} A/V^2
V_T = 2 V

I_{DS} =1.92m A

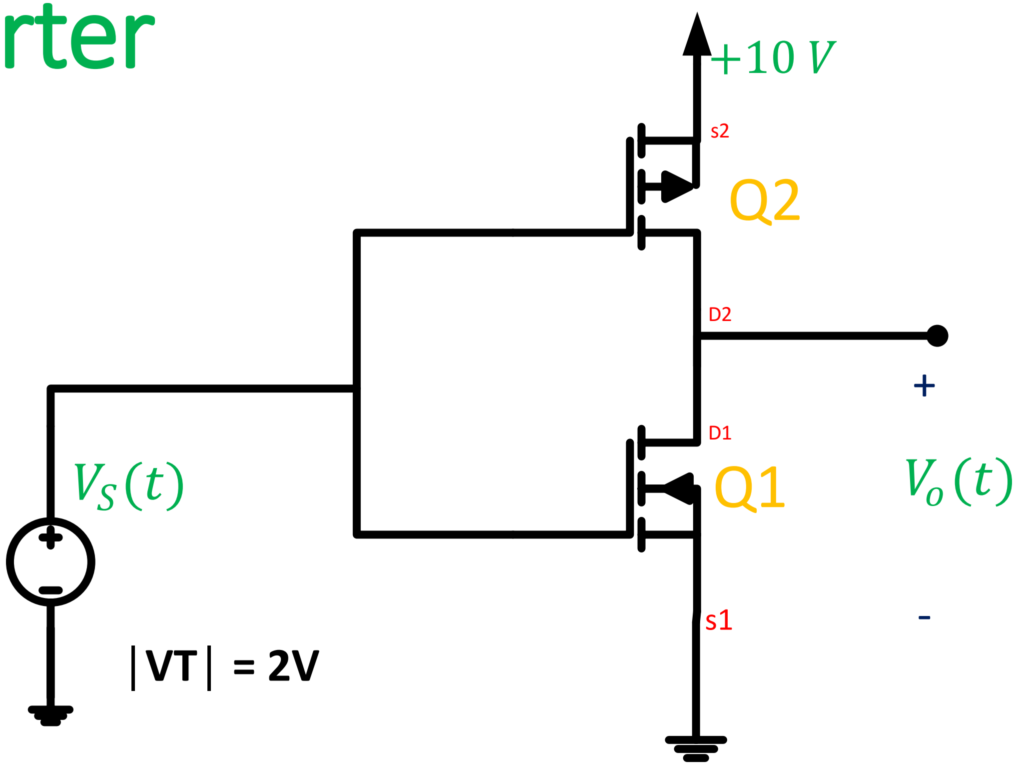
V_{DS} = 12.82 $> |V_{GS} - V_T|$

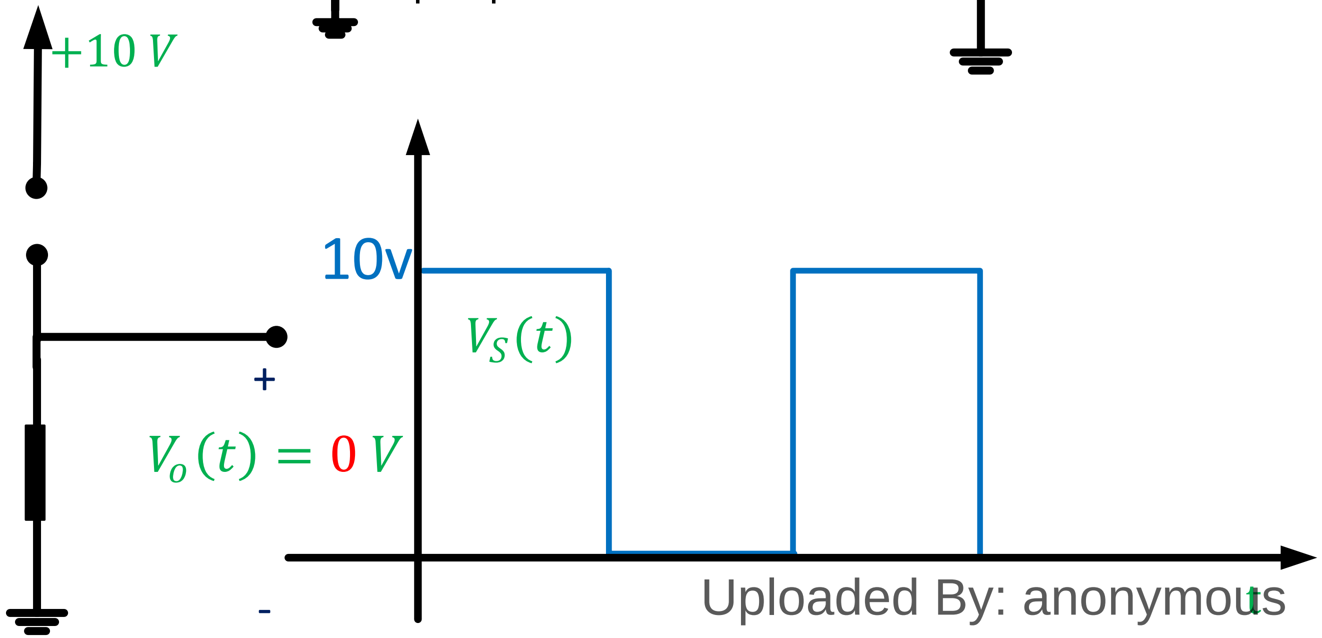
Complementary MOS (cmos) inverter

1) Let V_S(t) = 10 V

V_{GS1} = V_{G1} - V_{S1} = 10-0 = 10 V $> V_{T1}$

Q_1 is on , replaced with short circuit





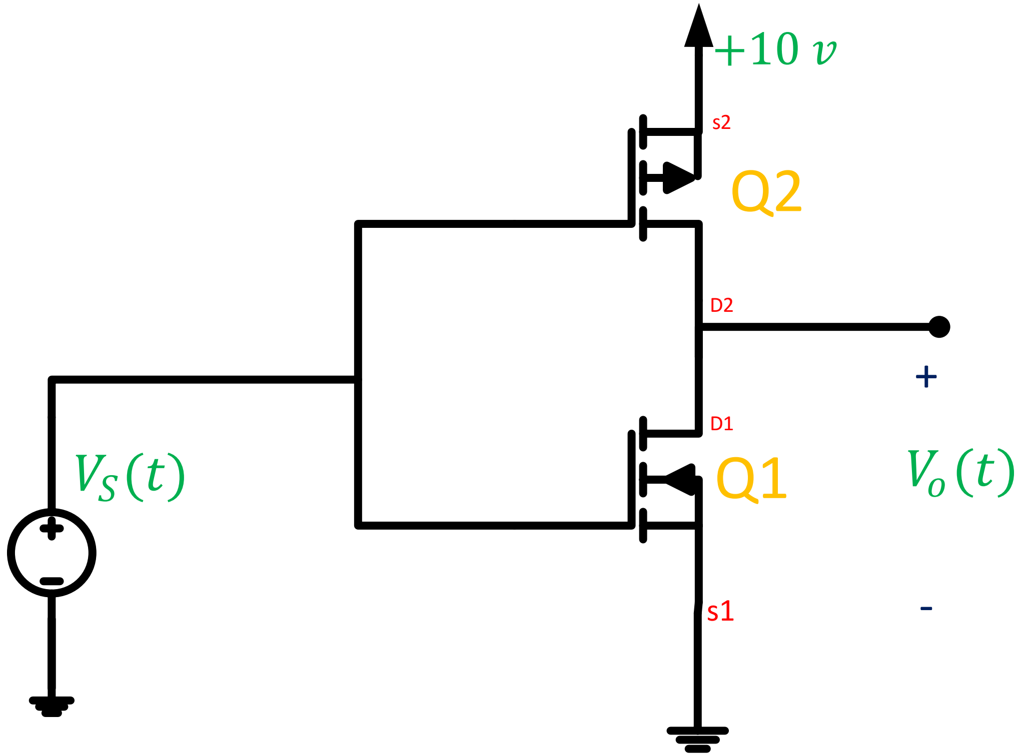
V_{GS2} = V_{G2} - V_{S2} = 10-10 = 0 V $> V_{T2}$

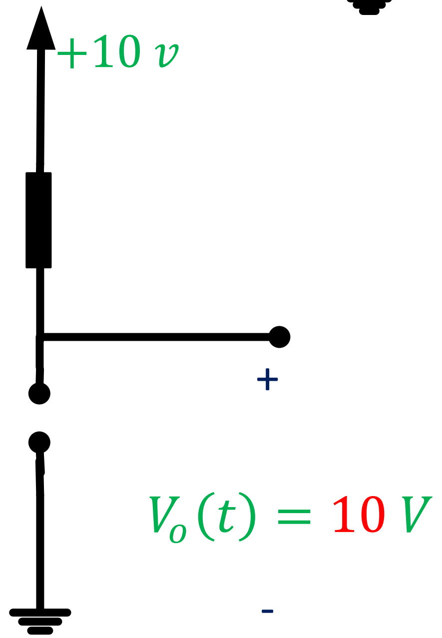
Q_2 is off , replaced with open circuit

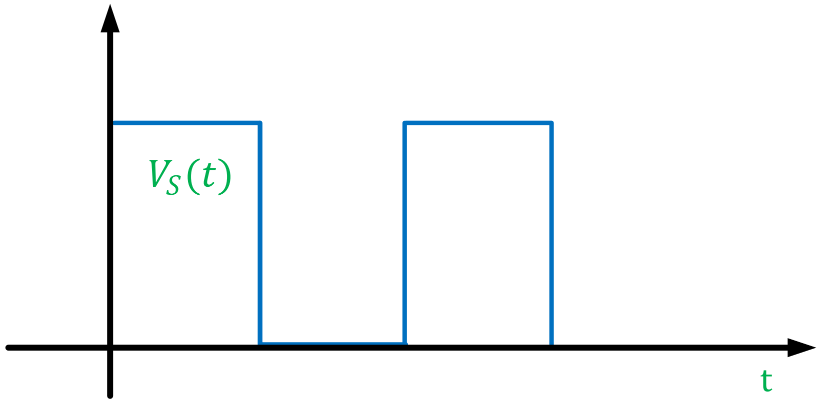
2) Let V_S(t) = 0 V

$V_{GS1} = V_{G1} - V_{S1} = 0 = 0\text{ V} < V_{T1}$

Q_1 is off , replaced with open circuit



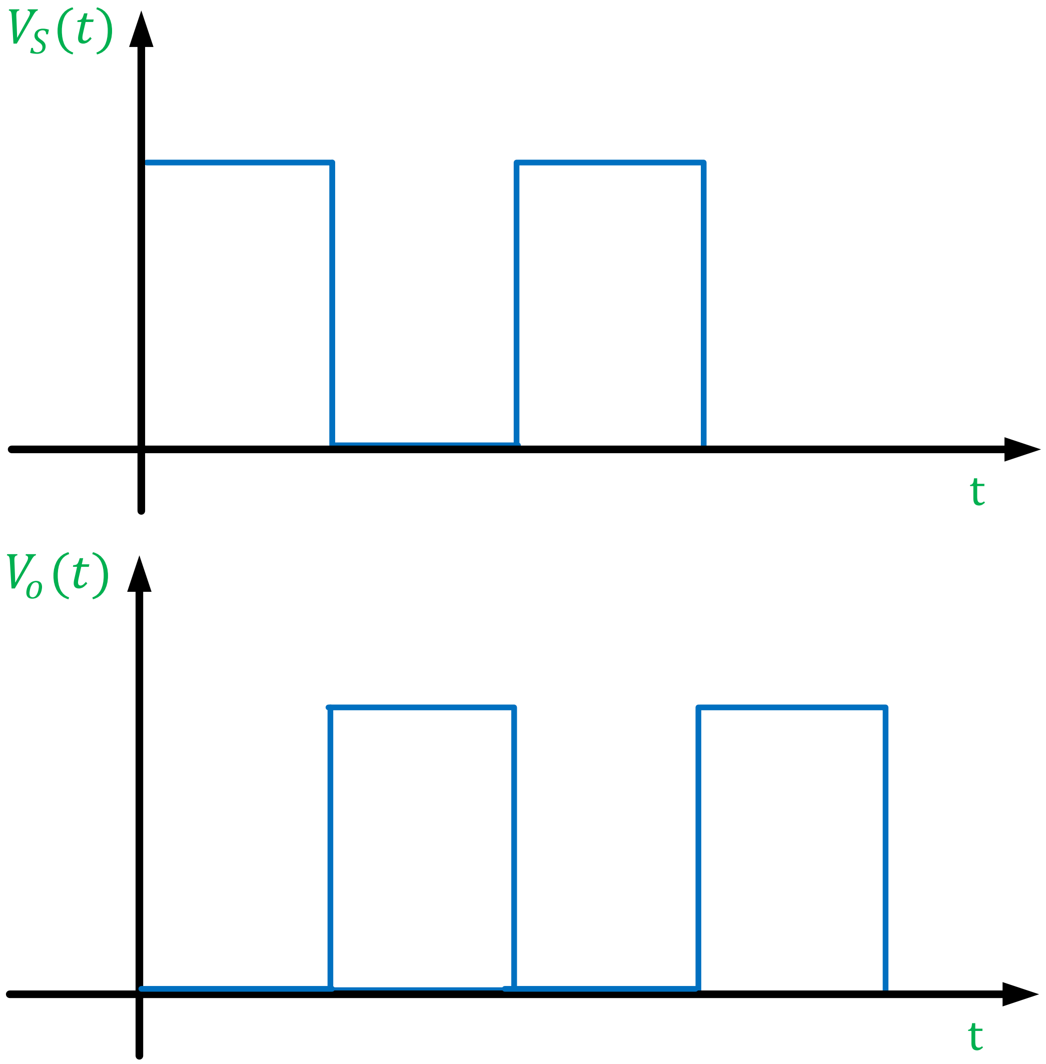




$V_{GS2} = V_{G2} - V_{S2} = 0\text{-}10 = -10\text{ V} < V_{T2}$

Q_2 is on , replaced with short circuit

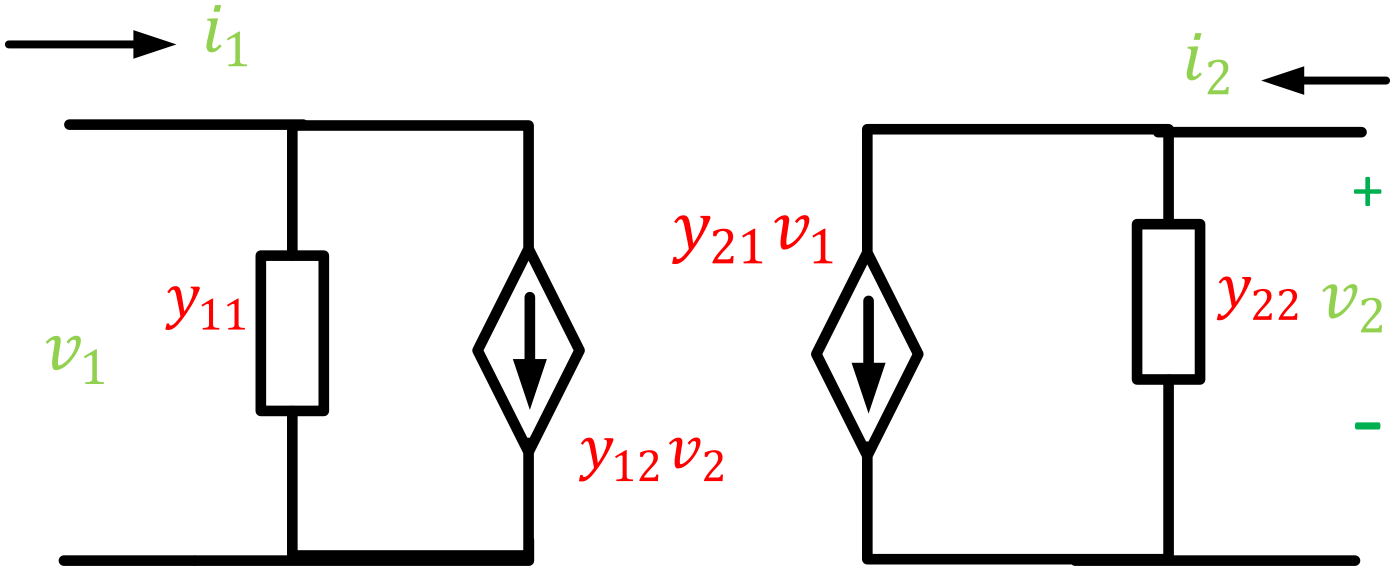
Inverter = NOT GATE



Ac small signal Equivalent for FET

$$i_1 = y_{11}v_1 + y_{12}v_2$$

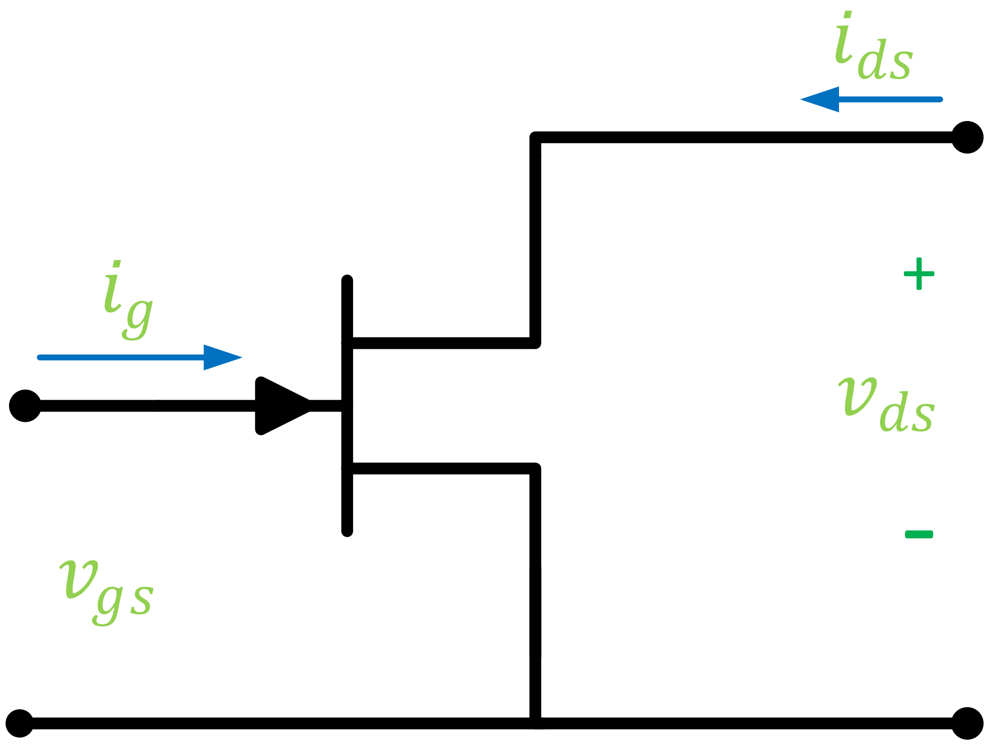
$$i_2 = y_{21}v_1 + y_{22}v_2$$



$$i_g = y_{11} v_{gs} + y_{12} v_{ds}$$

$$i_{ds} = y_{21} v_{gs} + y_{22} v_{ds}$$

$$y_{11} = \frac{i_g}{v_{gs}} \bigg|_{v_{ds}=0} = \frac{\Delta i_{G(t)}}{\Delta V_{GS(t)}} \bigg|_{V_{DS(t)}=V_{DSQ}}$$



But $i_{G(t)} = 0$

$\therefore y_{11} = 0$

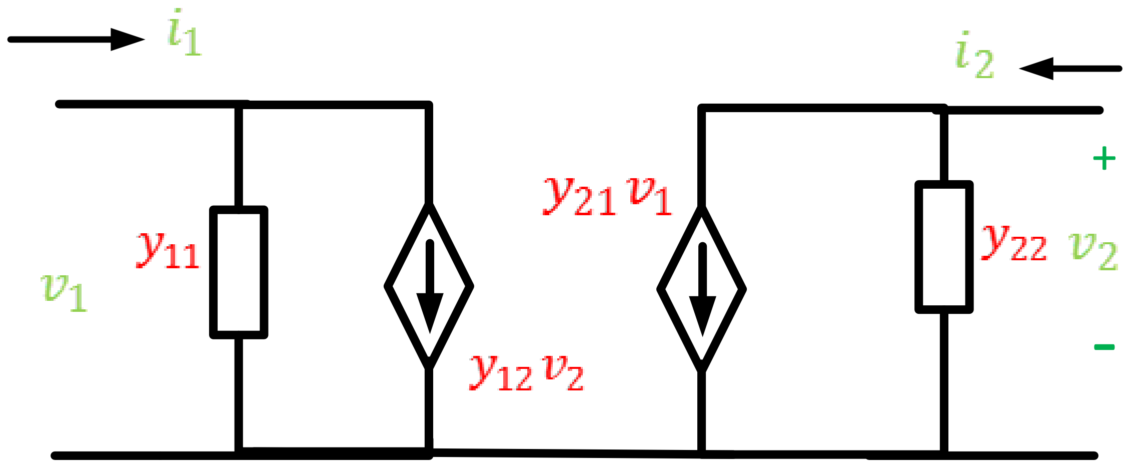
(open circuit)

$$y_{12} = \frac{i_g}{v_{ds}}\Big|_{v_{gs=0}} = \frac{\Delta i_{G(t)}}{\Delta V_{DS(t)}}\Big|_{V_{GS(t)}=V_{GSQ}}$$

But $i_{G(t)} = 0$

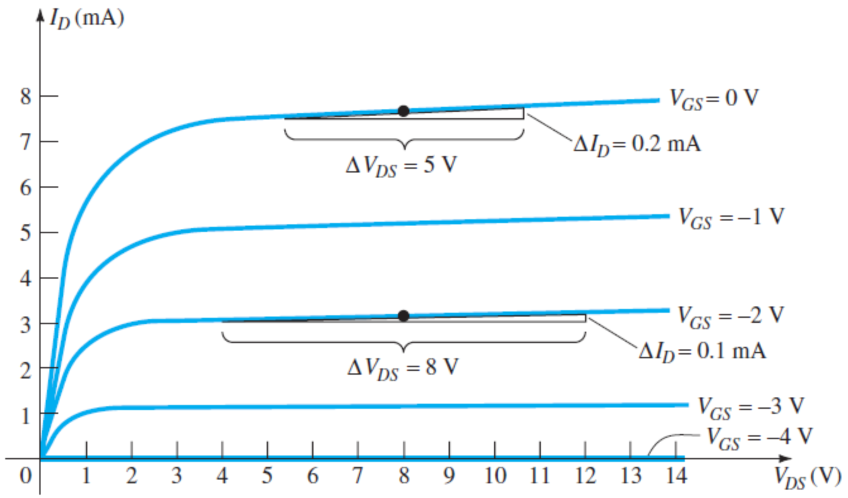
$$\therefore\ y_{12} = 0$$

$$\therefore\ y_{12} v_{gs} = 0$$



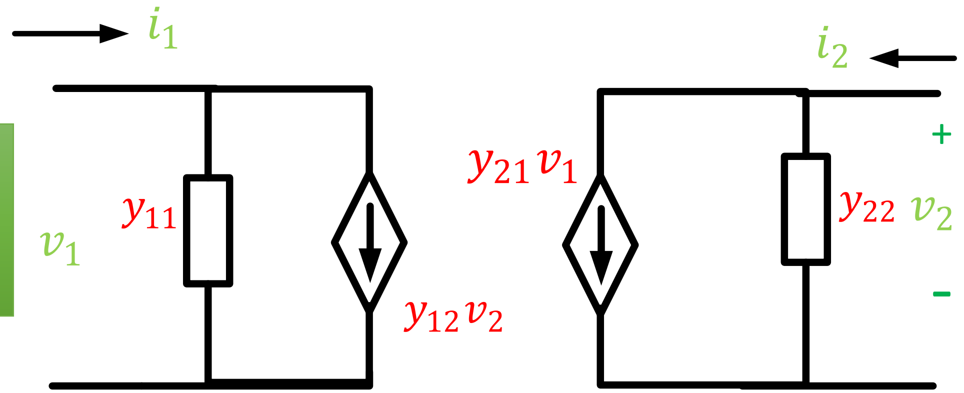
(open circuit)

$$y_{22} = \frac{i_{ds}}{v_{ds}}\Big|_{v_{gs}=0} = \frac{\Delta i_{DS(t)}}{\Delta V_{DS(t)}}\Big|_{V_{GS(t)}=V_{GSQ}}$$



$$\frac{1}{y_{22}} = r_{ds} = \frac{V_A}{I_{DSQ}}$$

$$y_{21} = \frac{i_{ds}}{v_{gs}}\Big|_{v_{ds}=0} = \frac{\Delta i_{DS(t)}}{\Delta V_{GS(t)}}\Big|_{V_{DS(t)}=V_{DSQ}}$$



$$y_{21} = \frac{d\, i_{DS(t)}}{d\, V_{GS(t)}}\Big|_Q$$

$y_{21} = g_m$; Forward Trans conductance

1) For JFET and DMOSFET

$$i_{DS}(t) = I_{DSS}\left(1 - \frac{V_{GS}(t)}{V_P}\right)^2$$

$$g_m = \frac{-2I_{DSS}}{V_p}\left(1 - \frac{V_{GS}(t)}{V_P}\right)\Big|_Q$$

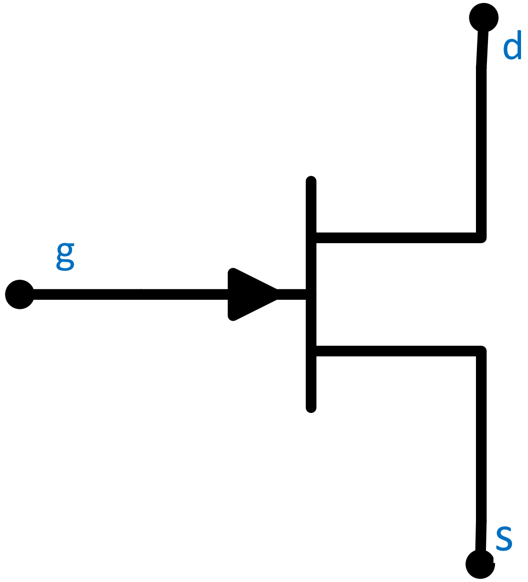
$$g_m = \frac{-2I_{DSS}}{V_p}\left(1 - \frac{V_{GS}}{V_P}\right)$$

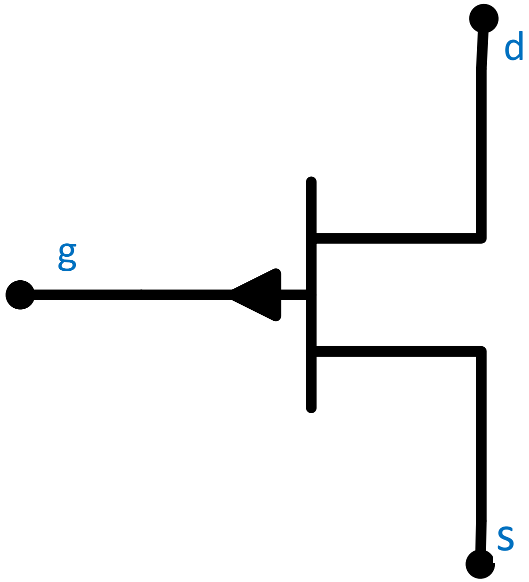
2) For EMOSFET

$$i_{DS} = K_n(V_{GS}(t) - V_T)^2$$

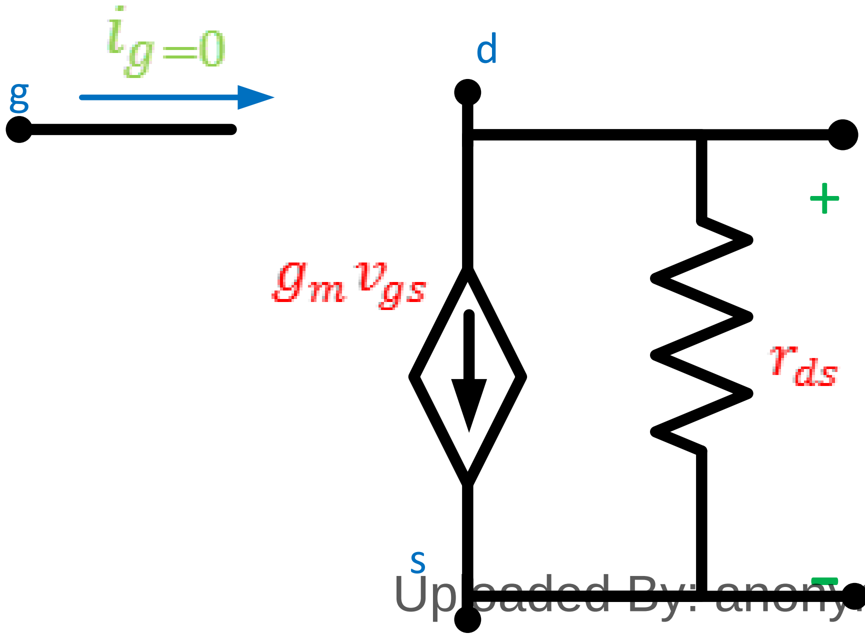
$$g_m = 2K_n(V_{GS} - V_T)$$

$$g_m = 2\sqrt{K_n I_{DS}}$$ **proof !!**

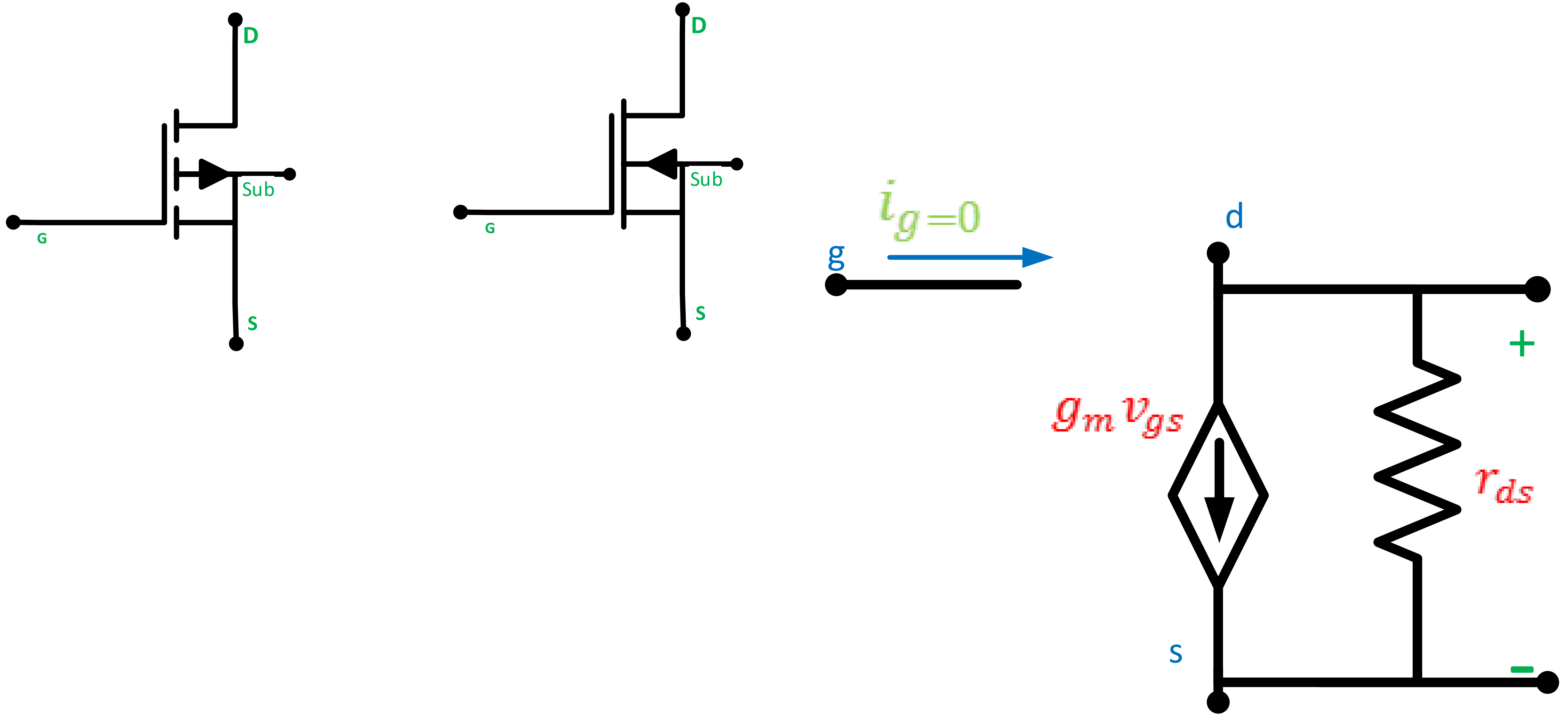




ac small signal equivalent circuit of JFET



ac small signal equivalent circuit for MOSFET



FET Ac Small Signal Amplifiers

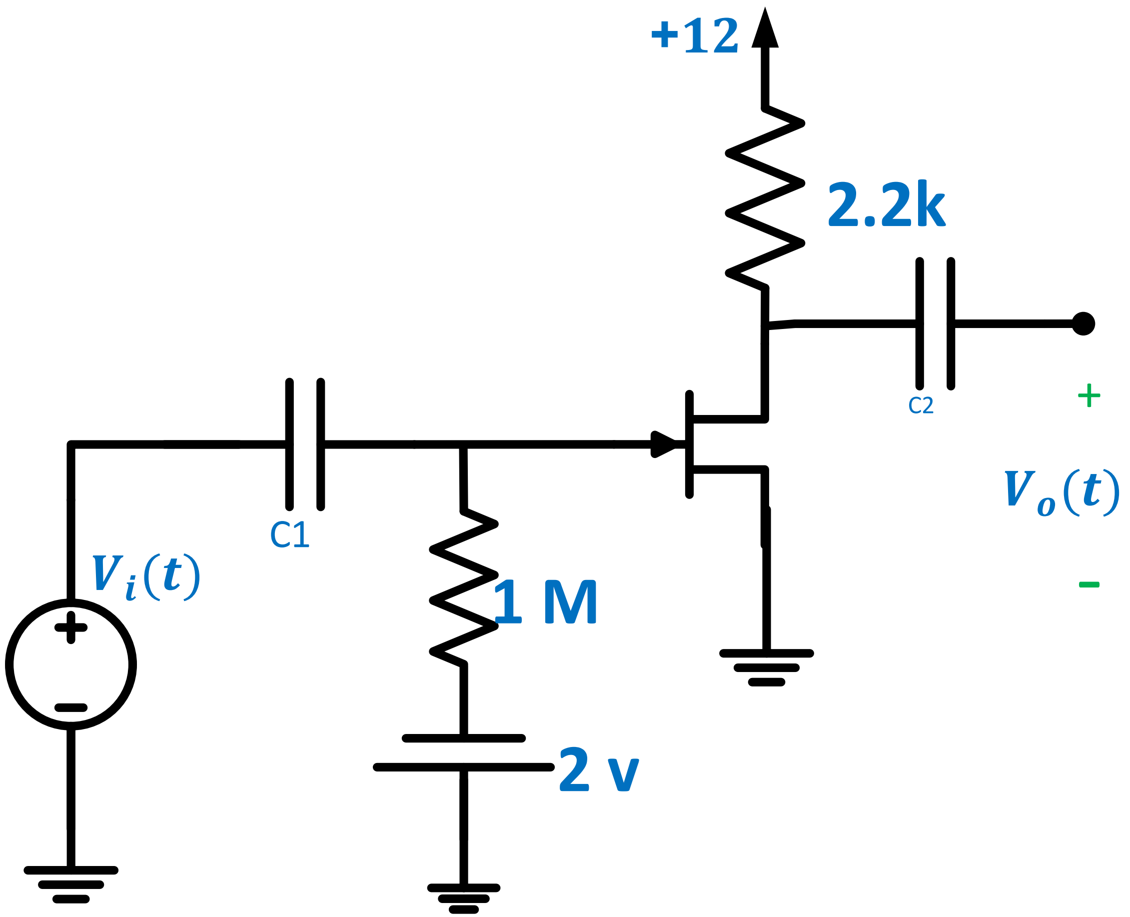
I_{DSS}= 12mA
V_p= - 4 v
r_{dS}= 100 K

1) Common Source Amplifier

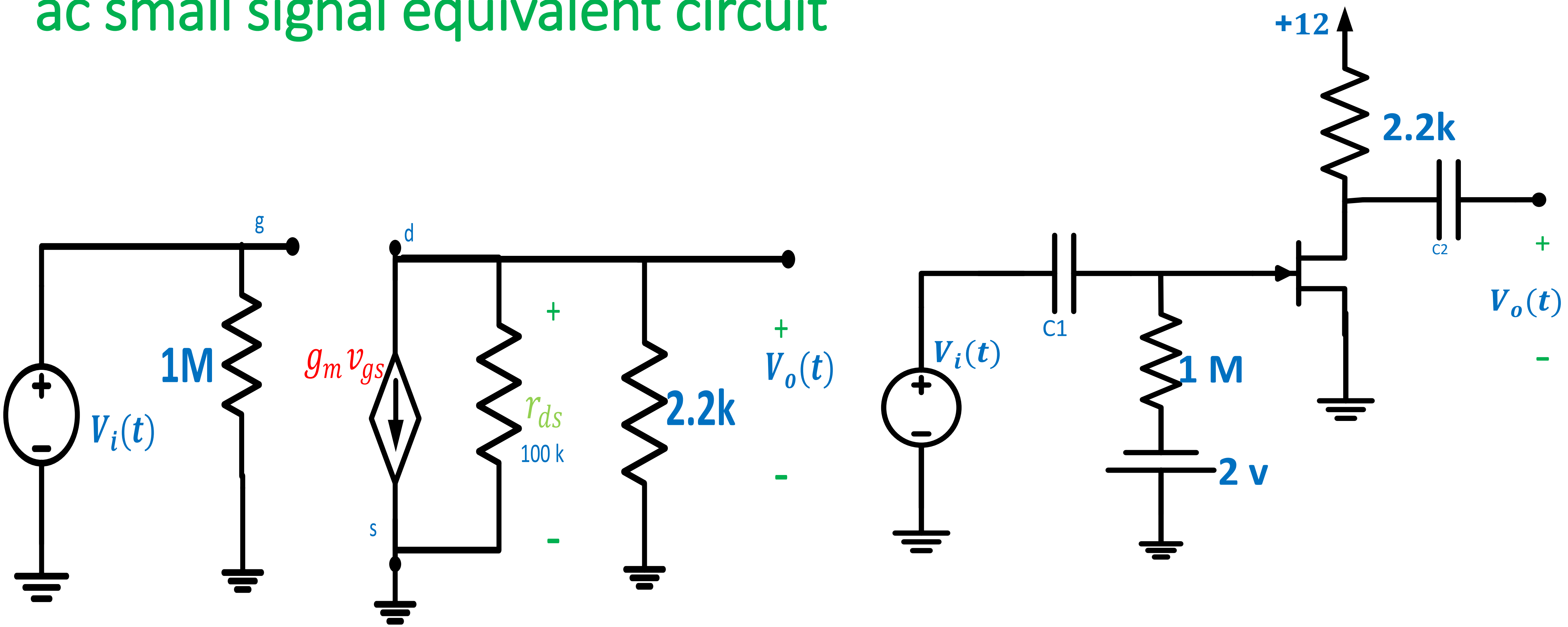
$$g_m = \frac{-2I_{DSS}}{V_p}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$V_{GS} = -2\text{ v}$$

$$\therefore\ g_m = 3\text{m}\ \mho$$



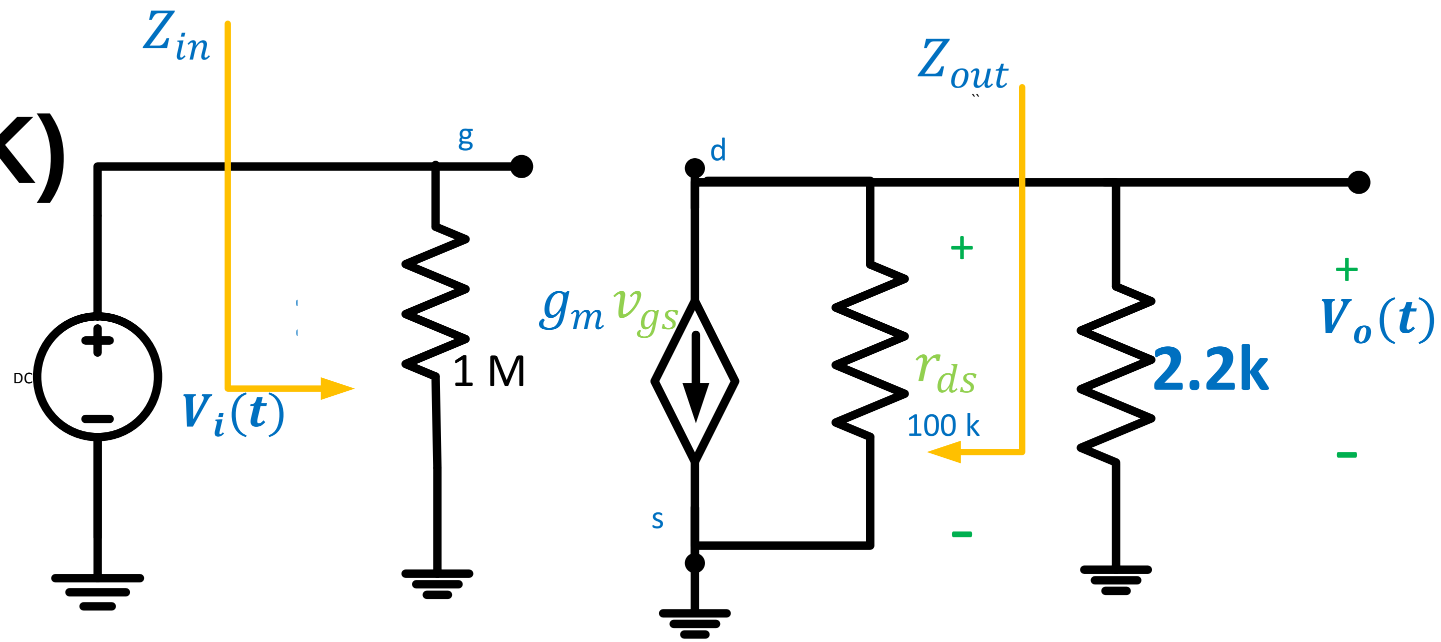
ac small signal equivalent circuit



ac small signal equivalent circuit

v_O = - $g_m v_{gs}$(100K \\ 2.2K)

$v_{gs} = v_g - v_S$



$v_S = 0$

$v_g = V_i$

A_v = - 6.6

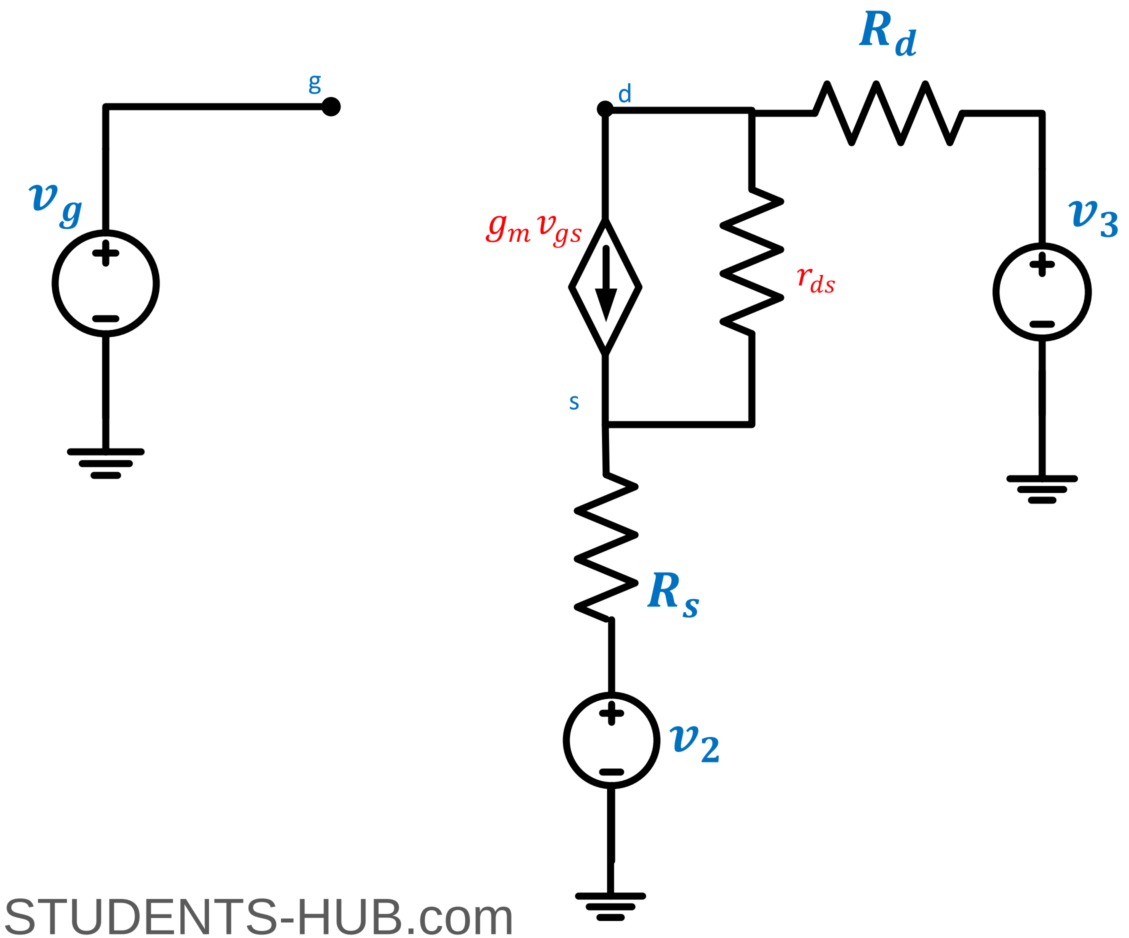
$Z_i = 1M\Omega$

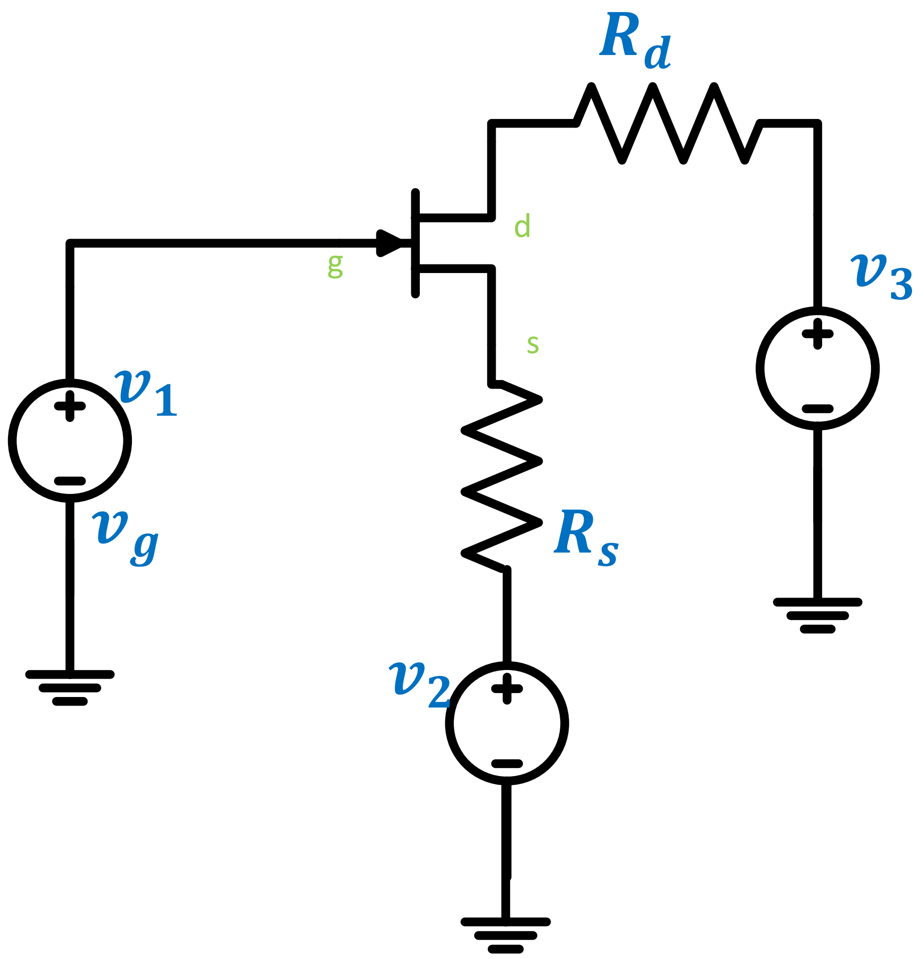
$$A_v = \frac{v_O}{V_i} = -\, g_m \text{ (100K \\ 2.2K)}$$

$Z_o = r_{ds}$ = 100K

Impedance Reflection

ac small signal equivalent circuit





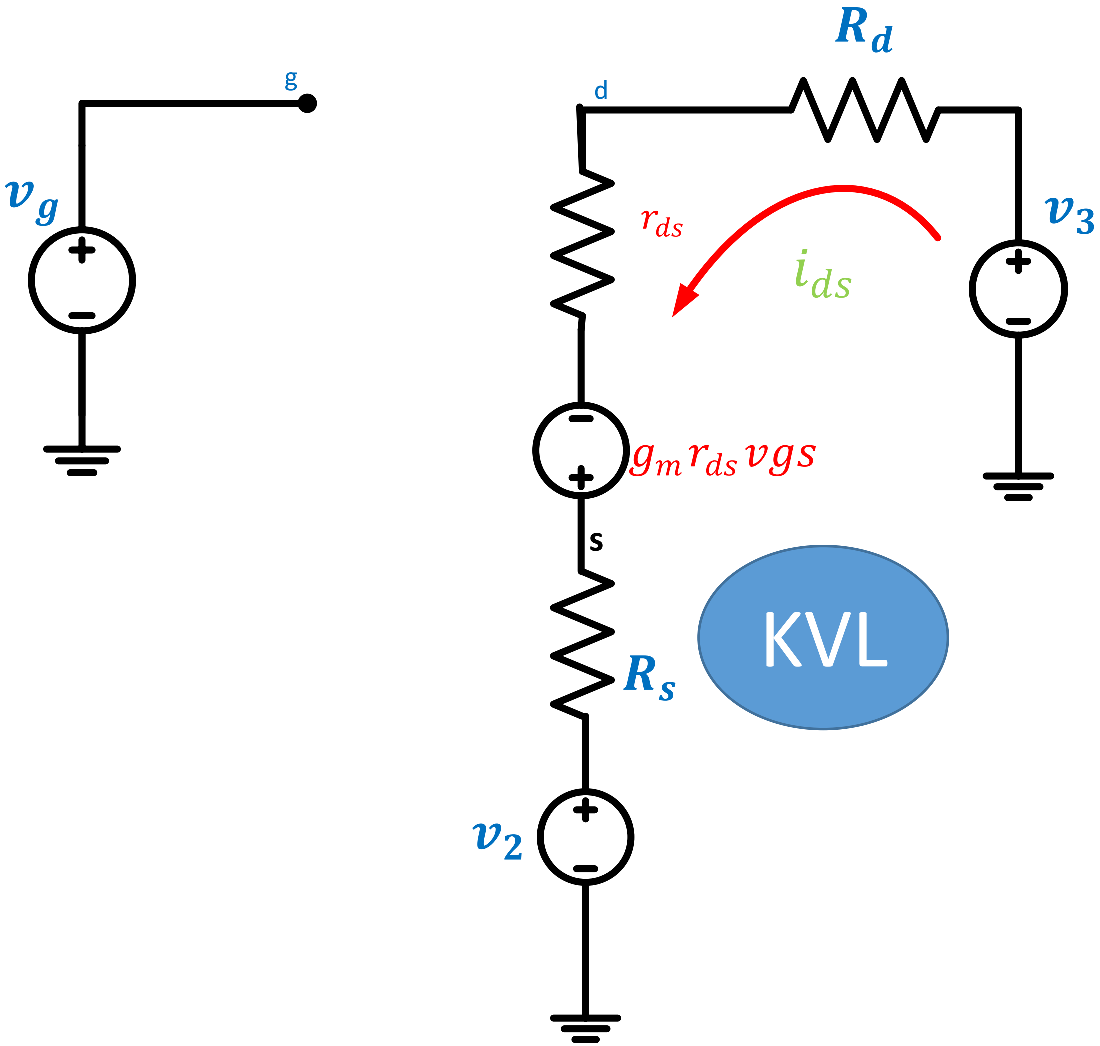
$$\text{let } g_m r_{ds} = \mu$$

$$i_{ds} = \frac{v_3 + \mu v_{gs} - v_2}{R_d + R_s + r_{ds}}$$

$$v_{gs} = v_g - v_s$$

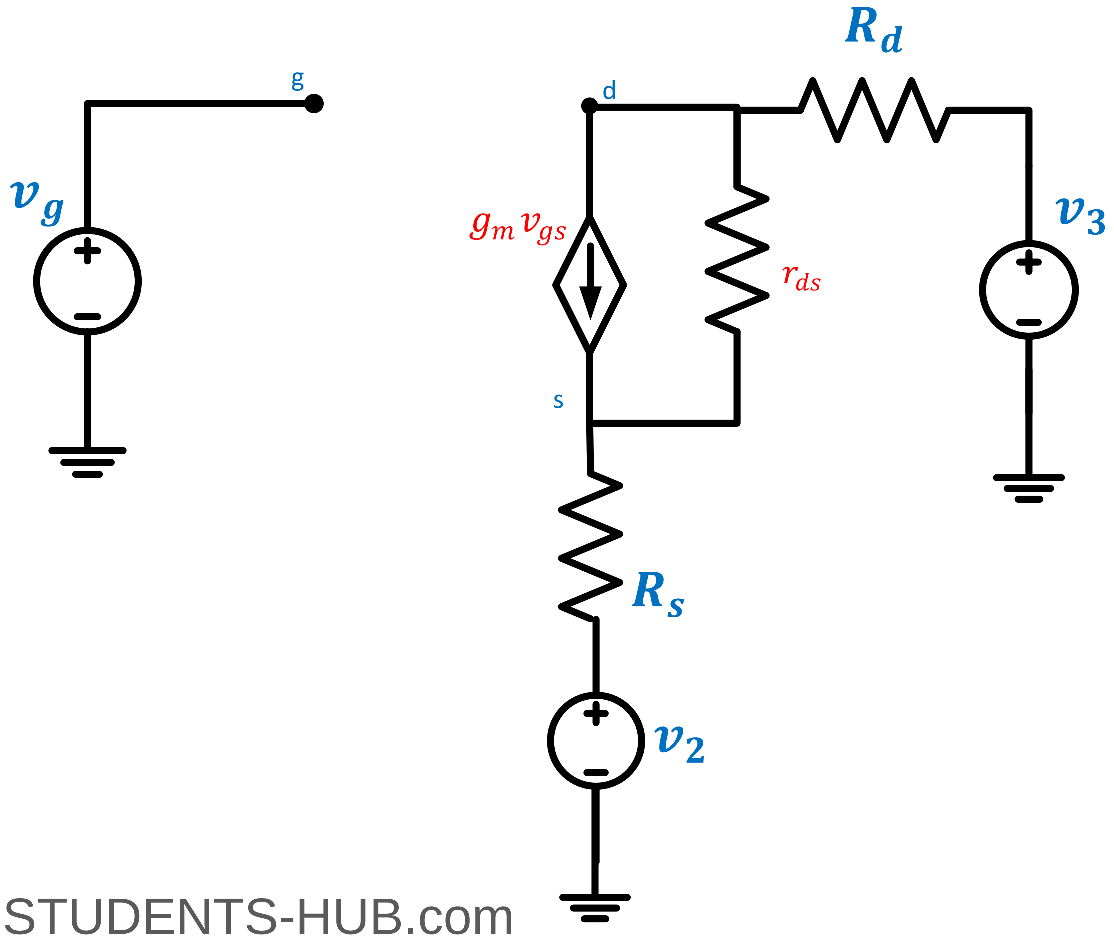
$$v_s = R_s i_{ds} + v_2$$

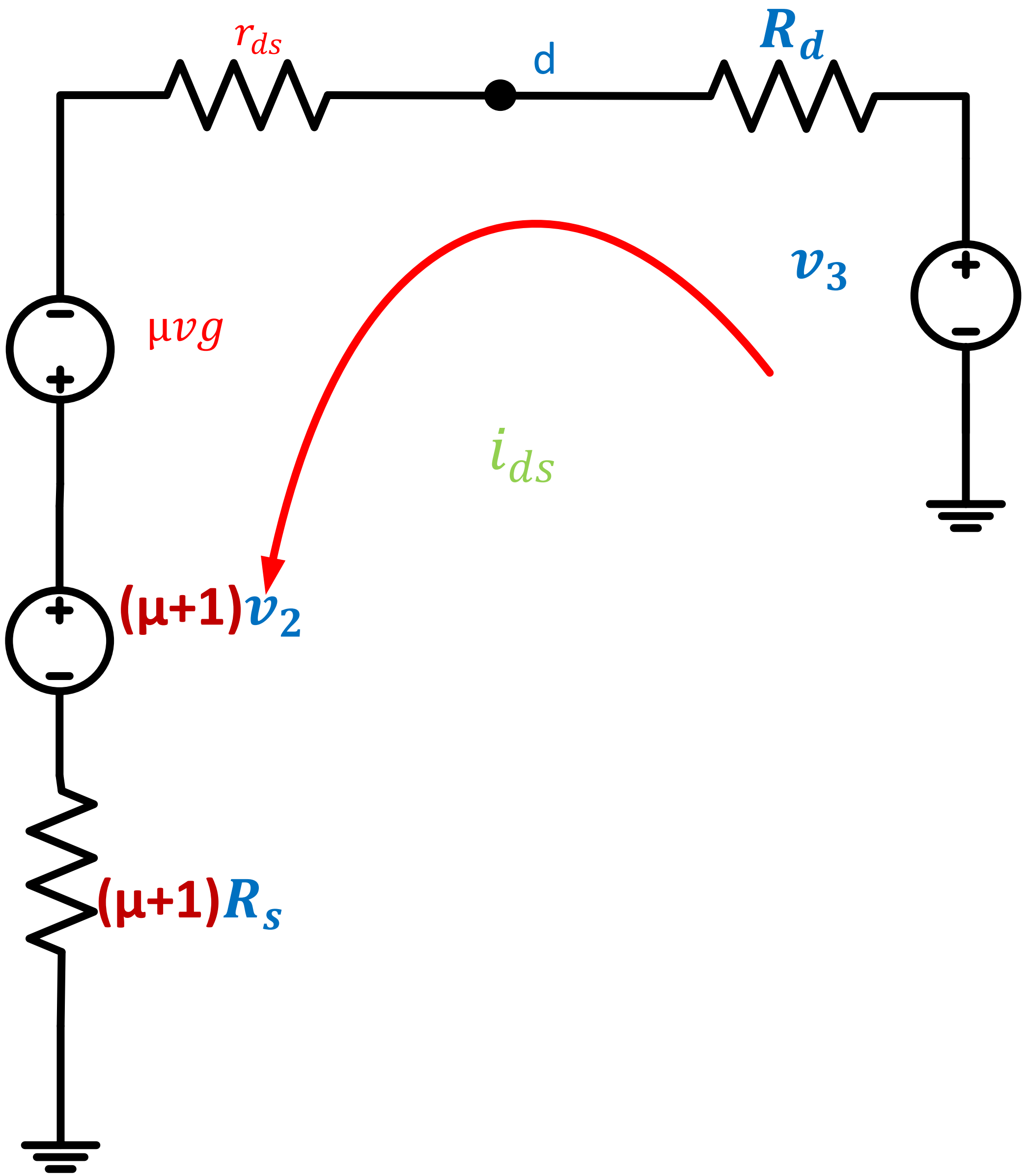
$$\therefore \quad i_{ds} = \frac{\mu v_g + v_3 - (\mu+1) v_2}{r_{ds} + R_d + (\mu+1) R_s}$$



Drain equivalent circuit

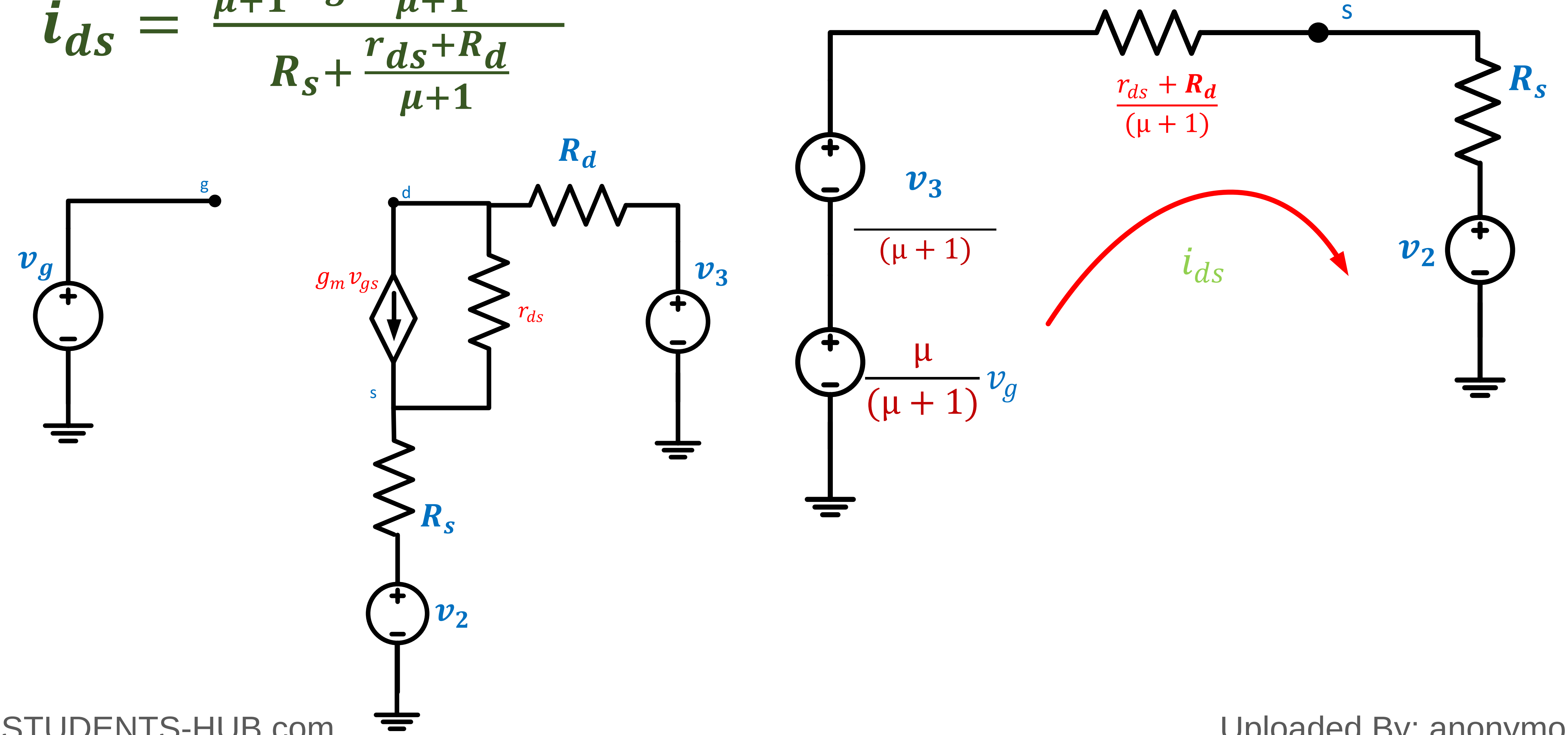
$$i_{ds} = \frac{\mu\, v_g + v_3 - (\mu+1)v_2}{r_{ds} + R_d + (\mu+1)R_s}$$





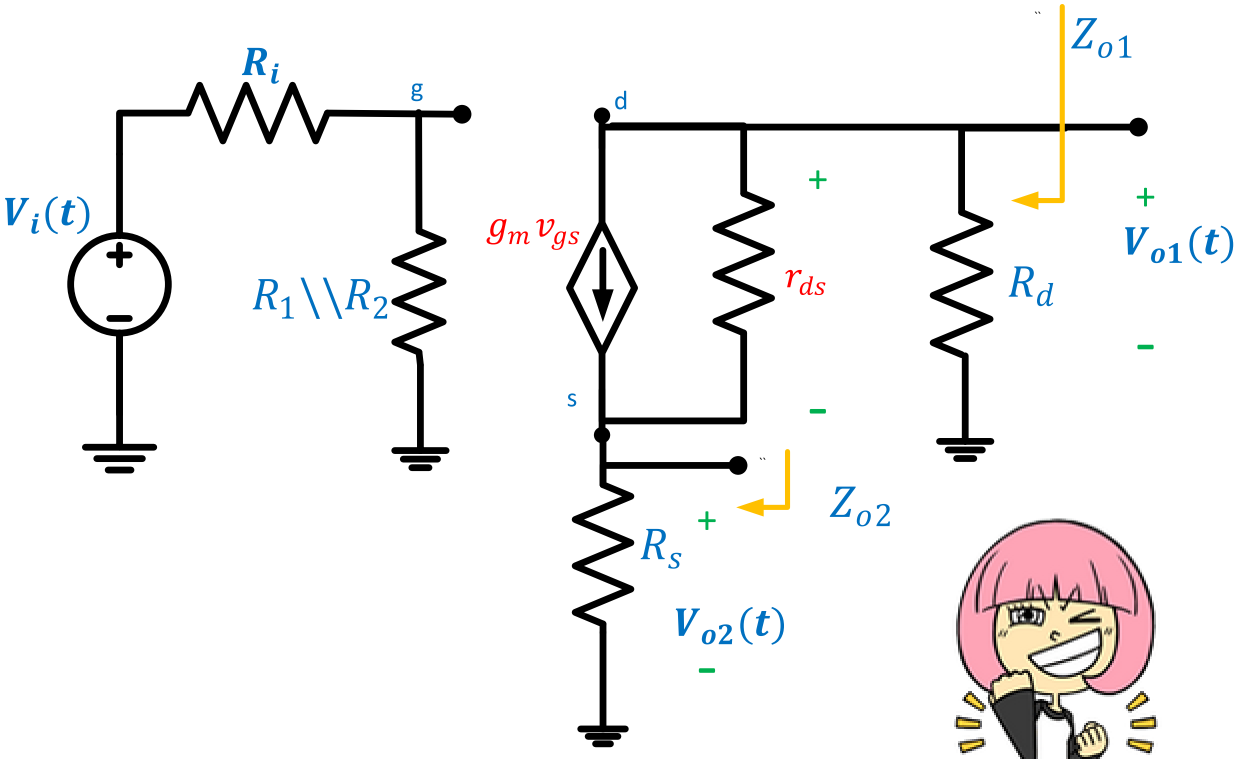
Source equivalent circuit

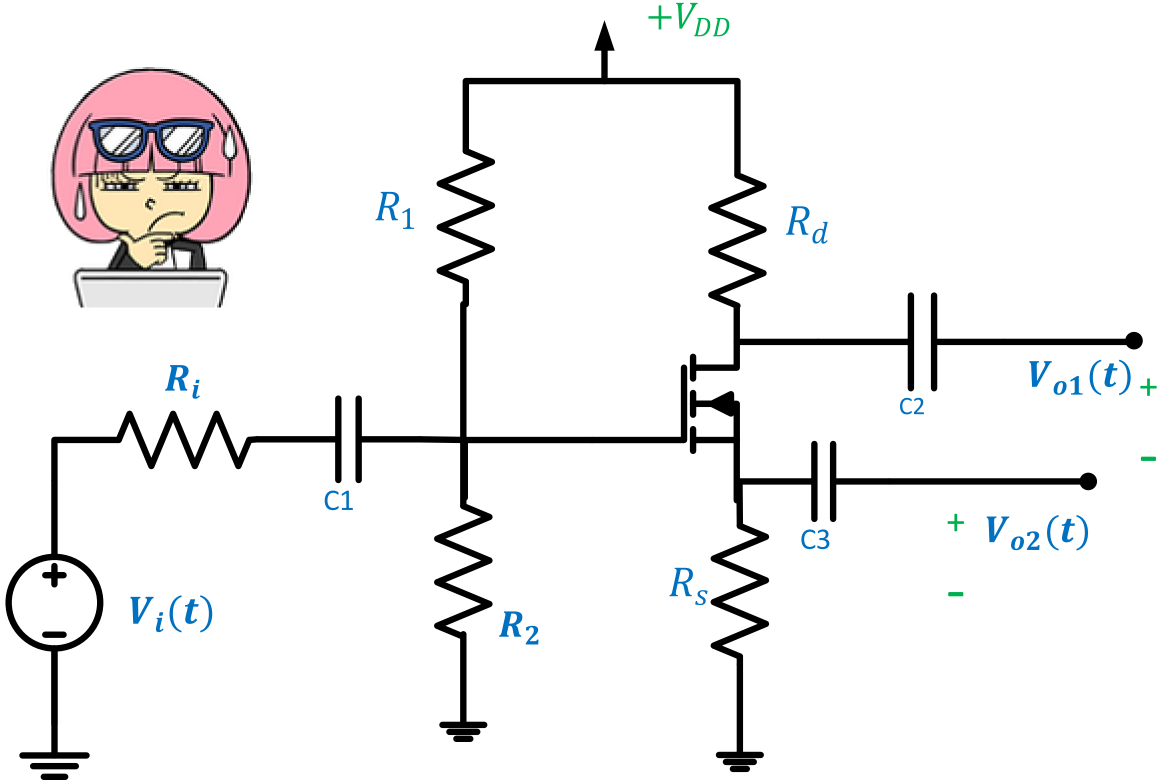
$$i_{ds} = \frac{\frac{\mu}{\mu+1} v_g + \frac{v_3}{\mu+1} - v_2}{R_s + \frac{r_{ds}+R_d}{\mu+1}}$$



Phase splitting circuit

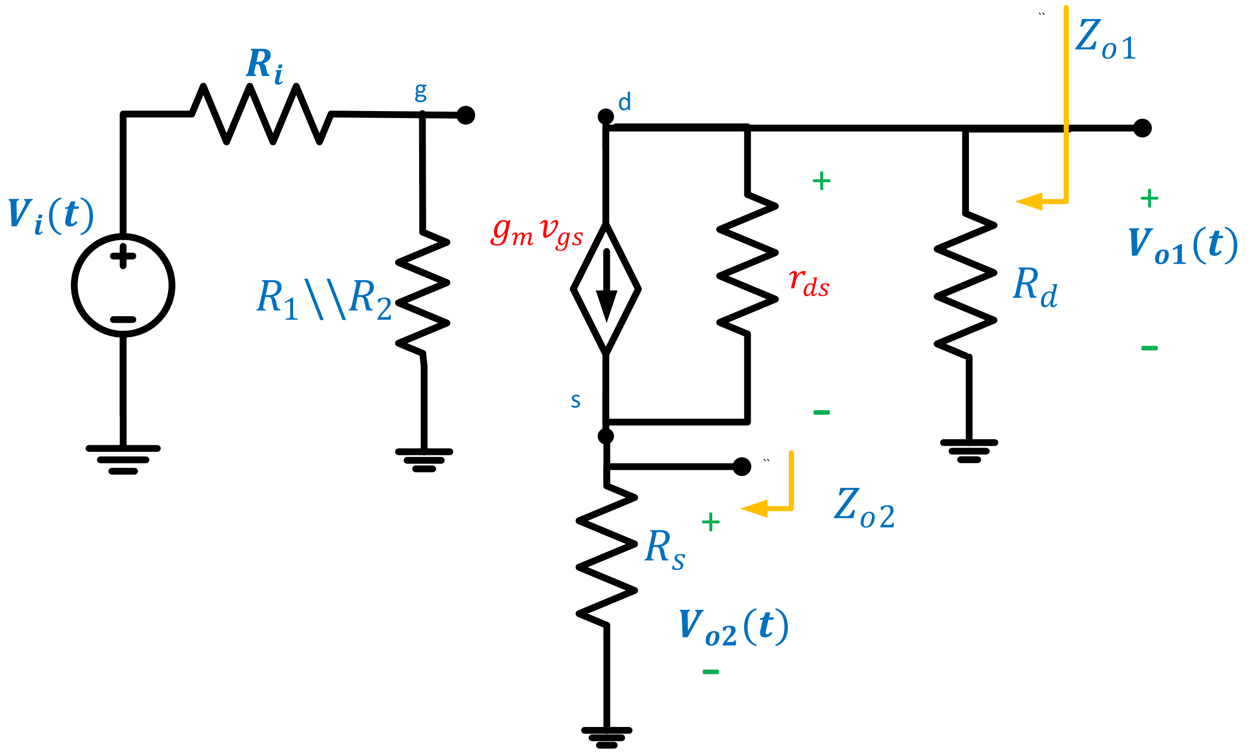
ac small signal equivalent circuit





To find v_{o1} , and Z_{o1}

$\rightarrow$ **drain equivalent CKT**



$$v_{o1} = -\frac{R_d\,\mu\,v_g}{r_{ds}+R_d+(\mu+1)R_s}$$

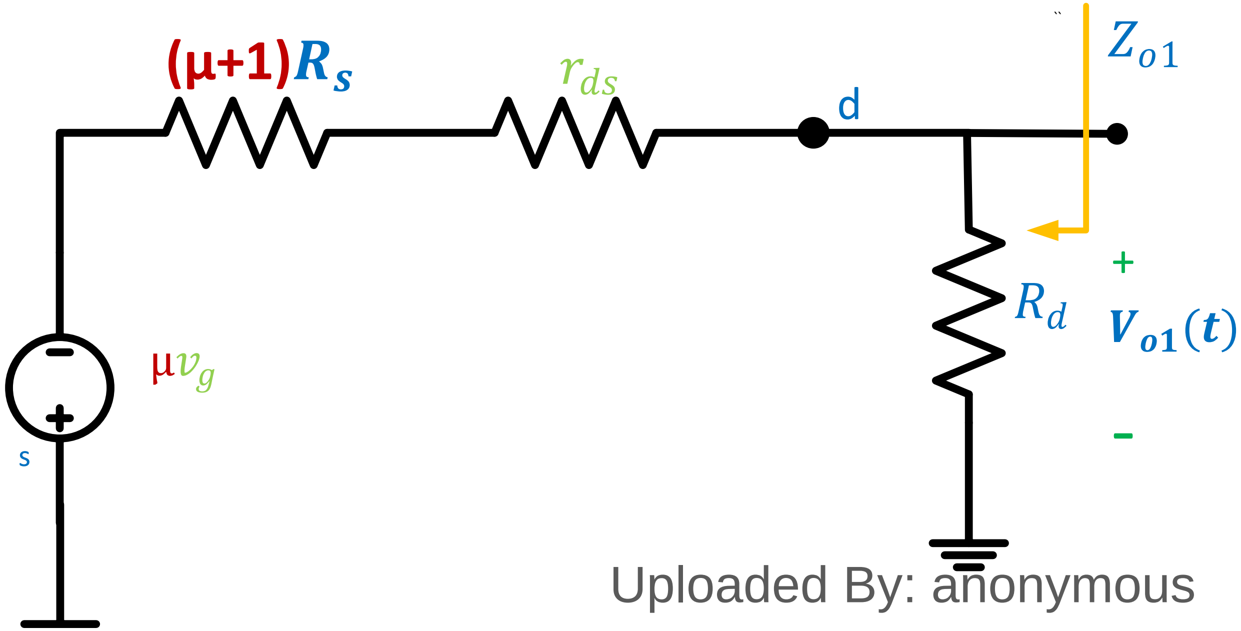
$$v_g = \frac{R_1 \,||\, R_2}{R_1 \,||\, R_2+R_i}\, v_i$$

$$\therefore \quad v_{o1} = -\frac{R_1 \,||\, R_2}{R_1 \,||\, R_2+R_i} \cdot \frac{R_d\ \mu}{r_{ds}+R_d+(\mu+1)R_s}\, v_i$$

$$Z_{o1} = R_d \,||(r_{ds} + (\mu+1)R_s)$$

if $r_{ds} = \infty$

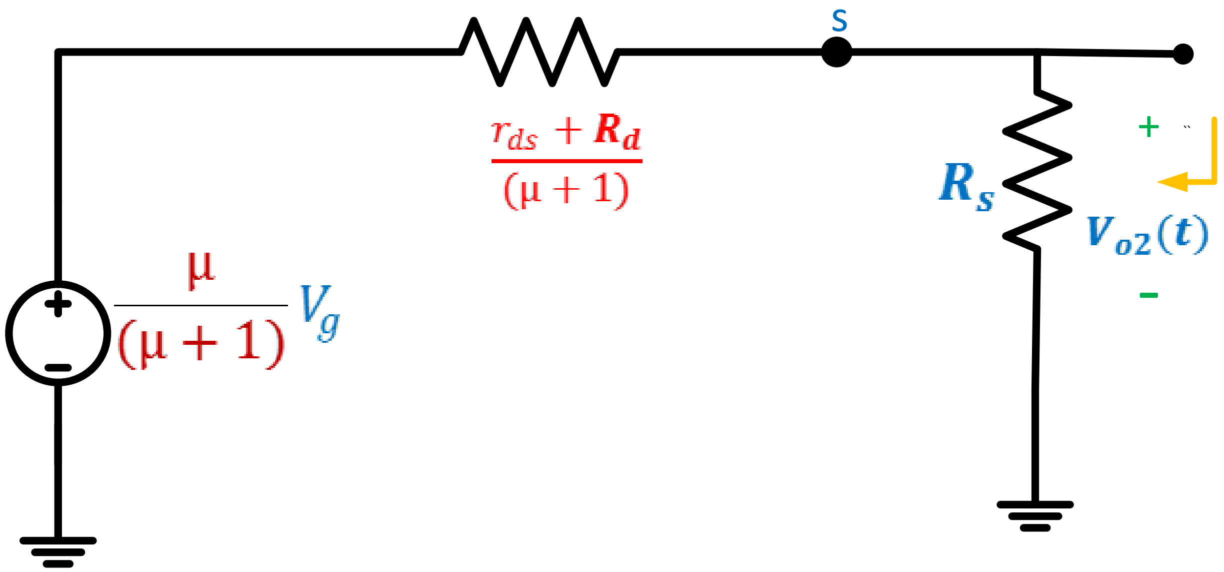
$$\therefore \quad Z_{o1} = R_d$$



To find V_{o2} , and Z_{o2}

→source equivalent CKT

$$v_{o1} = -\frac{R_1 \,||\, R_2}{R_1 \,||\, R_2 + R_i} \cdot \frac{R_d \;\mu}{r_{ds}+R_d+(\mu+1)R_s} v_i$$



$$v_{o2} = \frac{R_s \left(\frac{\mu}{\mu+1}\right) v_g}{R_s + \frac{r_{ds}+R_d}{\mu+1}}$$

$$v_g = \frac{R_1 \,||\, R_2}{R_1 \,||\, R_2 + R_i} v_i$$

$$v_{o2} = \frac{R_1 \,||\, R_2}{R_1 \,||\, R_2 + R_i} \cdot \frac{R_s \left(\frac{\mu}{\mu+1}\right) v_g}{R_s + \frac{r_{ds}+R_d}{\mu+1}}$$

$$v_{o2} = \frac{R_1 \,||\, R_2}{R_1 \,||\, R_2 + R_i} \cdot \frac{R_s (\mu) v_i}{(r_{ds}+R_d) + (\mu+1)R_s}$$

if $R_s = R_d$

$$\therefore |V_{o2}| = |V_{o1}|$$

$$Z_{o2} = R_s \,||\, \frac{R_d + r_{ds}}{\mu+1}$$

$$Z_{o2} = R_s \,||\, \frac{R_d + r_{ds}}{\mu + 1}$$

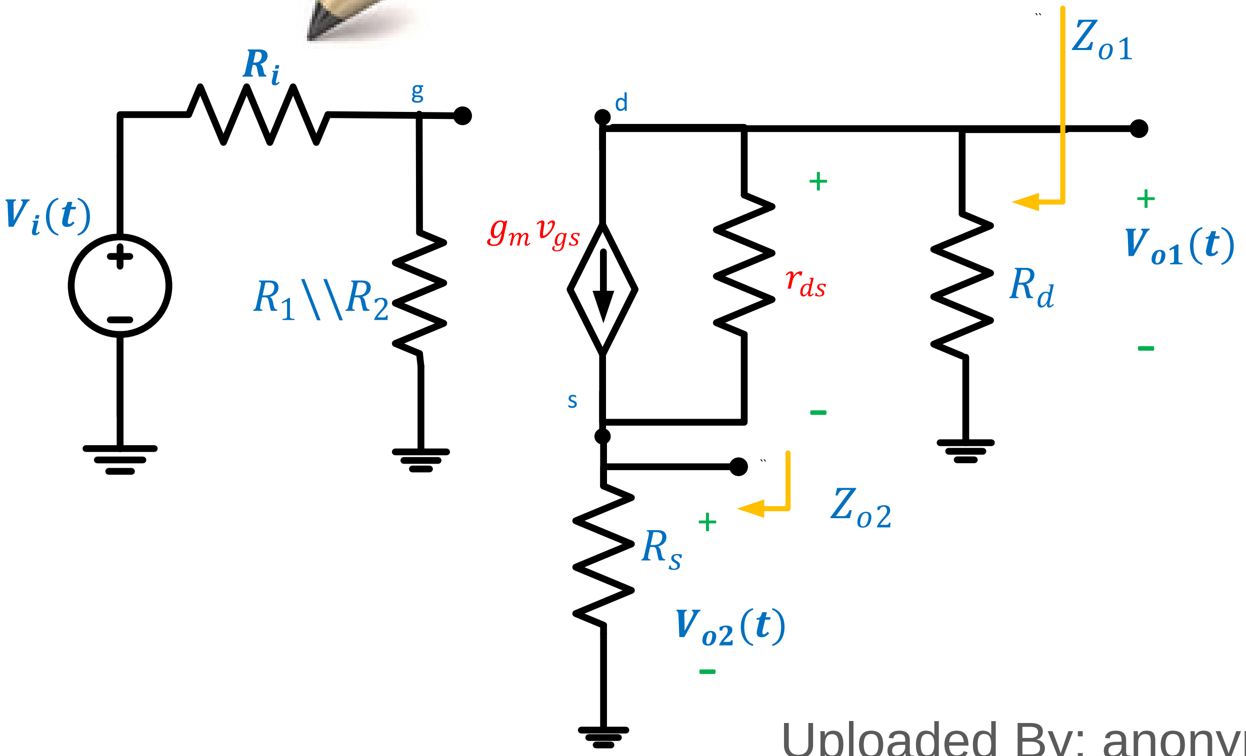
If $r_{ds} = \infty$

$$\frac{R_d + r_{ds}}{\mu + 1} = \frac{R_d + r_{ds}}{g_m r_{ds} + 1}$$

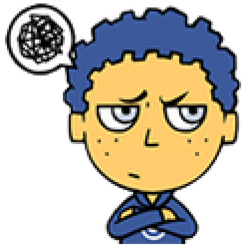
$$\lim_{r_{ds} \to \infty} \frac{R_d + r_{ds}}{g_m r_{ds} + 1} = \frac{1}{g_m}$$

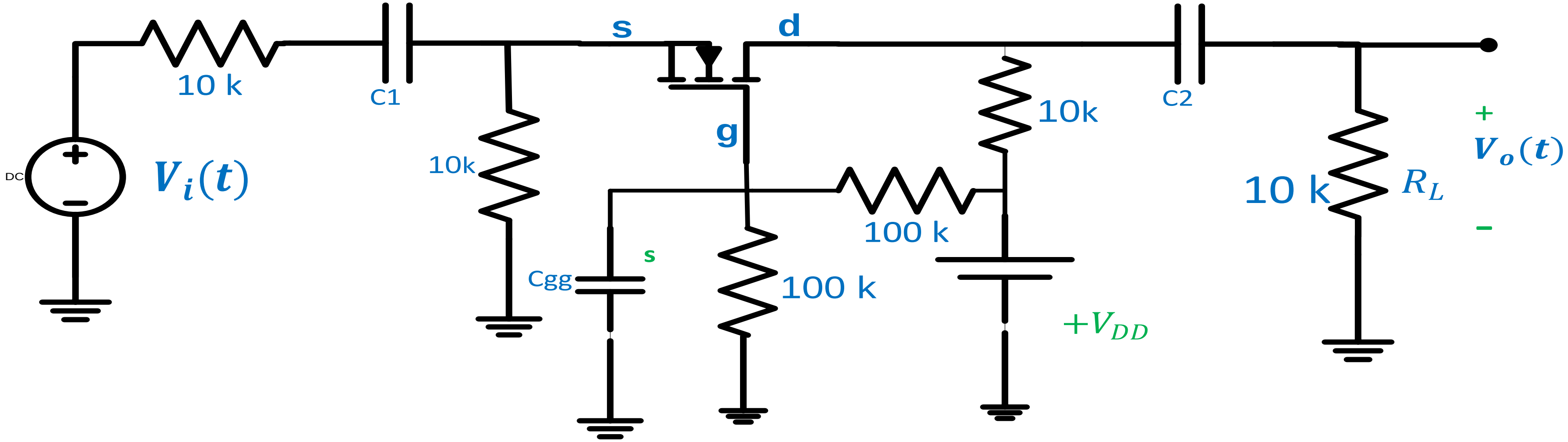
$\therefore$ If $r_{ds} = \infty$

$$Z_{o2} = R_s \,||\, \frac{1}{g_m}$$

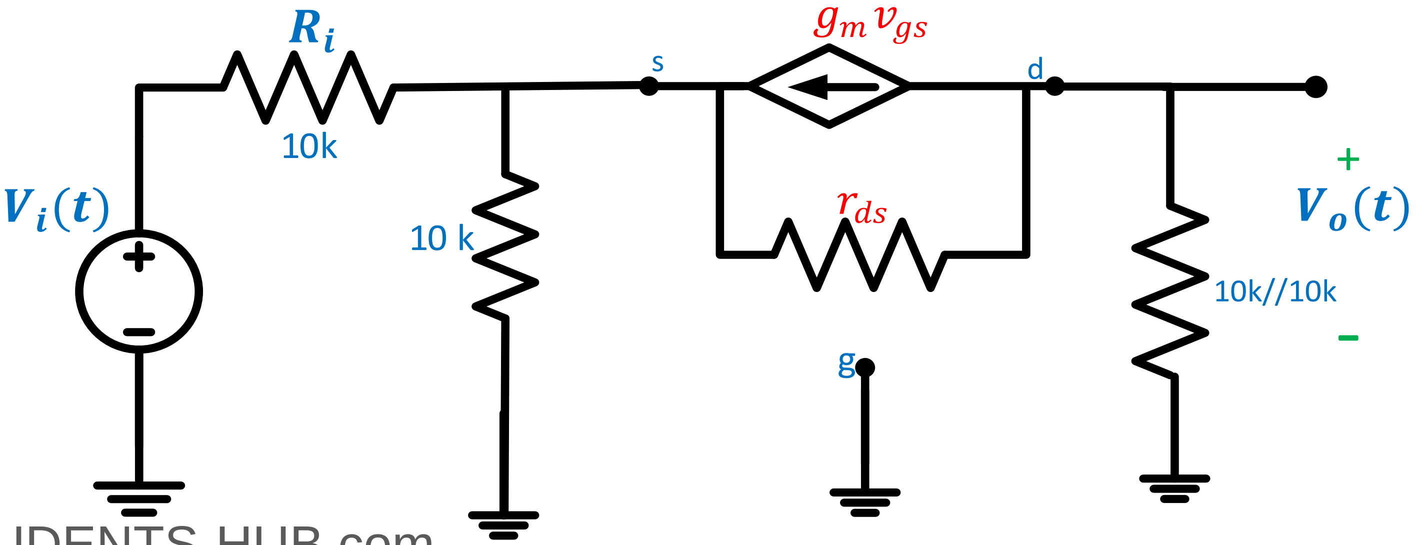


Common Gate Amplifier

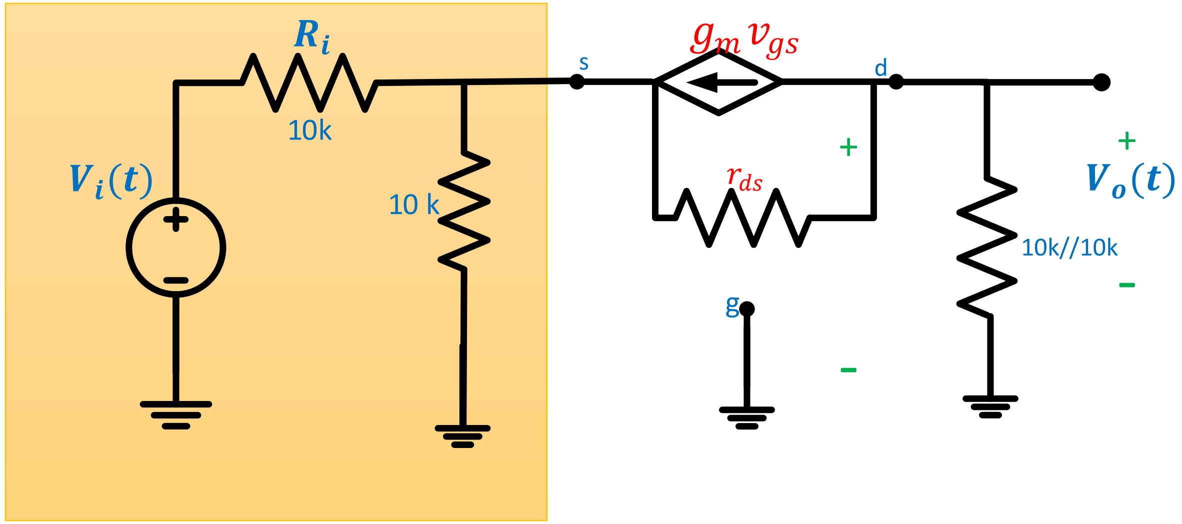


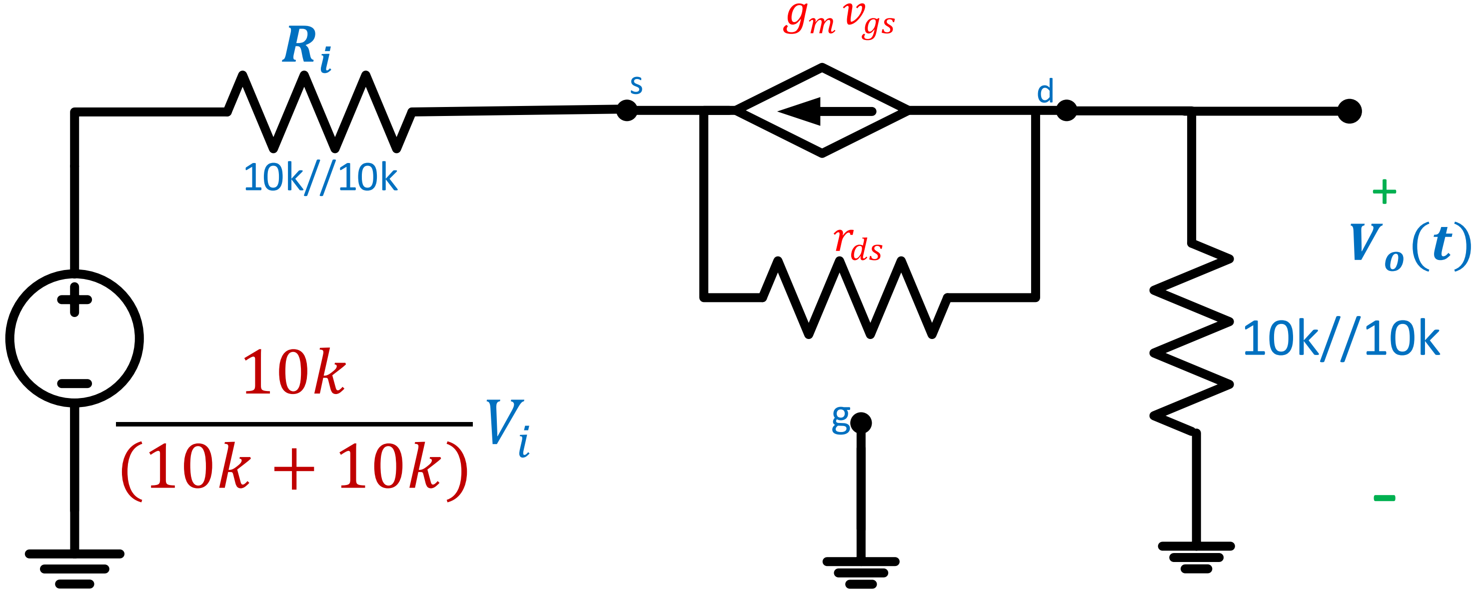


Ac small signal equivalent circuit



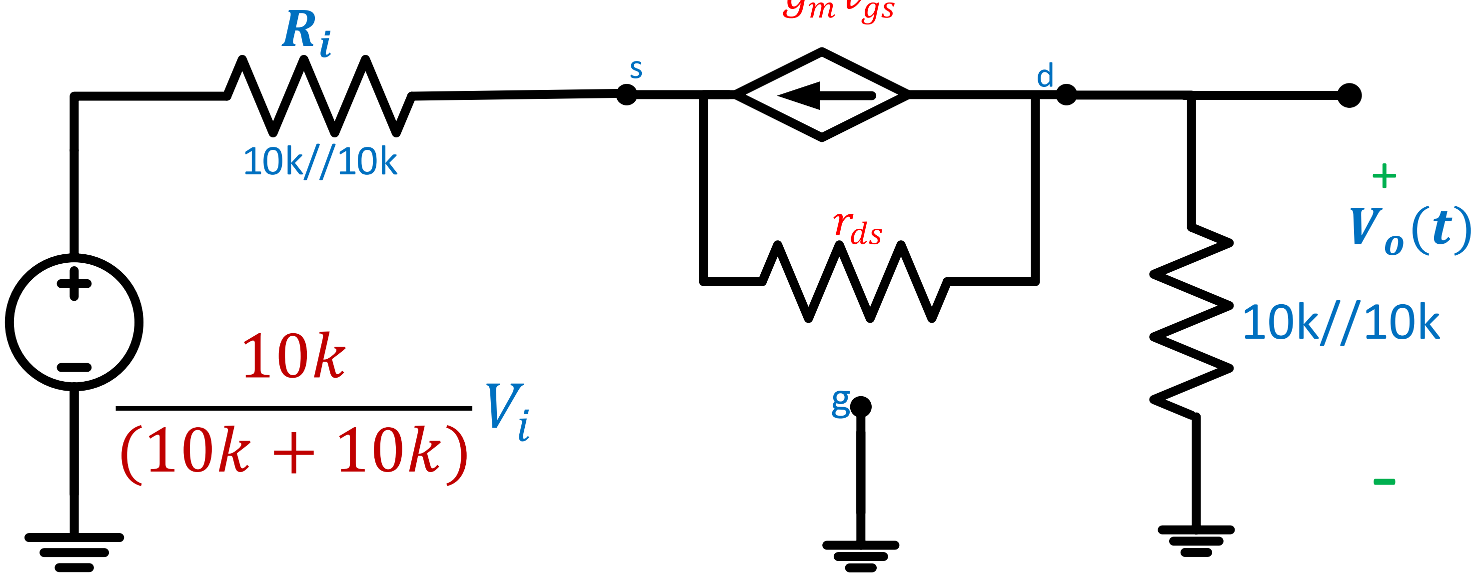
To find v_o $\rightarrow$ Drain equivalent circuit





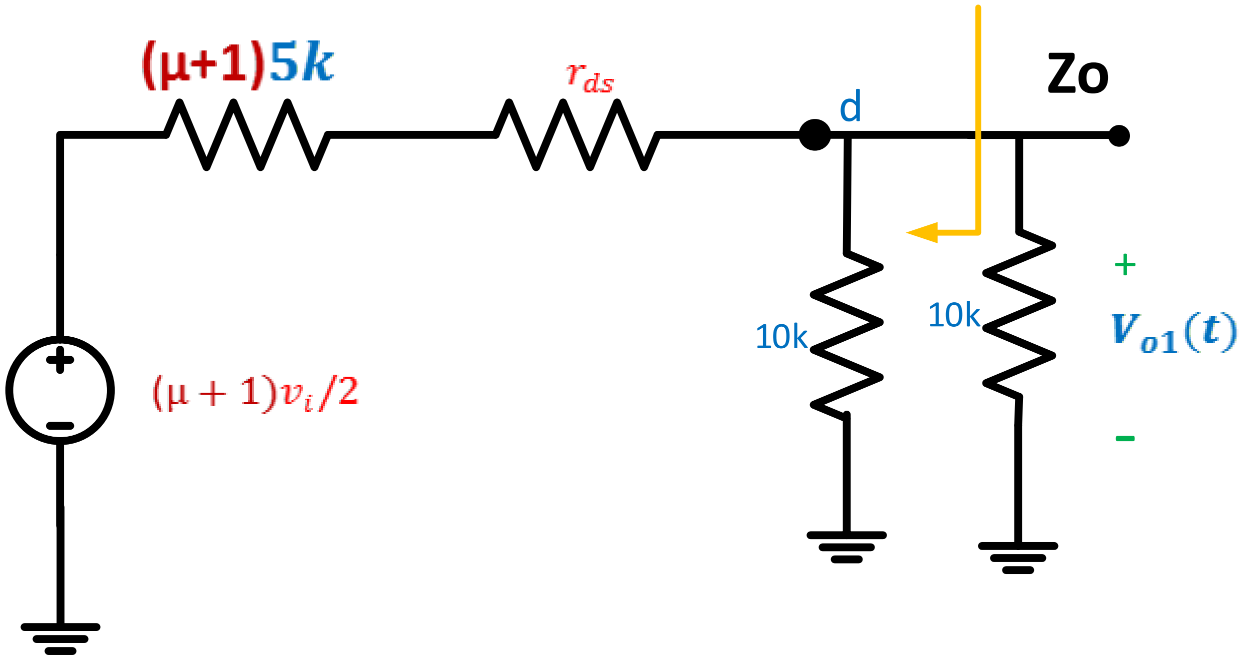
To find v_o , and Z_o

drain equivalent CKT

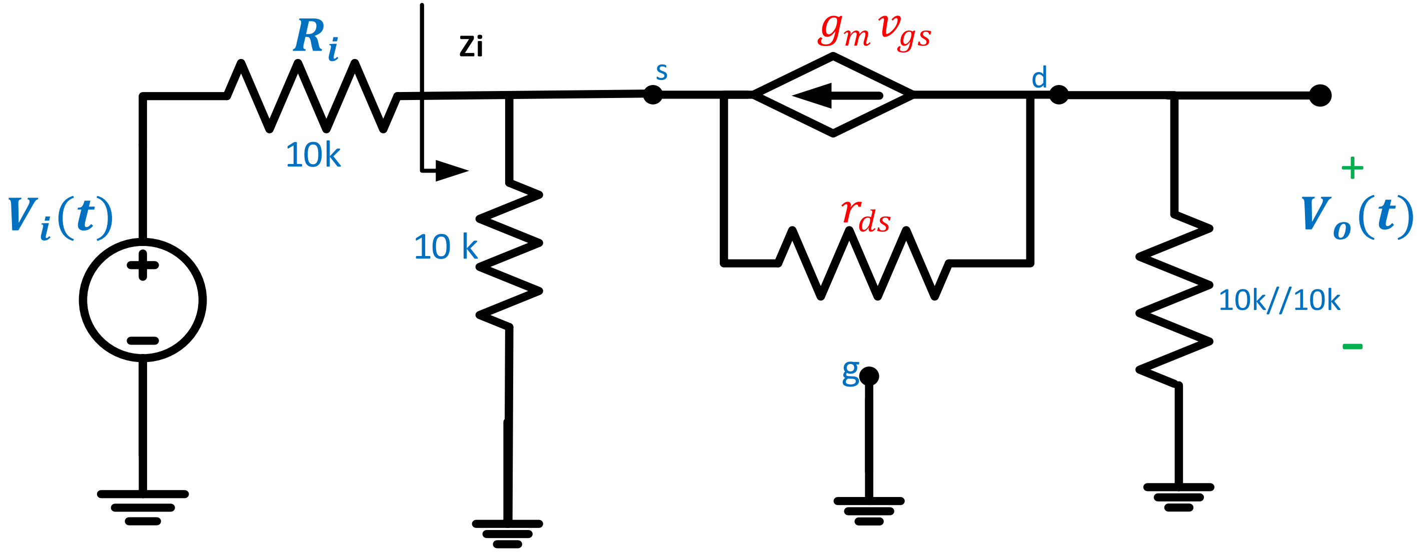


$$v_o = \frac{(10k\,||10k)(\mu+1)\,\frac{1}{2}}{10k\,||10k + r_{ds} + (\mu+1)*5k}\, v_i$$

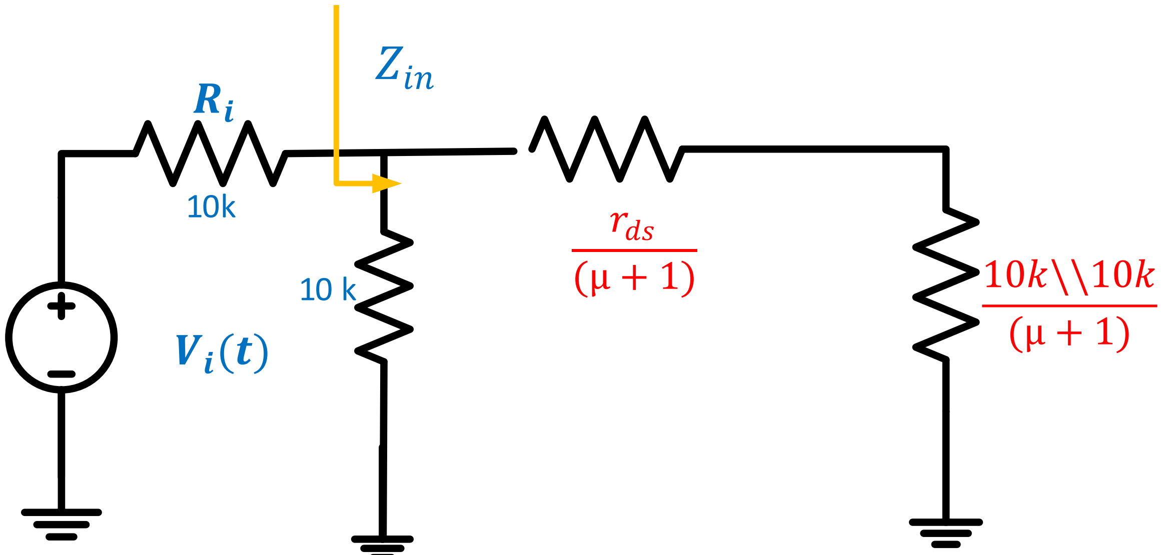
$$Z_o = 10K \,||\, [r_{ds} + (\mu+1)5k]$$



To find Z_i →source equivalent CKT



$$Z_i = 10\text{k} \,||\, \frac{r_{ds}+10k||10k}{\mu+1}$$



Common Source Amplifier :Design

- **Design a Common source MOSFET Amplifier to provide a voltage gain $\left|\frac{V_o}{Vi}\right| = 10$, between a small signal voltage source having a resistance 10kΩ and load $R_L = 10k$**

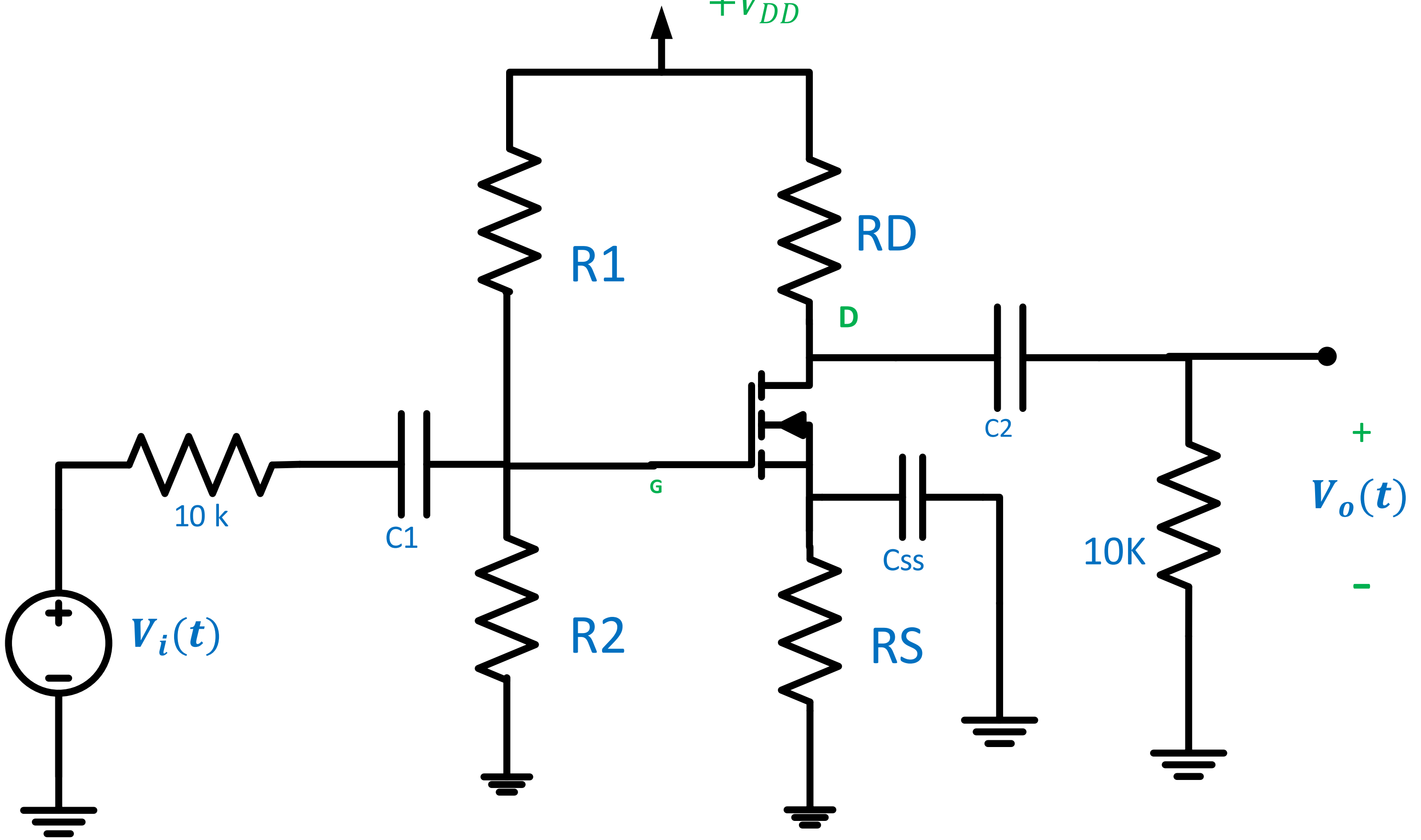
and Zi = 1MΩ.

The MOSFET has rds = 20k , VT = 1.419 V , Kn = $\frac{2\ mA}{V^2}$,

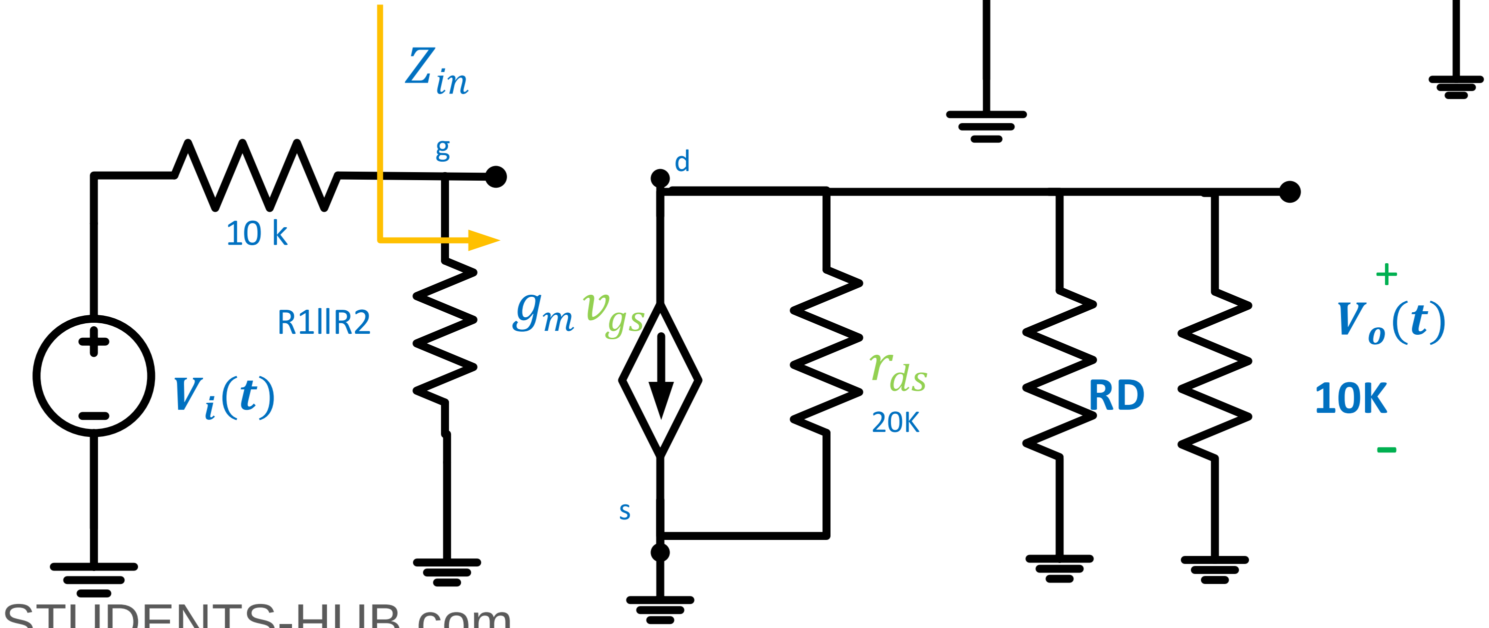
and IDS = 5mA.

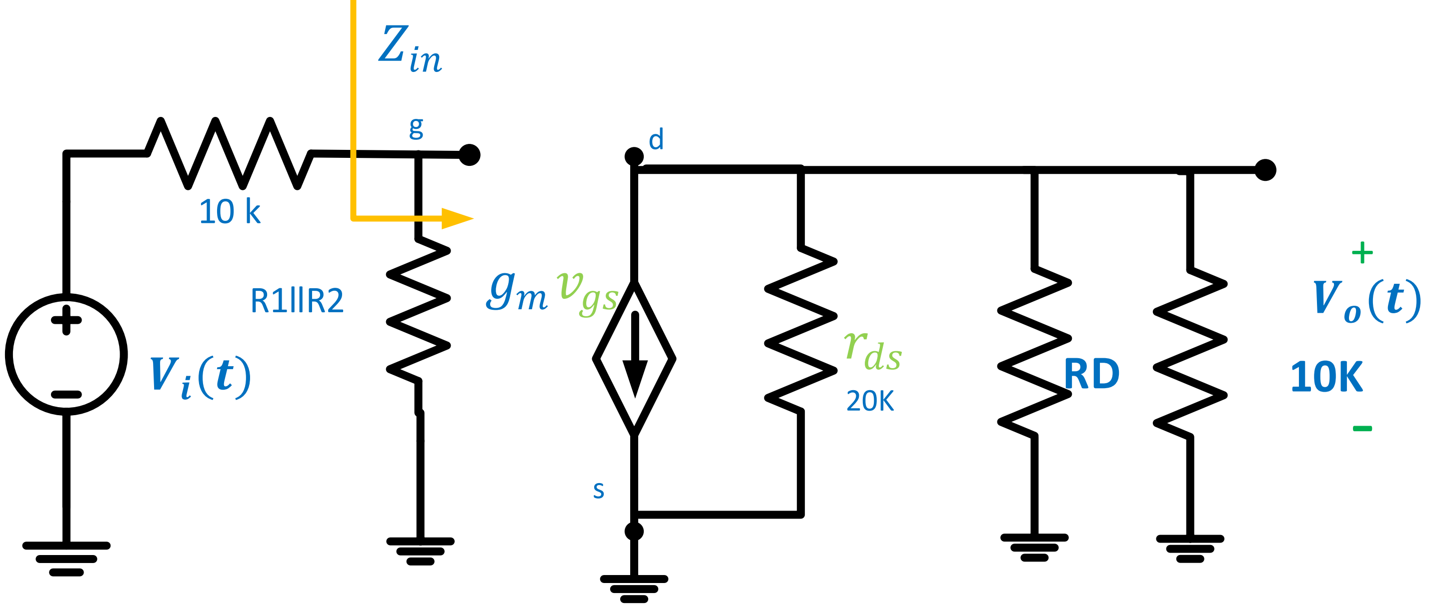
Assume VDD = 24V.

Solution :



Ac small signal equivalent circuit





$$v_O = -\, g_m v_{gs} (R_D \parallel r_{ds} \parallel 10K)$$

$$v_{gs} = v_g - v_S$$

$$vg = \frac{R1//R2}{R1//R2 + Ri} Vi = \frac{Zi}{Zi + Ri} Vi = \frac{1000k}{1000k + 10k} Vi$$

$vg \cong Vi$ $\quad vs = 0$ $\quad \therefore A_v = -\, g_m (R_D \parallel 20K \parallel 10K)$

$$\therefore A_v = -g_m (R_D \parallel 20K \parallel 10K)$$

Using $gm = 2\sqrt{Kn\, IDS}$ → gm = 6.23m℧

For Av = -10 → RD = 2.1KΩ

VDS = 8.7V Pinch off region

DC Analysis

Let VS = VDD/5 = 4.8V → RS = 0.96K Ω

$But \;\; I_{DS} = K_n(V_{GS} - V_T)^2$

$For \;\; I_{DS}$ = 5mA ∴ VGS = 3V

$V_{GS} = V_G - V_S$

∴ VG = 7.8V

NOW

$V_G = \frac{R2}{R2+R1}(24) = 7.8V$

Z_i = R1\\ R2 = 1M Ω

Solving for R1 and R2 , we get

R1 = 3.1M Ω

R2 = 1.48M Ω


THANKS!

