

Faculty of Engineering and Technology

Department of Electrical and Computer Engineering

Digital Electronics and Computer Organization

ENCS 2110

**Experiment No. 1 - Combinational Logic Circuits**

Post Lab1

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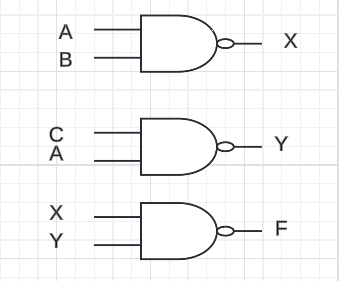
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T.A : Haleema Hmedan

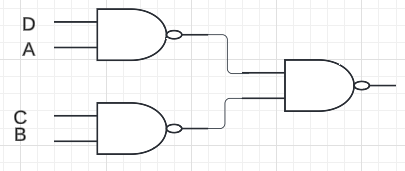
Section : 1

Q1)Draw the logic diagram showing the implementation of the following Boolean equation using “NAND” gates

1. F = AB (CA).

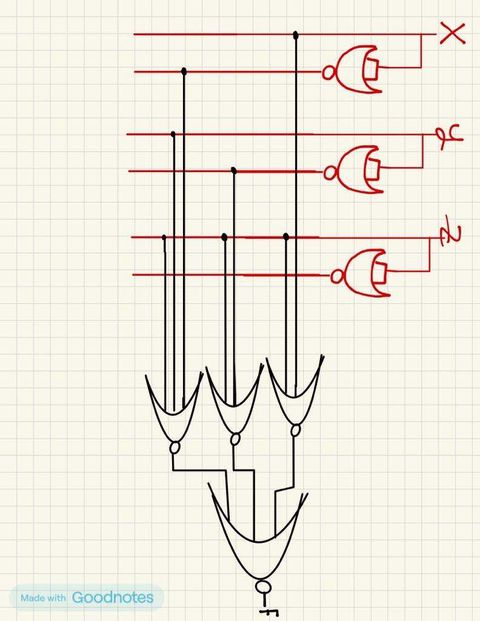


1. F= (D.A) + (C.B)

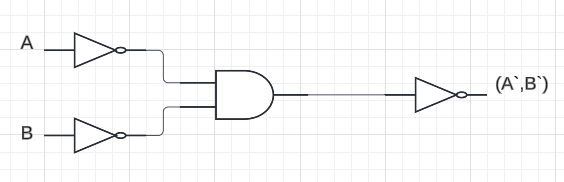


2)Draw the logic diagram of the following Boolean equations using NOR gates.

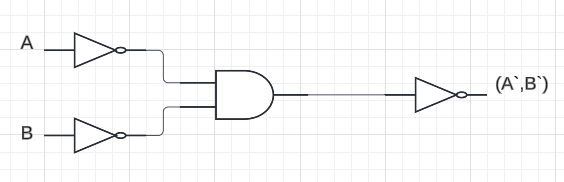
c)F = (X+Z) (Y’+Z) (X’+Y+Z)



Q4) Implement the OR operation using AND, NOT gate. Draw the logic diagram and write the Boolean equation.



Q5) Implement the AND gate using OR, NOT gate. Draw the logic diagram and write the Boolean equation.



Q6) Prove that the equality operation Fl =AB+A’B’ is the inverse of exclusive OR operation

F2=AB’+A’B (use Demerger’s theorem).

Q7)Show how is it possible to reduce Boolean expressions using the Karnaugh map:

a) F1 = A’B’C + ABC’ + A’BC’ + AB’C

b) F2=A’D+A’C+BD+AB’D’

