1. NMOS devices are formed from what type of materials?

NMOS transistors are made of semiconductor material.

2. Source and drain in nMOS device are isolated by what ?

The source and drain regions are formed by diffusing n-type impurity, it gives rise to depletion region which extend in more lightly doped p-region. Thus Source and drain in a nMOS device are isolated by two diodes.

3. The condition for non saturated region?

Vds less that Vgs - Vt, The condition for non saturated region is Vds lesser Vgs – Vt. In non saturation region MOSFET acts as a voltage source. Varying Vds will provide significant change in drain current.

4. As source drain voltage increases, channel depth

a) increases b) decreases c) logarithmically increases d) exponentially increases

As source drain voltage Vds increases, the channel depth at the drain end decreases.

5. Speed power product is measured as the product of switching delay and gate power dissipation is that true?

True, Speed power product is measured in picojoules and it is the product of gate switching delay and gate power dissipation.

6. MOS transistors consists of what layers ?

Metal layer, oxide layer and a semiconductor layer.

7. In MOS transistors,____ is used for their gate

a) metal b) silicon-di-oxide c) polysilicon d) gallium

In MOS transistors, polycrystalline silicon is used for their gate region instead of metal. Polysilicon gates have replaced all other older devices.

8. The gate region consists of what materials?

The gate region is a sandwich consisting of semiconductor layer, an insulating layer and an upper metal layer.

9. Electrical charge flows from where to where in NMOS device?

Electrical charge or current flows from source to drain depending on the charge applied to the gate region.

10. In N channel MOSFET which is the more negative of the elements?

a) source b) gate c) drain

In N channel MOSFET, source is the more negative of the elements and in the case of P channel MOSFET, it is the more positive of the elements.

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11. VLSI technology uses WHAT to form integrated circuit?

Very-large scale integration is the process of creating integrated circuit with thousands of transistors into one single chip.

12. SIlicon-di-oxide is WHAT TYPE OF MATERIALS?

Oxide Material.

SIlicon-di-oxide is a very good insulator so a very thin layer is required in the fabrication of MOS transistors.

13. CMOS technology is used in developing WHAT ?

This technology is used in developing microprocessors, microcontrollers, digital logic circuits and many other integrated circuits.

14. In CMOS fabrication, nMOS and pMOS are integrated in the same substrate. IS THAT TRUE ?

In CMOS fabrication, nMOS and pMOS are integrated in the same chip substrate. n-type and p-type devices are formed in the same structure.

15. P-well is created on ON WHAT KIND OF substrate ?

P-well is created on n substrate to accommodate n-type devices whereas p-type devices are formed in the n-type substrate.

16. Which type of CMOS circuits are good and better?

a) p well b) n well c) all of the mentioned d) none of the mentioned

N-well CMOS circuits are better than p-well CMOS circuits because of lower substrate bias effect.

17. Lithography is Process used to transfer a pattern to a layer on the chip , IS THAT TRUE?

Yes, Lithography is the process used to develop/transfer a pattern to a layer on the chip.

18. When the channel pinches off, Under what condition ?

Happens when drain voltage increases beyond the limit, Vds > Vgs-Vt, >Vgs>Vt

19. When threshold voltage is more, leakage current will be less or more ?

You can see smaller the threshold voltage, the smaller the delay, the larger is the leakage current. On the other hand,you can say that low Vt provides high performance, on the other hand as you increase the threshold voltage; larger is the delay lower is the leakage current.

20. MOSFET can be used as current source or voltage source ? explain

Mosfet acts as a constant current source in the saturation region. This is because, after the Vds is increased to such a level that pinch-off of the channel occurs, the gate and the drain voltages loses the control over the current flowing. That is, beyond that value of Vds, current will be almost constant.

21. Increasing Vsb, How does the threshold voltage change ?

Threshold voltage increases as Vsb increases. The threshold voltage will also vary along the gate. This is called the body effect, or back gate effect

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22. How does Ids change with the length L of the channel ?

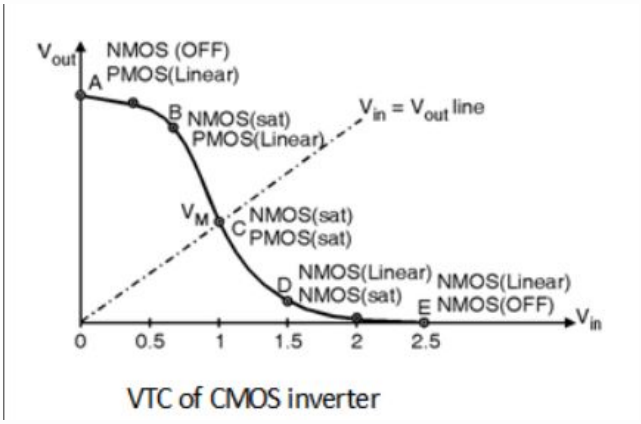
Ids is inversely proportional to the length L of the channel and using this relationship strong dependence of output conductance on channel length can be demonstrated.

23. In basic inverter circuit, is source or drain connected to ground ?

A basic inverter circuit consists of transistors with source connected to ground and a load resistor connected from drain to positive supply rail Vdd.

24. CMOS inverter has 2 regions of operation ,is that true?

No, CMOS has 5 different regions of operations explained in the figure:



VTC of CMOS inverter

25. Which layer has high capacitance value? metal or diffusion?

Diffusion or active layer has high capacitance value due to which it has low or moderate IR drop.

26. Which layer has high resistance value? polysilicon or metal ?

Polysilicon layer has high resistance value and due to this it has high IR drop.

27. Polysilicon is suitable for connecting to VDD or vss grid , is that true ?

Polysilicon is unsuitable for routing Vdd or Vss other than for very small distance because of the relatively high Rs value of the polysilicon layer.

28. Interlayer capacitance occurs due to what ?

Interlayer capacitance occurs due to parallel plate effect between one layer and another. When one capacitance value comes closer to another they create some combined effects.

29. Total wire capacitance is equal to what type of capacitance?

Total wire capacitance can be given as the sum of area capacitance and fringing field capacitance.

30. Overall delay increases as n_____ where n is the number of pass transistors connected in series. increases or decreases?

Overall delay increases as n increases where n is the number of pass transistors connected in series. The overall delay is directly proportional to n^2

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31. Small disturbances of noise how can that affect function of inverter?

Small disturbance of noise switches the inverter stage between 0 and 1 or vice versa. It disturbs the normal operation or behaviour.

32. The overall delay is to the relative resistance r proportional to what?

The overall delay is directly proportional to the relative resistance r. Overall delay is given as the product of (n^2)RCτ.

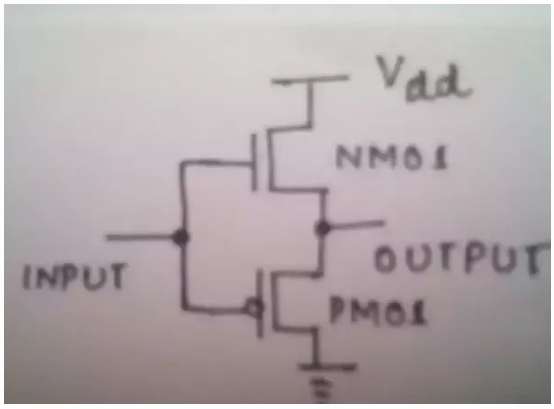
33. Buffer is used for what ?

Buffer is used for long polysilicon runs because it increases the speed and reduces the sensitivity to noise.

34. How is Propagation time proportional to the propagation distance ?

Propagation time is directly proportional to the square of the propagation distance (x^2). It is the time taken by the signal to move from input port to output port.

35. Please explain the reason, why we usually implement the Pull-up network with PMOS and Pull-Down network with NMOS.



Here pull up is nMOS transistor and pull down is pMOS transistor.When logic 1 is applied as input, nMOS transistor turns ON and PMOS transistor turns OFF. Hence, the output should get charged to Vdd. But due to threshold voltage effect, nMOS is not capable of passing Vdd/ good logical 1 at the output. Hence, the output will be Vdd-Vth.When logic 0 is applied as input, nMOS transistor turns OFF and PMOS transistor turns ON. Hence, the output should get discharged to ground level. But due to threshold voltage effect, pMOS is not capable of passing good logical 0 at the output. Hence, the output will be 0-|Vth|.

36. A) ***[T] During the floor planning step the overall cell is defined, including: cell size, supply network, etc.***

[T] If a designer wants a perfectly balanced rise time and fall time for a CMOS inverter driving a capacitive load, Since the mobility of electrons is normally twice the mobility of holes, we need to make the width of PMOS twice as large as the width of NMOS.

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B)Use up to two sentences to explain why PMOS SLOWER THAN NMOS :

holes generally travel more slowly than electrons in IC semiconductors. "higher particle mass for holes than electrons" or "more likely interaction with holes and semiconductor lattice results in higher probability of change in particle direction" the majority carriers in PMOS (holes) are slower than those in NMOS

C) Give one reason for an increase in the complexity of individual design rules with process scaling.

• Bloat. Rule decks have become so large, and the processes so complex, that no one is sure why some rules still exist or how extensive this problem has become. This increases the number of required checks, and it makes debugging more difficult.

• Dependencies. Some rules rely on other rules, which is a growing problem for some foundries at some processes, but not all foundries at all processes.

• Uniqueness. Below 28nm, design rule decks are unique to each foundry. That makes it especially difficult to second-source a design, a problem that is exacerbated by the fact that IP vendors may not support all of the new processes because it's too complicated and time-consuming.

D) Indicate whether each of the following has been increasing (↑) or decreasing (↓) with process scaling for synchronous integrated circuits. If you feel the need to qualify your answer, limit the qualification to three words at most.

(a) Clock frequency: Increase

(b) Power consumption per device per switching event: decrease

(c) Dynamic power consumption as a proportion of total power consumption: increase

(d) tox: except high-k dielectric increase

E) In a misguided attempt to increase the number of usable gates per unit area of IC, a designer has decided to use CMOS only for inverters, and to build all other logic gates using pull-up networks composed of NMOS and pull-down networks composed of PMOS.

(a) How many transistors are required to implement a three-input AND using this design style?
6 transistors

(b) Does the IC have a good chance of implementing the desired logic functions ("Yes" or "No")?
Yes, ignoring the performance of the design.

(c) List two disadvantages of the proposed design style.
Slow. Not full-swing, resulting in reduced noise immunity.

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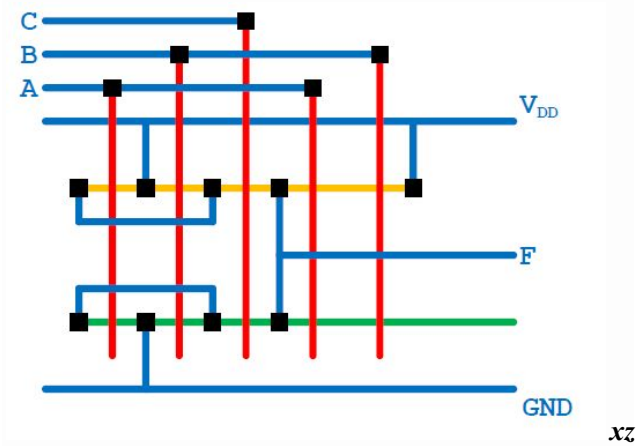
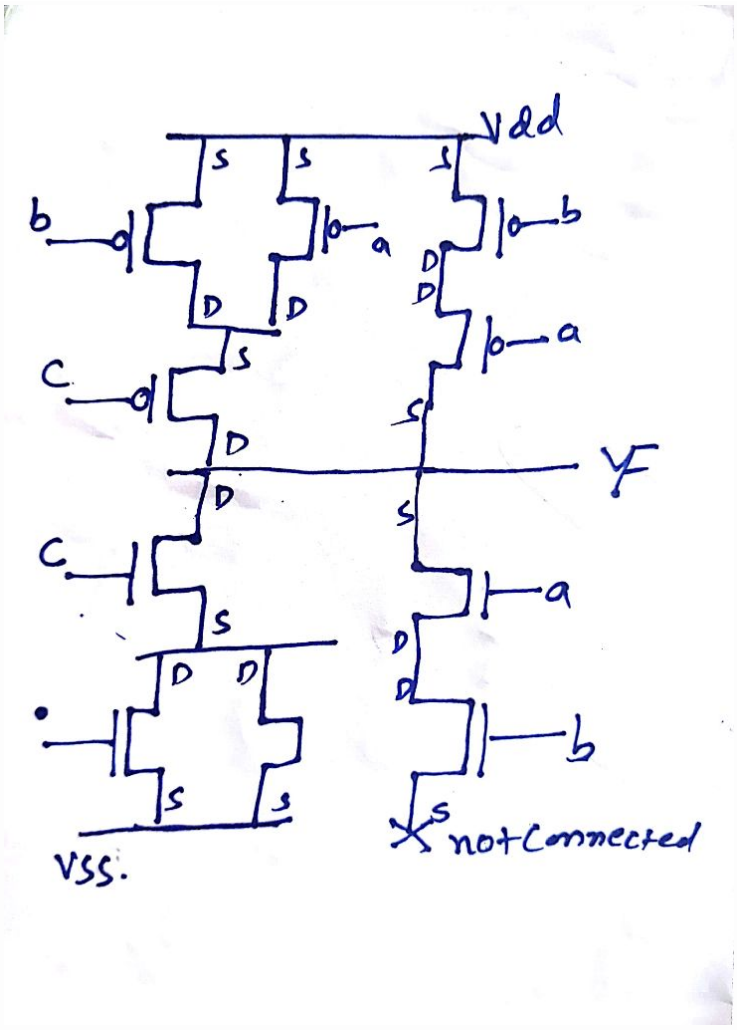
Question2 :Given* function to stick diagram layout *below , derive the schematic



xz



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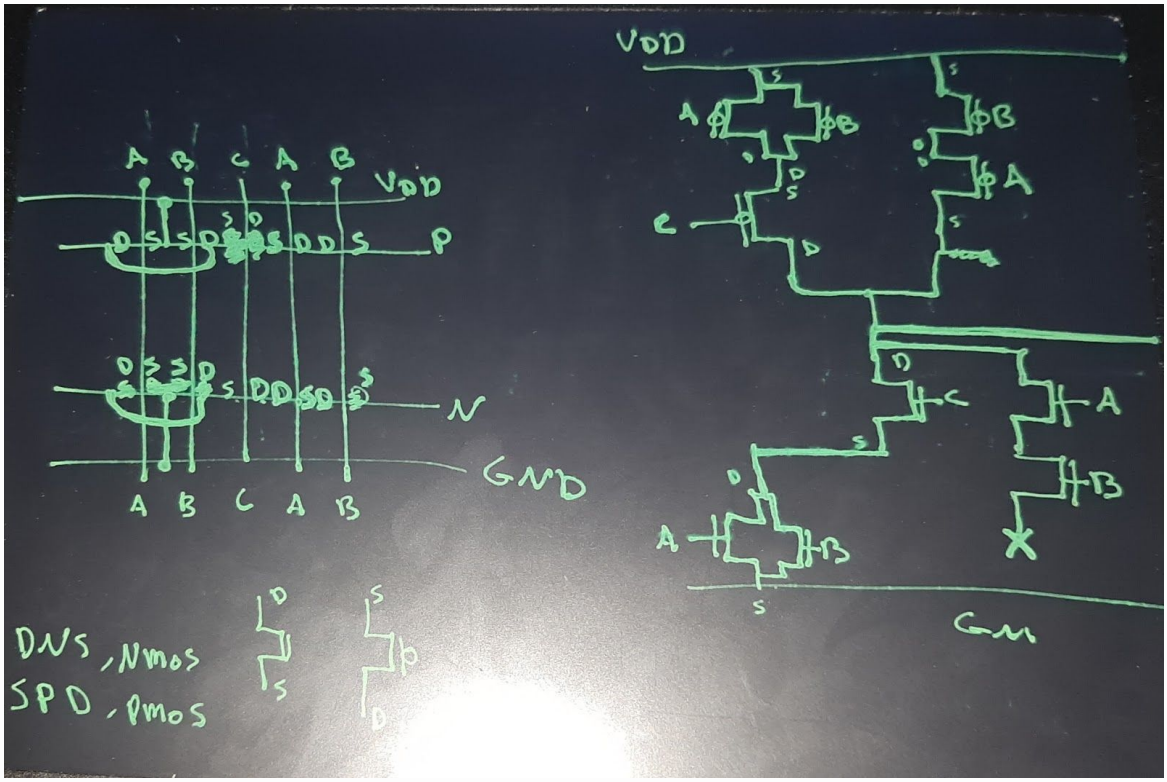
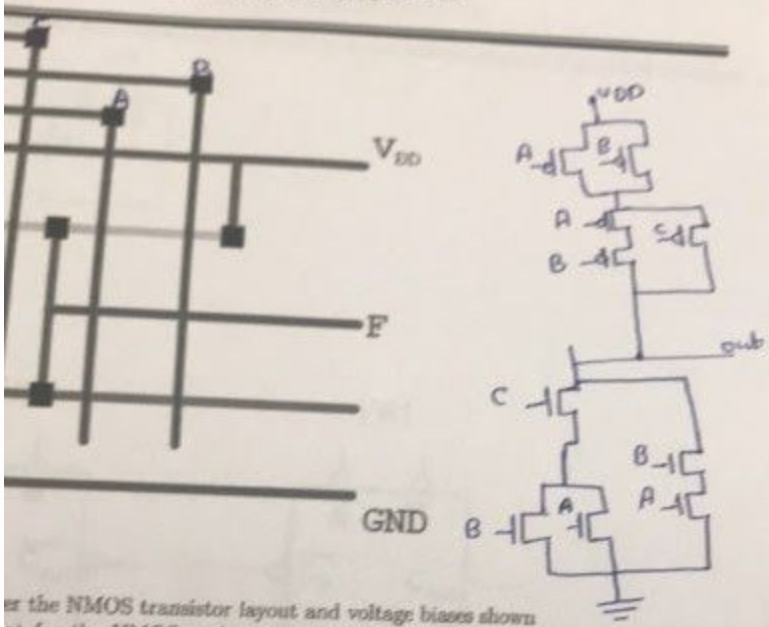


Same as the solution above.



er the NMOS transistor layout and voltage biases shown
st for the NMOS under bias, $V_{T0,n} = 0.3V$, minimum
$.27V^{1/2}$, channel length modulation factor $\lambda = 0\ V^{-1}$,
.6 V. Assume the bulk node of the transistor is at 0V.

$V_s = 0.7$

$V_g = 1.5$

$V_d = 1.8$

$V_b = 0$

$V_{T_0} = 0.3$

$\frac{W}{L} = \frac{9.5}{2} = 4.75$

$V_{ds} = V_d - V_s = 1.1$ volt.

$V_{gs} = 0.8$ volt.

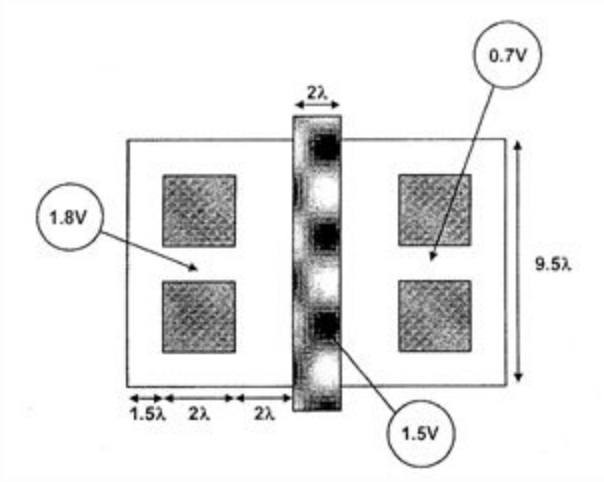
check

$V_{ds} > V_{gs} - V_{t_0}$

$1.1 > 0.8 - 0.3$ ← ⇒ Sat

Problem1.1:

Problem 1.1 (10 points) Consider the NMOS transistor layout and voltage biases shown in Figure 1. Suppose we know that for the NMOS under bias, $V_{T0,n} = 0.3$V, minimum feature size $2\lambda = 2 \times 90$nm, $\gamma = 0.27\text{V}^{1/2}$, channel length modulation factor $\lambda = 0\ \text{V}^{-1}$, $\mu C_{ox} = 299\ \mu\text{A/V}^2$, and $-2\Phi_F = 0.6$ V. Assume the bulk node of the transistor is at 0V. Find the drain-source current I_{DS}.



Solution:

$$I_D = 0 \begin{cases} V_{GS} > V_T \end{cases}$$

$$I_{D,lin} = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T)V_{DS} - V_{DS}^2] \begin{cases} V_{GS} \leqslant V_T \\ V_{DS} > V_{GS} - V_T \end{cases}$$

$$I_{D,sat} = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \begin{cases} V_{GS} \leqslant V_T \\ V_{DS} \leqslant V_{GS} - V_T \end{cases}$$

Vs = 0.7 volts, Vg = 1.5 volts, Vd = 1.8 volts, Vb=0,
Vt0 = 0.3
W/L = 9.5/2 = 4.75
Length: Look at Gate, Width: look at substrate
Vds = Vd-Vs = 1.1 volts

Vgs = 0.8 volts, Vds > Vgs - Vt0 ,, then saturation region. Hence, Apply Formula ID,sat above if it wasn't in saturation use formula ID,lin above

Ids = ½(299) * 4.75 (0.8-0.3)^2 = 177.53125 uA

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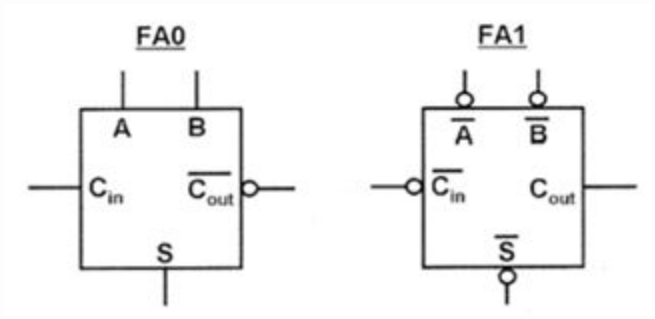
Question 3: Adder design Starts here



Problem 4.1 (**17 points**) Design a **fast** 4 bit ripple-carry adder using the two full adder cells shown in Figure 4 and CMOS inverters. Label the inputs $A[3:0]$, $B[3:0]$, C_{in} and the outputs $S[3:0]$ and C_{out}. Assume the delay through an inverter $t_{INV} = 4$ps, the delay from any input to the full adder carry output is $t_{C\delta} = 7$ps and to the sum output is $t_S = 10$ps. What is the worst case delay through the adder for your design?

Problem 4.4 (**2 points**) Suppose the adder has a total capacitance of 89fF, $V_{DD} = 5$V, and is operated at 1GHz. What is the adder's dynamic power dissipation?

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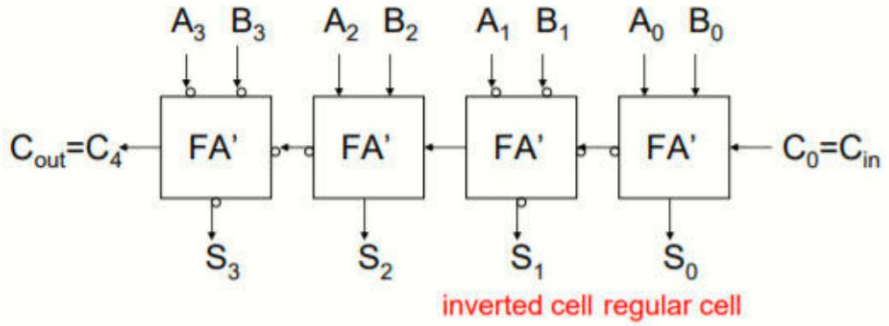
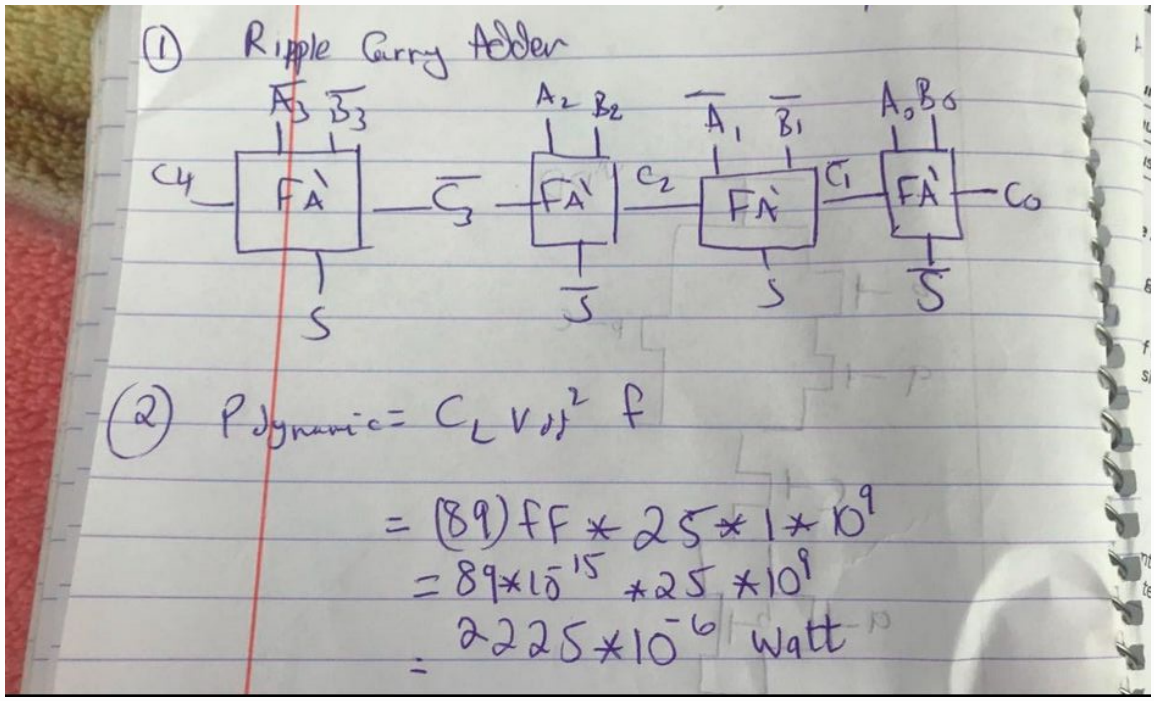
Exploiting the Inversion Property



- Minimizes the critical path (the carry chain) by eliminating inverters between the FAs (will need to increase the transistor sizing on the carry chain portion of the mirror adder).

Now need two "flavors" of FAs



Solution 4.1 + 4.4

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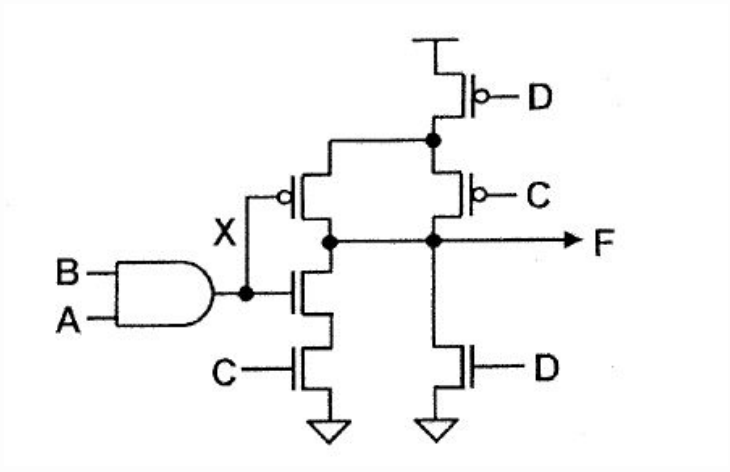
Problem 3.1 (2 points) Write a Boolean expression for the logic function F in terms of inputs A, B, C, and D implemented by the logic gate network in Figure 3.

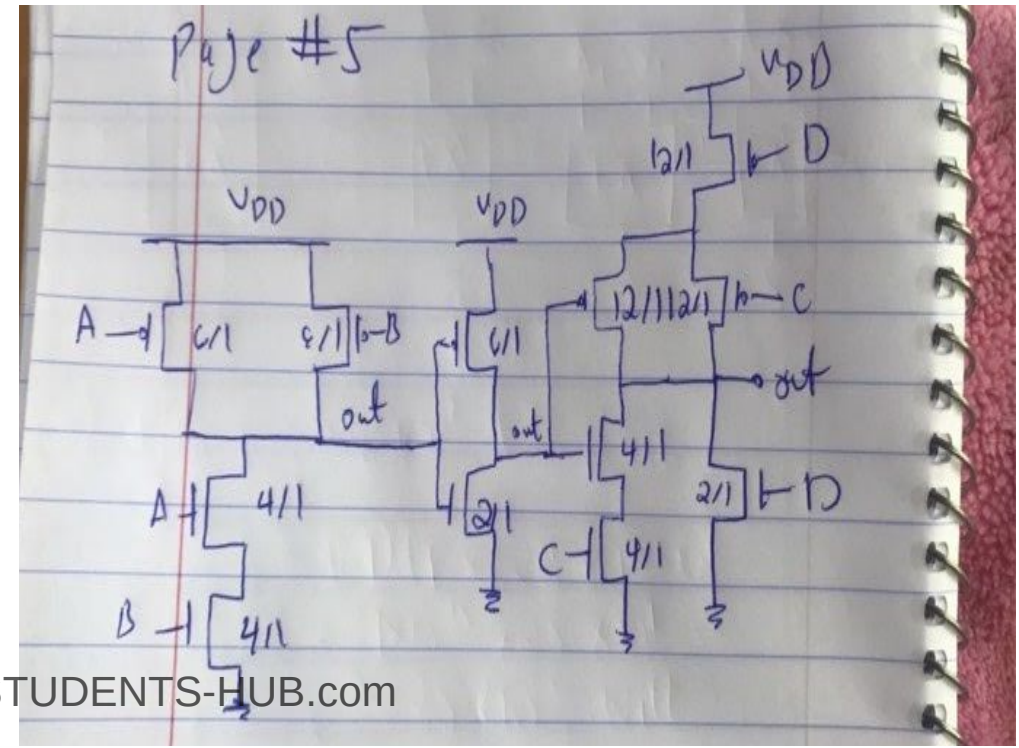


-Solution : F = ((A.B.C)+D)' , To simplify things , assume the AND gate is just an input (A.B)

Problem 3.2 (~~12~~ 10 points) Draw a transistor-level schematic for the circuit in Figure 3 using static CMOS circuits for any logic gates represented by a logic symbol. Be sure to label all inputs, outputs, and other circuit nodes.

AND gate is a 2 input NAND + An inverter.

Replace the first and with its respective NAND+ Inverter CMOS design and keep the rest as is.



Implement the logic function **F = ABD + CD** using a 4-input static **CMOS logic** gate with a **minimum number of** transistors and a single

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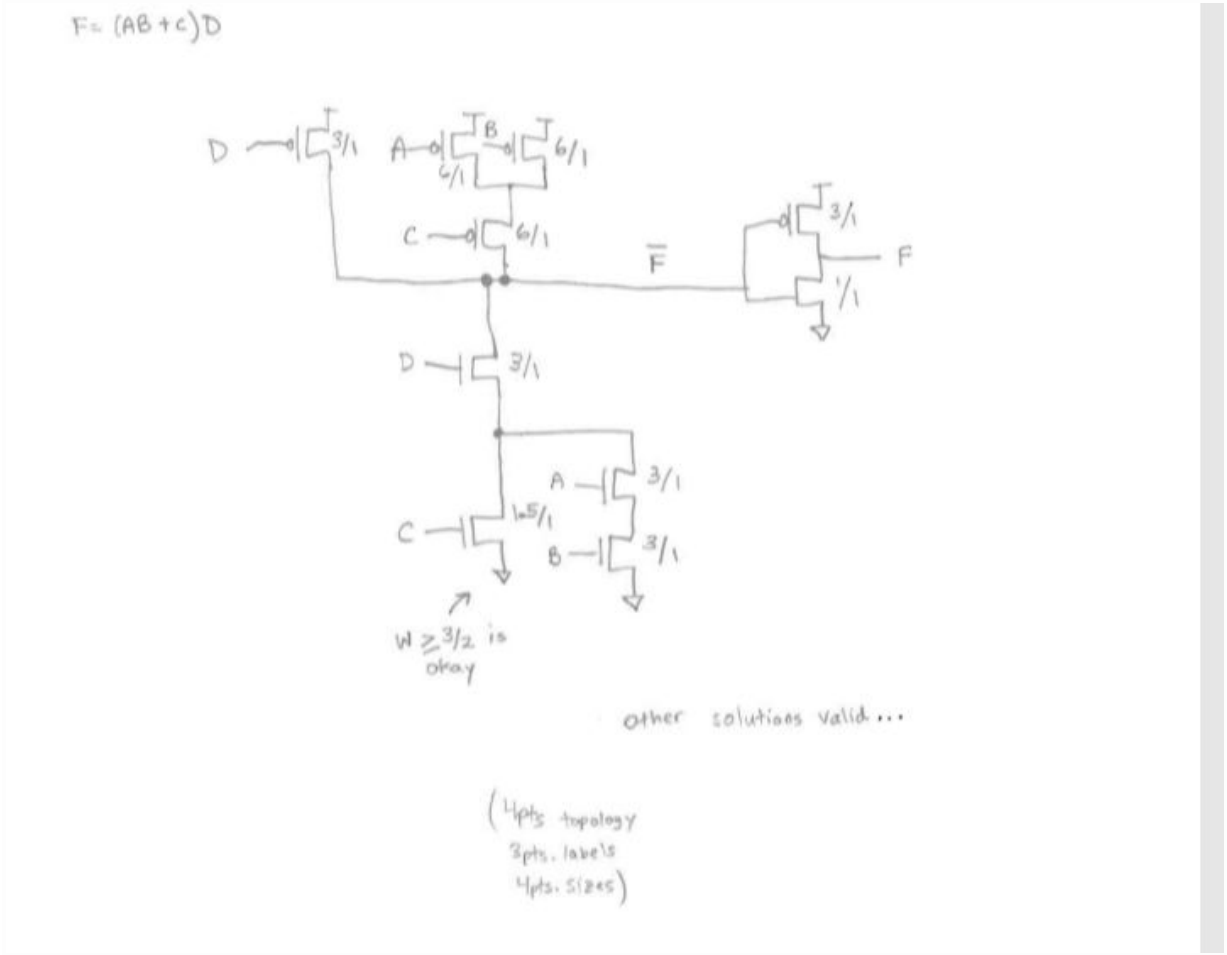
minimum-sized inverter with ratio n/p of (1/3). Size the 4-input gate such that the worst case rise and fall times at its output are equal to the

If Function kept as ABD+CD number of transistors needed will be 10 for circuit + 2 for inverter.

By Grouping D to (AB+C) we removed 2 unneeded transistors.

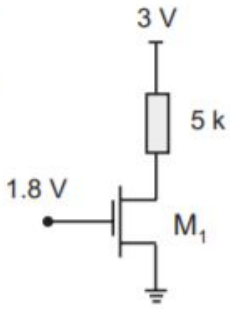


A) **Calculate *ID* and *VDS* if *Kn* = 100 µA/V2, *Vtn* = 0.6 V, and *W/L* = 3 for transistor M1.*(7 points)***

Example 3.2

Calculate I_D and V_{DS} if $K_n = 100\ \mu A/V^2$, $V_{tn} = 0.6$ V, and $W/L = 3$ for transistor M1.

The bias state of M1 is not known so we must initially assume one of the two states, then solve for bias voltages and check for consistency against that transistor bias condition. Initially, assume that the transistor is in the saturated state so that



$$I_D = \frac{\mu\varepsilon_{ox}}{2T_{ox}}\frac{W}{L}(V_{GS} - V_{tn})^2 = K_n\frac{W}{L}(V_{GS} - V_{tn})^2$$
$$= (100\ \mu A)\ (3)\ (1.5 - 0.6)^2$$
$$= 243\mu A$$

Using Kirchhoff's Voltage Law (KVL)

$$V_{DS} = V_{DD} - I_D R$$
$$= 5 - (243\ \text{mA})(15\ \text{k}\Omega)$$
$$= 1.355\,\text{V}$$

We assumed that the transistor was in saturation, so we must check the result to see if that is true. For saturation

$$V_{GS} < V_{DS} + V_{tn}$$
$$1.5\,V < 1.355\,V + 0.6\,V$$

so the transistor is in saturation, and our assumption and answers are correct.

++++++++++++++++++++++++**Question 3 Adder design ends here**

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Question 4

A) Derive the propagation delay of an aluminum wire that is 2 cm long and 500nm wide. Does using a lumped model introduce significant error? You may assume a sheet resistance of 0.075 /2 if needed.

- Since *h* is a constant for a given technology,

$$R = R_{\blacksquare}\frac{l}{w}$$

with

$$R_{\blacksquare} = \frac{\rho}{h}$$

- $R_{\blacksquare}$ the *sheet resistance* of the material in Ω/■

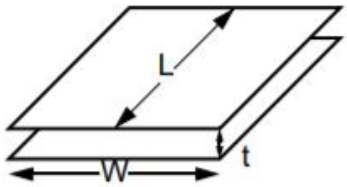
- To obtain the resistance of a wire, simply multiply the sheet resistance by its ratio (*l*/*w*).

R = 0.075*(0.02/500*10^-9) = 3000 ohm

$C = \frac{\varepsilon L * W}{t}$ $\varepsilon = 0.0345 fF/\mu$

Fixed by technology

$C = C_{per\_square\_micron} * W * L$



$$\tau_{Di} = \sum_{k=1}^{N} c_k r_{ik}$$

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B-

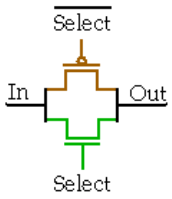
Problem 2.2 (2 points) Suppose the inverter you designed in Problem 2.1 drives a total capacitance of 45fF at 4.1GHz. How much power does it consume assuming $V_{DD} = 5V$?

$P = C V_{DD}^2 f$ (1pt.)

$= (45 \times 10^{-15} F)(5 V)^2 (4.1 \times 10^9 Hz) = \boxed{4.61 mW}$ (1pt.)

A) Construct a schematic (TRANSISTOR LEVEL) for a 2:1 MUX using two CMOS transmission gates and an inverter.

Transmission Gate

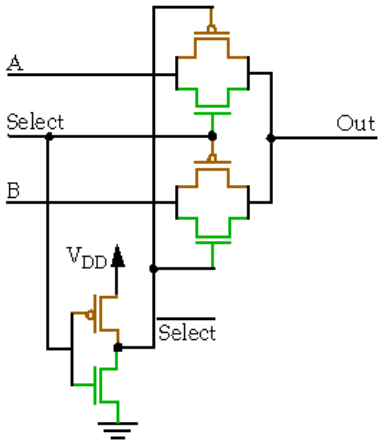


Truth Table for 2-to-1 MUX

Select	Out
0	B
1	A

$Out = A.S + B.\bar{S}$

2-to-1 MUX



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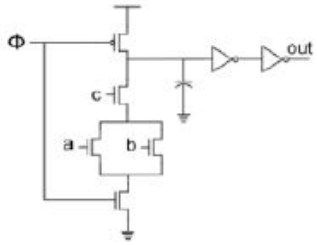
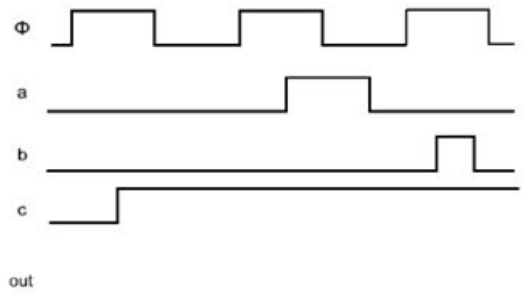
B) Consider the dynamic gate shown in the following figure.

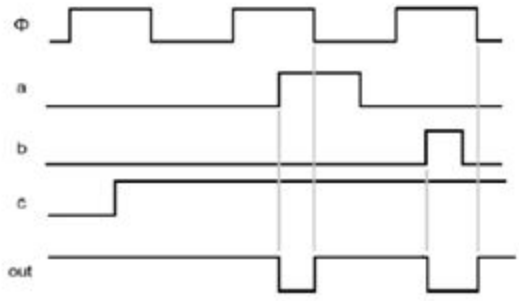


1) What function does this circuit implement?

solved in part 3

2) Based on the input signal, draw the output signal.





3) How can you convert this to STATIC gate , draw the schematic ?

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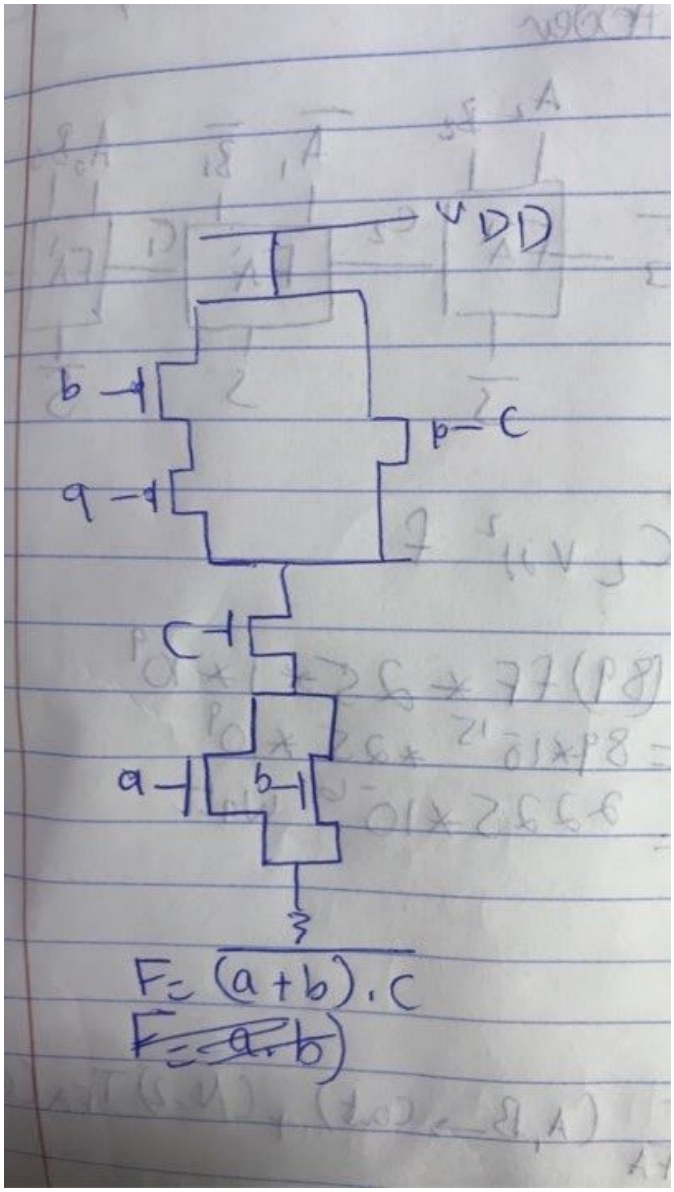

static gate

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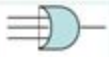
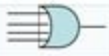
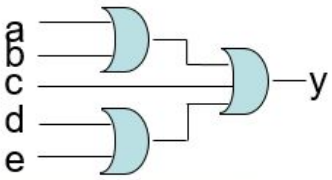
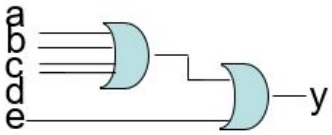
A) Show how you can optimize the design for power given that:

Y= a + b + c + d given that power per cell is given as shown below

Cell	Power
	2
	2.5
	3



Total power:~6



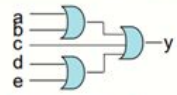
Total power:~5

Main Optimization Trade-Offs

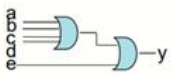
- Circuit design is a trade-off of timing, power and area
- Timing optimization
  - Goal: small delays
- Power optimization
  - Goal: low power consumption
- Area optimization
  - Goal: small area

Cell	Power
	2
	2.5
	3

Same function: Y=a+b+c+d



Total power:~6



Total power:~5

B) Explain the difference between latch and FF ?

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Latches	Flip Flops
Latches are building blocks of sequential circuits and these can be built from logic gates	Flip flops are also building blocks oof sequential circuits. But, these can be built from the latches.
Latch continuously checks its inputs and changes its output correspondingly.	Flip flop continuously checks its inputs and changes its output correspondingly only at times determined by clocking signal
The latch is sensitive to the duration of the pulse and can send or receive the data when the switch is on	Flipflop is sensitive to a signal change. They can transfer data only at the single instant and data cannot be changed until next signal change. Flip flops are used as a register.
It is based on the enable function input	It works on the basis of clock pulses
It is a level triggered, it means that the output of the present state and input of the next state depends on the level that is binary input 1 or 0.	It is an edge triggered, it means that the output and the next state input changes when there is a change in clock pulse whether it may a +ve or -ve clock pulse.

C)What do we mean by Transparency? Does it affect latch based design or FF based design?

Transparency Window

• The time when a data input flows unblocked through a sequential

Inputs may switch anytime in this window, so long as they are valid before the capturing edge of the clock, and remain valid until the hold time (+ skew)

Transparency reduces the impact of clock uncertainty

• If the opening clock edge is early, the valid time at the output of the latch for a transparent path is unchanged

• If the opening clock edge is late, but not as late as the transparent data, the valid time at the output is unchanged

• As long as the data is switching somewhere in the middle of the transparency window, the clock has no impact on the timing through this latch

-Level sensitive latches allow transparency

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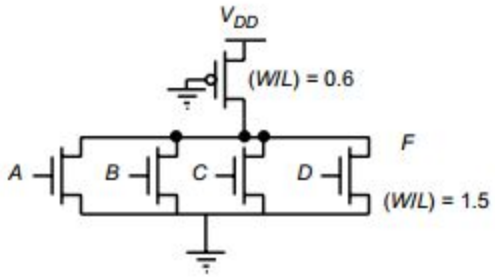
• When the latch opens, data may arrive and pass freely from input to output without waiting for clock

• Data only needs to be stable when the latch closes

D) For the circuit below, what is the output voltage if only one input is high? If all four inputs are high? Explain your answer.



a) What is the output voltage if only one input is high? If all four inputs are high?

Solution

$$I_D = K' \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{min} - \frac{V_{min}^2}{2} \right) \cdot (1 + \lambda \cdot V_{DS})$$

Consider a case when one input is high: A = V_{DD} and B = C = D = 0 V. Assume that V_{out} is small enough that $V_{min} = V_{DSAT}$ for the PMOS device, and $V_{min} = V_{DS} = V_{out}$ for the NMOS devices. Solve for V_{out} by setting the drain currents in the PMOS and NMOS equal to each other, $|I_{DP}| = |I_{DN}|$, where the drain currents are functions of V_{out}, V_{DD}, and the device parameters.

V_{out} = 102 mV, and I_D = 35.7 µA.

Now verify that the assumptions for V_{min} are correct. For the PMOS: V_{DS} = -2.34 V, V_{DSAT} = -1 V, V_{GT} = -2.1 V, therefore $V_{min} = V_{DSAT}$. For the NMOS: V_{DS} = 102mV, V_{DSAT} = 630mV, V_{GT} = 2.07 V, therefore $V_{min} = V_{DS}$.

Consider the case when all inputs are high: A = B = C = D = V_{DD}. For these hand calculations, this is numerically equivalent to a circuit with a single NMOS device with W/L = 4*1.5 and its gate tied to V_{DD}. Now, the analysis used above for the case when one device is on can be reused, replacing W/L of the NMOS with 6, and using the same assumptions for V_{min}. V_{out} = 25 mV, and I_D = 35.9 µA. The assumptions for V_{min} are correct.

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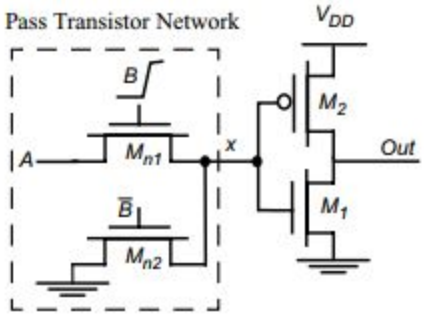
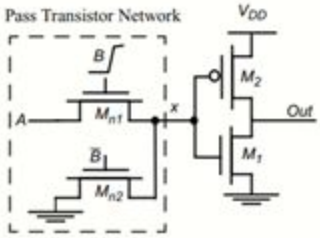
A) Explain why this circuit has non-zero static power dissipation.
Using only 1 transistor, design a fix so that there will not be any static power dissipation.
Explain how you chose the size of the transistor.



Problem 4: Pass Transistor Logic and Level Restoration

Consider the circuit of Figure 0.3. Assume the inverter switches ideally at $V_{DD}/2$, neglect body effect, channel length modulation and all parasitic capacitance throughout this problem.



$V_{DD} = 2.5V$
$(W/L)_2 = 1.5um/0.25um$
$(W/L)_1 = 0.5um/0.25um$
$(W/L)_{ni} = 0.5um/0.25um$

$k_n' = 115uA/V^2$, $kp' = -30uA/V^2$
$V_{tN} = 0.43V$, $V_{tP} = -0.4V$

Figure 0.3 Level restoring circuit.

a) What is the logic function performed by this circuit?

Solution

The circuit is a NAND gate.

b) Explain why this circuit has non-zero static dissipation.

Solution

When A=B= V_{DD}, the voltage at node x is $V_X=V_{DD}-V_{tN}$. This causes static power dissipation at the inverter the pass transistor network is driving.

c) Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.

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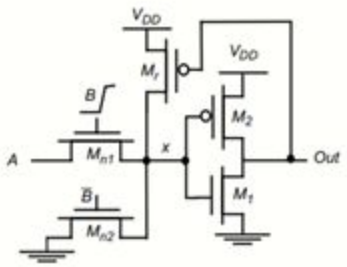
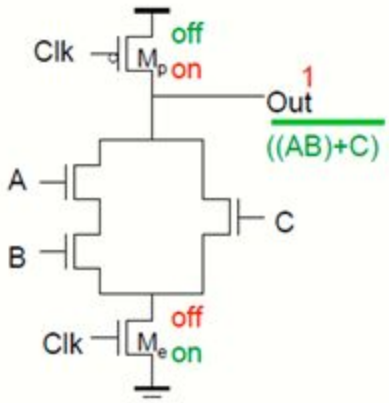
The modified circuit is shown in the next figure



The size of M_r should be chosen so that when one of the inputs A or B equals 0, either M_{n1} or M_{n2}, would be able to pull node X to $V_{DD}/2$ or less.

Question 5: (20 points)

A) Draw dynamic logic gates for F= $\overline{((AB)+C)}$ **(2 points)**



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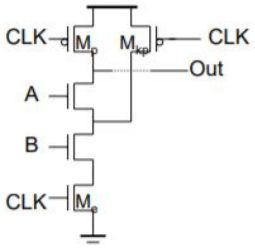
B) What are the main Issues in Dynamic Design and how we can fix/avoid? (3 points)

Charge leakage and charge distribution or sharing. Fix: keeper for leakage and precharge internal nodes using a clock driven transistor

1. **Charge leakage, we can fix it by using a keeper that compensates for the charge lost due to the pull-down leakage paths.**
2. **Charge sharing, solution:**

Solution to Charge Redistribution



Precharge internal nodes using a clock-driven transistor (at the cost of increased area and power)

3. **Backgate coupling**
4. **Clock feedthrough**

C) Define:

For latch:

- Setup time
  - Time, before the latch closes, that the data must arrive to guarantee the data is captured correctly after the latch closes
- Hold time
  - Time, after the latch closes, that the data can not switch to guarantee the data is captured correctly when the latch closes
- Clk to out delay
  - Delay from clk to out when the data is setup before the clk
- Data to out delay
  - Delay from data to out when the data arrives after the clk

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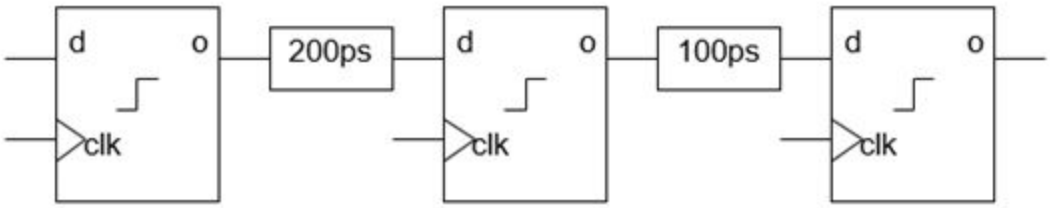
For FF:

Flip-flop parameters

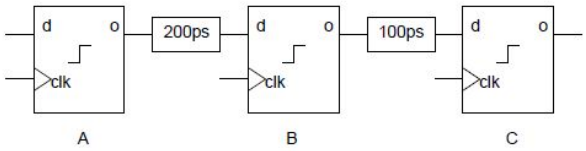
- Setup time
  - Time, before the opening clk edge, that the data must arrive to guarantee the data is captured correctly
- Hold time
  - Time, after the clk edge, that the data can not switch to guarantee the data is captured correctly
- Clk to out delay
  - Delay from clk to out when the data is setup before the clk.
- Note that there is no data to out delay since flops must have data setup to the edge.

D)Based on the figure below, Assuming 100ps setup time, skew and clk-out delay



Flop Answers

- 2 paths (A->B and B->C) each 1 cycle
- 200ps + 100ps = 300ps. 1/300ps = 3.33GHz
- 100ps + 100ps = 200ps. 1/200ps = 5.0GHz
- Max frequency = 3.33GHz



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• **What are the advantage of time borrowing? How can we benefit of time borrowing in this question?**

Time borrowing is a technique to increase frequency by converting flops to latches. • Allows amortizing skew, jitter, clk to out and data delays across more than 1 cycle

Positives: • Allows some amount of time borrowing without some of the negative of time borrowing

• Very little extra clock load • No latch explosion • No RTL change •

Negatives: • Only allows only a buffer delay of borrowing • Min delay of the first path has been worsened by 1 buffer delay. • Skew has increased

2 advantages of time borrowing

• Allows "borrowing" time from a cycle that has extra margin to a cycle that doesn't in our example, the cycle that ran at 3.33GHz borrows time from the cycle that had 5GHz

• Allows amortization of setup time and skew over several cycles

In our example, the 100ps overhead penalty is now over 2 cycles so the per cycle penalty is 50ps

And we can turn the flop in the middle into two latches making 6 paths

Question 6

A) What are the two line model? (2 points)

1)lumped: not very accurate , cap at the end of the line , pessimistic

2)distributed: many lumped lines on one distributed line , more accurate

B) Why and where we use repeaters? (3 points)

To break lengthy high metal routes into segments, also assist routes not get into slopes and noise issues, with different sizes we can minimize the delay.

Connected to transistor layers, grouped in percolated repeater boxes spread around the chip

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E) What is Coupling Capacitance? Which of the below figures have bigger coupling caps? (4 points)

A coupling capacitor is a capacitor which is used to couple or link together only the AC signal from one circuit element to another. The capacitor blocks the DC signal from entering the second element and, thus, only passes the AC signal.

F)

1. Given the RC network below:

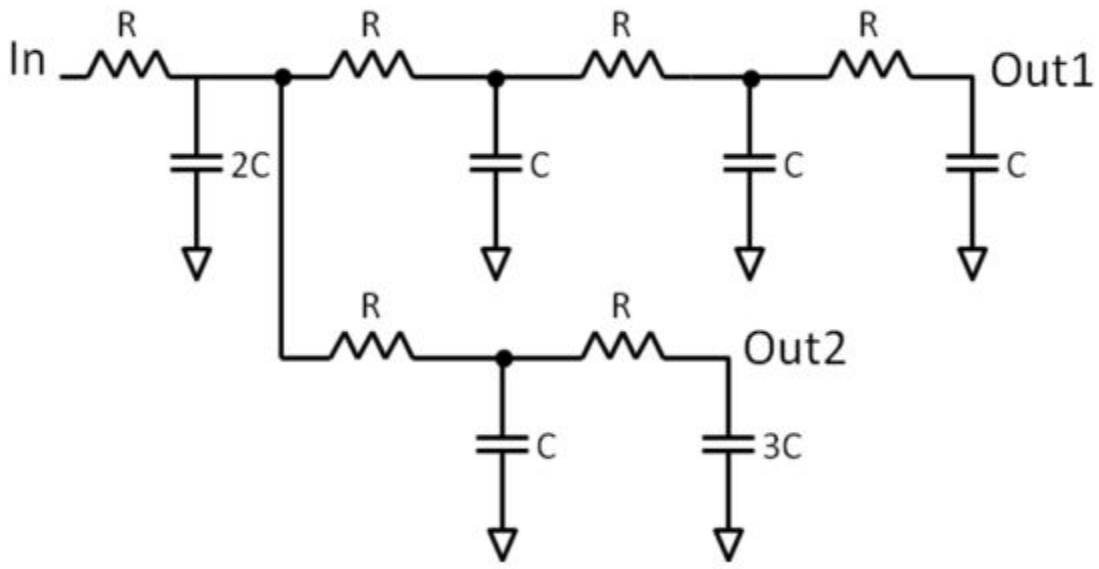

Figure 1 RC network.

(1) Calculate the Elmore delay from In to Out1 and from In to Out2. Which one is critical path? (10 pts)
(2) Assume R = 100Ω and C = 10fF. Calculate the Elmore delay of the critical path you find in part (1) and verify the result using Spectre. (10 pts)

Solution:

(1) From In to Out1:

$$\tau_1 = R \cdot (2C + C + 3C) + 2RC + 3RC + 4RC = 15RC$$

From In to Out2:

$$\tau_2 = R \cdot (2C + C + C + C) + 2RC + 3R \cdot 3C + 4RC = 16RC$$

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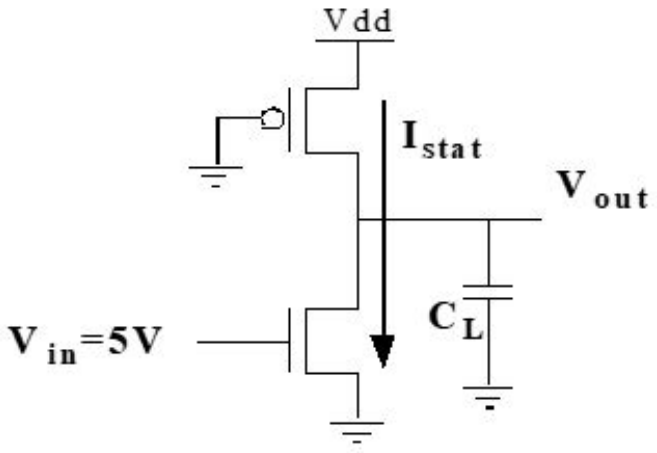
Critical path is 16RC from in to out2 ,Elmore Delay = 16*100*10fF= 16*100*10*10^-15= (1.6*10^-11) second

A) What kind of power dissipation in each circuit below : (3 points)



Pstatic = P(in=1)*Istatic * Vdd

B) What type of power we define as $P = \alpha f C V_{DD}^2$ **: what does each factor represent and how it affect the power ? (3 points)**

This is total power dissipation

Alfa= signal transition switching activity

F=operating frequency of the bus

C=load capacitance of the wire line

Vdd= swing voltage

Reduce all to reduce power in the bus.

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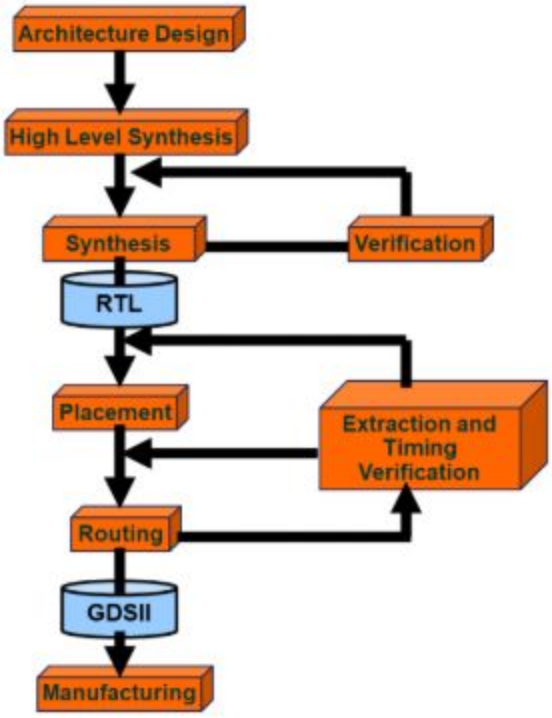
A) Complete the missing block name from the level design flow for chip/IC (6 points)



B) The transistor current changes with the operating temperature mainly through the mobility and Vt temperature dependencies. Explain how does temperature affect the

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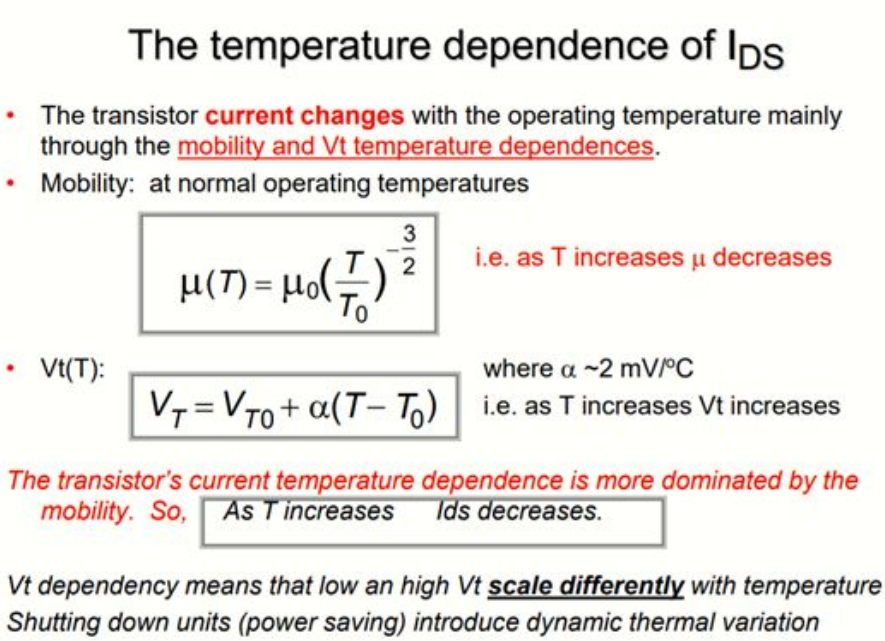
current ? (2 points)



C) When the hot-e happen (which region of operation) and how we can avoid it?

When a MOS transistor is in saturation, the electric field across the pinch-off region may be high enough that carriers gain enough energy to excite electron-hole pairs.

How to reduce the hot-e degradation?

- **Decrease C_{load} (reduce fanout).**
- **Speed up the input edge rate.**
- **Avoid slowly varying output signals where possible.**
- **Increase Width of NMOS.**
- **Use NAND gates if possible (or gates with NMOS in series).**
- **Increase NMOS channel length.**
- **Avoid false transitions (glitches) - reduce the real AF.**
- **Avoid capacitive coupling above Vcc (overshoots).**

D) What are the main three Physical Synthesis Steps?

Physical synthesis is the process that produces layout of logic circuit.

- **Floorplanning: During the floorplanning step the overall cell is defined, including: cell size, supply network, etc.**
- **Placement: Placement – exact placement of modules (modules can be standard cells, IPs)**
- **The goal is to minimize the total area and interconnect length**
- **Routing: Routing connects placed cells according to schematic • the goal is minimal impact of interconnects on circuit operation**

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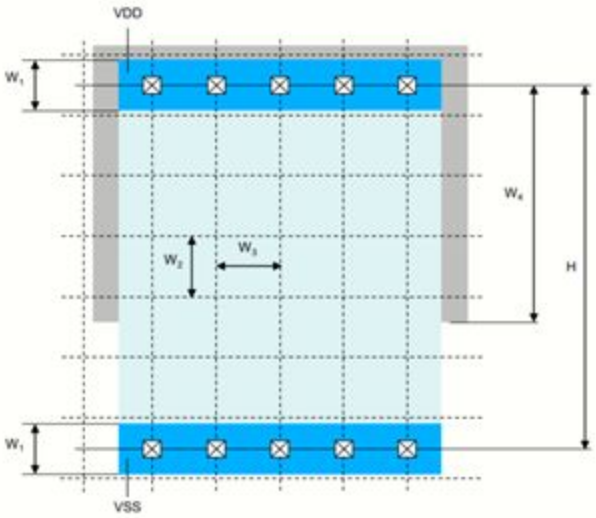
E) Is it true that all clock pins are driven by a single clock source for the same chip? If yes/no explain why? (2 points)

Yes, All clock pins are driven by a single clock source, Physical synthesis not only places and routes the cells of a circuit but also optimizes the cell as required by the designer, so we phy. Syn. Implements A buffer tree is built to balance the loads and minimize the delays

F) Given that the physical structure for standard cell design is shown below, match or mark the following parameters to the cell (5 points)



Parameter	Symbol
Cell height	H
Power rail width	W_1
Vertical grid	W_2
Horizontal grid	W_3
N-Well height	W_4

Qustion3

A.*Point +++out what kind of DRC errors in the below examples: (3 points*)

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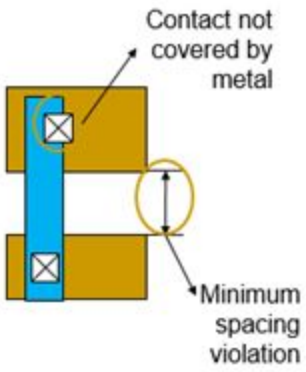

B. What type of logic function does this layout implement? Point out the three largest problems with this layout. For each explain the impact on gate behavior.(5 POINTS)

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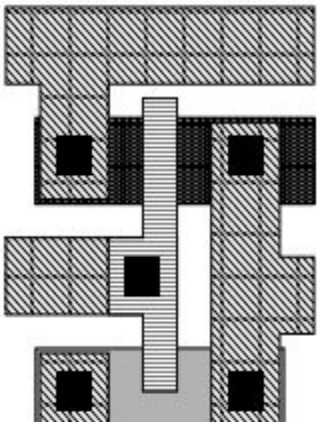
(8 pts.) Point out the three largest problems with this layout. For each explain the pact on gate behavior. When possible, indicate the ways in which important parame are influenced, e.g., k'.

i. The bottom half of the NMOSFET gate is missing.
ii. The PMOSFET drain is bigger than it needs to be, increasing capacitance without benefit.
iii. The NMOSFET and PMOSFET active regions are the same width, which would result in asymmetric pull-up and pull-down resistances if the gates were designed correctly.



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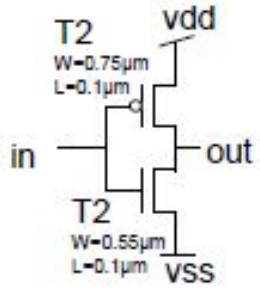
B) Below is text-based format so is readable and can be easily modified. Draw the schematic level of this text spice netlist.

```
.subckt test
        mt1 out in vss nmos l = 0.1u w = 0.75u
        mt2 out in vdd pmos l = 0.1u w = 0.55u
.ends
```

SPICE Description Example

- SPICE is a hardware description language (HDL) which enables to describe circuit at device level
- It has text-based format so is readable and can be easily modified



Inverter.sp

```
.subckt inverter
        mt1 out in vdd nmos l = 0.1u w = 0.75u
        mt2 out in vdd pmos l = 0.1u w = 0.55u
.ends
```

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5 Latch

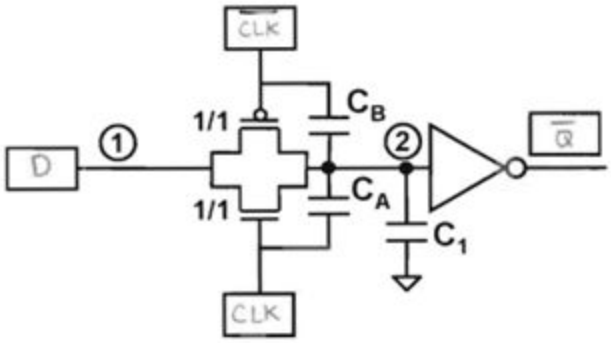

Figure 5: Latch schematic.

Problem 5.1 (**4 points**) For the latch circuit shown in Figure 5, label the boxes D, CLK, $\overline{CLK}$, $\overline{Q}$ such that the circuit works as a **positive transparent** inverting latch.

Problem 5.2 (**2 points**) Is the circuit in Figure 5 a static or dynamic latch (circle one)? Justify your answer.

- Static
- Dynamic — No positive feedback, logic level stored as capacitor charge.

Problem 5.3 (**6 points**) Suppose the latch is used as the slave stage of an edge-triggered flip-flop and that node 1 and node 2 in Figure 5 are initially at 1.8V and 0V, respectively. Assuming $R_p = 300\Omega$ for a PMOS device with $W/L = 1/1$ and $R_n = 100\Omega$ for an NMOS device with $W/L = 1/1$, $C_A = 19$fF, $C_B = 23$fF, $C_1 = 150$fF, and t_{pHL} for the inverter is 8.9ps, estimate the clock-to-Q delay for the latch using the switch RC model for the transistors.

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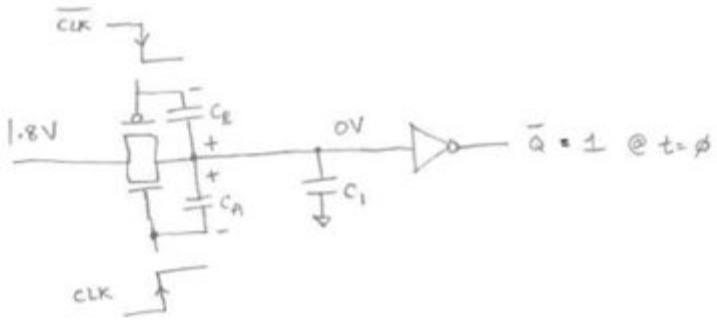
Problem 5.3 (cont.)

$t_{C\to Q}$: when CLK goes high, D propagates to output $\overline{Q}$



$R_{eq} = R_n \| R_p = 100\Omega \| 300\Omega = 75\Omega$

$t_{C\to Q} = 0.69\, R_{eq}\, C_{TOT} + t_{pHL}$

ΔV for $C_B = 1.8V - (-1.8V) = 3.6V$ ← Miller effect

ΔV for $C_1 = 1.8V - 0V = 1.8V$

ΔV for $C_A = 0V - 0V = 0V$ ← ignore C_A's contribution to delay

$C_{TOT} = C_1 + 2C_B = 150\,fF + 2\cdot 23\,fF = 196\,fF$

$t_{C\to Q} = 0.69 \cdot 75\Omega \cdot 196\,fF + 8.9\,ps$

$\boxed{t_{C\to Q} = 19.043\,ps}$

$C_{TOT} = C_1 + C_A + C_B = 192\,fF \Rightarrow t_{C\to Q} = 18.836\,ps$

$C_{TOT} = C_1 + 2\cdot(C_A + C_B) = 234\,fF \Rightarrow t_{C\to Q} = 21.01\,ps$

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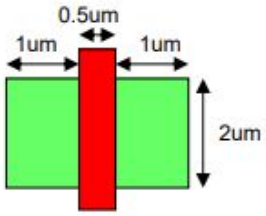
Problem 5

The simplified layout of a pMOS transistor in a 0.5µm process is shown here with the "actual" fabricated dimensions. Determine the device parasitics below using the following process model values:

$k'p = 90\mu A/V^2$, $|Vtp| = 0.5V$, $Cox = 1.8fF/\mu m^2$, $Cj = 0.75fF/\mu m^2$

and $Cjsw = 0.25\ fF/\mu m$



a) What is the gate capacitance, C_G?
b) What is the gate-to-drain capacitance, C_{GD}?
c) What is the drain-to-bulk capacitance, C_{DB}?
d) What is the total capacitance at the drain node?
e) If the drain node RC time constant is 4psec, what is channel resistance?

solution:

a) $C_G = Cox\ (W\ L) = (1.8fF/\mu m^2)\ (2\mu m)\ (0.5\mu m) =$ **1.8fF**

b) $C_{GD} = \frac{1}{2}\ C_G = \frac{1}{2}\ (2f) =$ **0.9fF**

c) $C_{DB} = C_j\ A_{Dbot} + Cjsw\ P_{DSW}$

$A_{Dbot} = 2\mu m \times 1\mu m = 2\mu m^2$

$P_{DSW} = 2\ (2\mu m + 1\mu m) = 6\mu m$

$C_{DB} = C_j\ A_{Dbot} + Cjsw\ P_{DSW} = 0.75f\ (2) + 0.25f\ (6) =$ **3fF**

d) Total capacitance at the drain node is

$C_D = C_{GD} + C_{DB} = 0.9 + 3 =$ **3.9fF**

e) $\tau = Rn\ C_D \rightarrow Rn = \tau / C_D = 4p/3.9f =$ **1,025 Ω**

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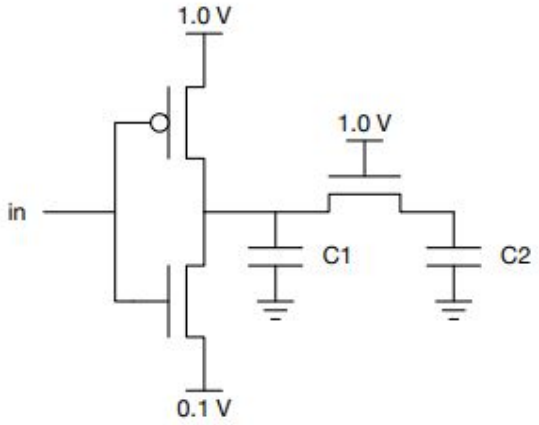
Given the circuit below, answer the following questions. Assume that the capacitances associated with the FETs are negligible.

$C_1 = C_2 = 90fF$

$V_{th,n} = |V_{th,p}| = 0.4V$



Part a

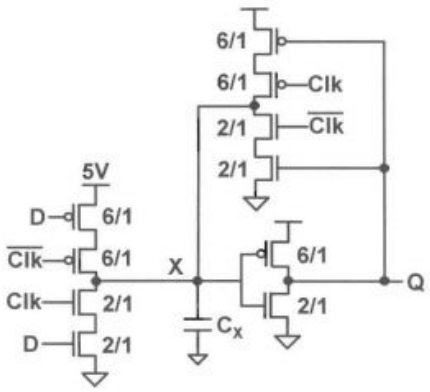
How much energy is stored in each capacitor after a 1V to 0V transition on `in`? Please show your work.

$E_1 = \frac{1}{2} \cdot C_1 \cdot V_1^2 = \frac{1}{2} \cdot 90fF \cdot (V_{DD})^2 = \frac{1}{2} \cdot 90fF \cdot (1.0V)^2 = 45.0fJ$

$E_2 = \frac{1}{2} \cdot C_2 \cdot V_2^2 = \frac{1}{2} \cdot 90fF \cdot (V_{DD} - V_{th,n})^2 = \frac{1}{2} \cdot 90fF \cdot (0.6V)^2 = 16.2fJ$

What kind of circuit is the circuit below? is it dynamic or static circuit ? is it a latch or a ff ?(3 points)

Answer: Static positive edge latch



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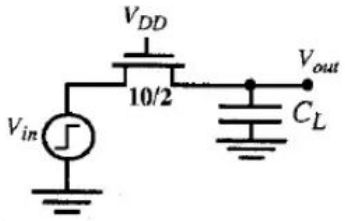
Problem 1: Static and dynamic analysis Total: 15

Consider the following logic circuit:



a. Assume that $V_{out}(t = 0) = 0$ V. Determine V_{out} (t = ∞) when V_{in} is raised from 0 V to V_{DD} at $t = 0$. Assume $V_{DD} = 3$ V. You may assume that $L = L_{eff}$, or that the lateral diffusion can be ignored in this problem.

$V_{out}(t=\infty) = V_{DD} - V_T(V_{out})$

$= 3 - (0.7 + 0.5(\sqrt{V_{0.7}+V_{out}} - \sqrt{0.6}))$

Iterate for solution

$V_{out}(t=\infty)$: 1.89V

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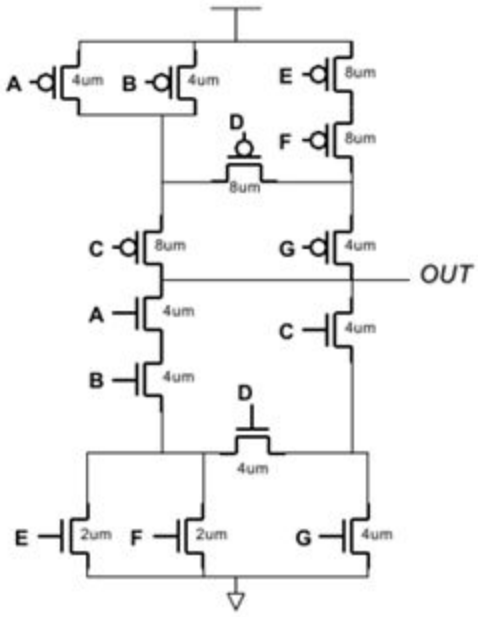
A) What is the function of the figure below ? F prime=A.B(F+E)+ABDG+CG+CD(F+E)



Explanation :

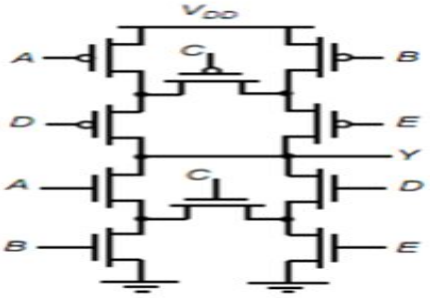
The picture below shows the logic function of a similar case. If we looked carefully and analyzed the Pull-Down network. We can assume transistors A,B connected in series as one transistor lets call it x and transistors E,F connected in parallel as one transistor let's call it y. The resulting logic equation will be (XY + XDG+CG+CDY), substituting the values of both X and Y. we get

F` = AB.(E+F) + ABDG + CG + CD(F+E) which is the result.

Note: To make it easier to remember do (and) between the two transistors on the left side(AB) then (and) across the diagonal(ACE) to the right then do (and) between the two on the right(DE) then return diagonally again.(DCB).

$$\overline{f} = (A \cdot B) + (A \cdot C \cdot E) + (D \cdot E) + (D \cdot C \cdot B)$$

tion



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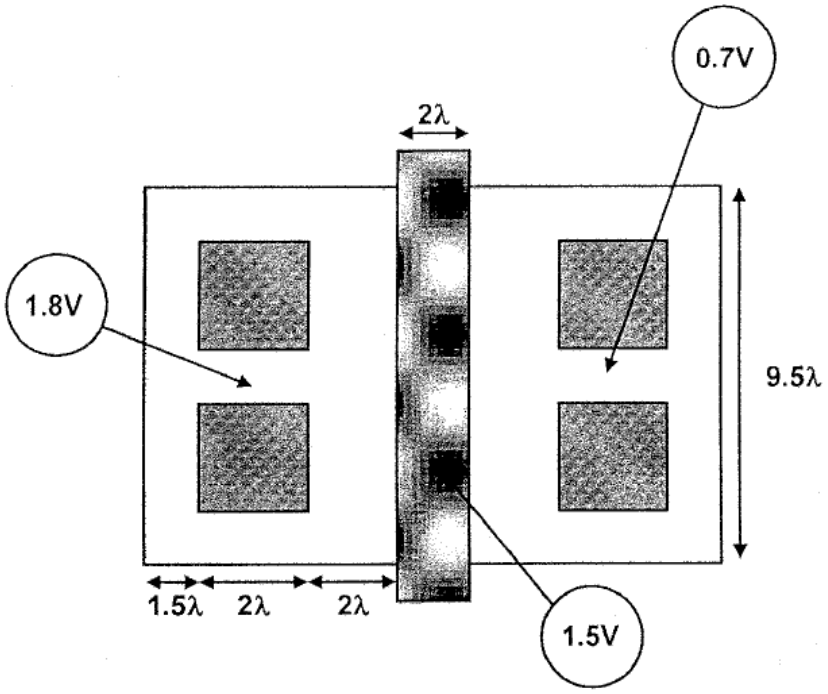
Problem 1 Consider the NMOS transistor layout and voltage biases shown in Figure 1. Suppose we know that for the NMOS under bias, $V_{T0,n} = 0.3\text{V}$, minimum feature size $2\lambda = 2 \times 90\text{nm}$, $\gamma = 0.27\text{V}^{1/2}$, channel length modulation factor $\lambda = 0\ \text{V}^{-1}$, $\mu C_{ox} = 299\ \mu\text{A/V}^2$, and $-2\Phi_F = 0.6\ \text{V}$. Assume the bulk node of the transistor is at 0V. Find the drain-source current I_{DS}.

Hint: Need threshold $V_{Tn} = V_{Tn\phi} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$



Sol:

$V_G = 1.5\text{V}$ $V_D = 1.8\text{V}$ $V_S = 0.7\text{V}$ $V_B = 0\text{V}$

D 1.8V, I_{DS}, 1.5V G, B, S 0.7V (2pt.)

$V_{Tn} = V_{Tn\phi} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$ $V_{SB} = 0.7\text{V}$ (1pt.)

$= 0.3\text{V} + (0.27\ \text{V}^{1/2})\left(\sqrt{|0.6\text{V} + 0.7\text{V}|} - \sqrt{0.6\text{V}}\right)$ (1pt.)

$= 0.3987\ \text{V} \approx 0.4\text{V}$ (1pt.)

$V_{GS} = 0.8\text{V} > V_{Tn} = 0.4\text{V}$ (1pt.)

$V_{DS} = 1.8\text{V} - 0.7\text{V} = 1.1\text{V} > V_{GS} - V_{Tn} = 0.4\text{V}$

sat (1pt.)

$I_{DS,n} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{Tn})^2(1 + \lambda V_{DS})$ (2pt.)

$= \frac{299\ \mu\text{A/V}^2}{2}\left(\frac{9.5}{2}\right)(0.8\text{V} - 0.4\text{V})^2$ (1pt.)

$= 114.4\ \mu\text{A}$

$= \boxed{114\ \mu\text{A}}$ (1pt.)

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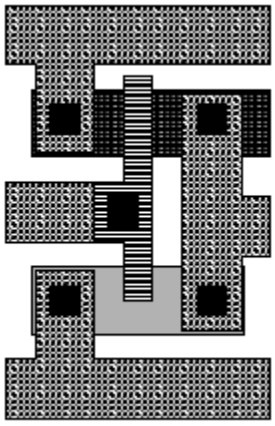
Problem 2

What type of logic function does this layout implement? Point out the three largest problems with this layout. For each explain the impact on gate behavior.



Inverter

The bottom half of the NMOSFET gate is missing.

ii. The PMOSFET drain is bigger than it needs to be, increasing capacitance without bene_t.

iii. The NMOSFET and PMOSFET active regions are the same width, which would result in asymmetric pull-up and pull-down resistances if the gates were designed correctly.

Problem 3:
What function does this layout represent?
How many Metal 1 track in horizontal and vertical direction we have ?

CMOS compound gate for function $Y = \overline{(A + B + C) \bullet D}$

5 vertical and 6 horizontal

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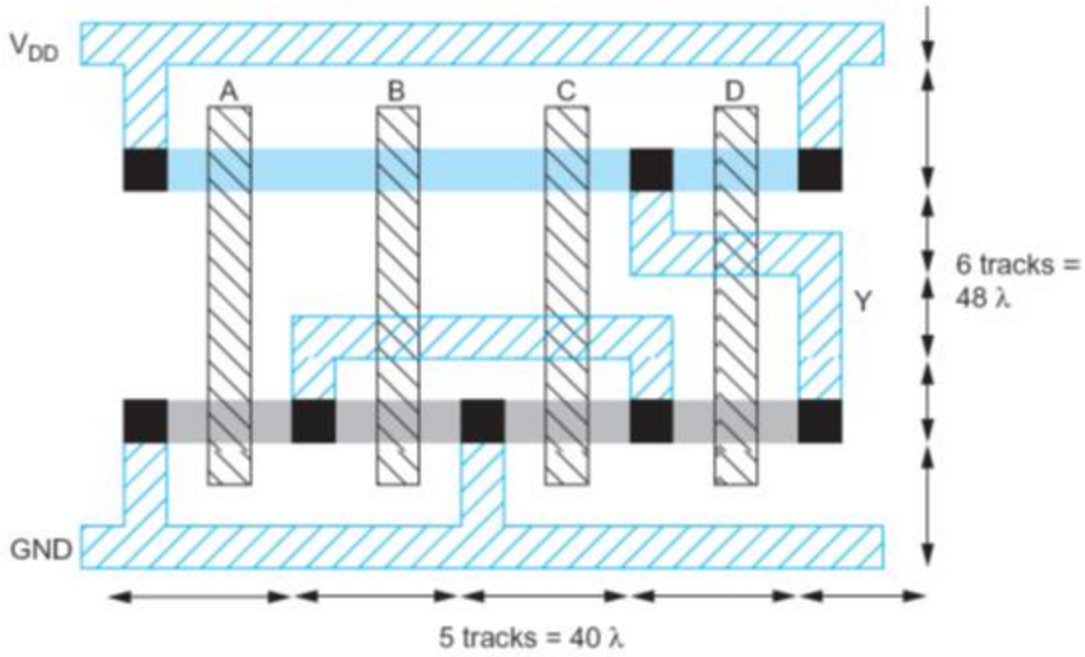

Problem 4:
Given the following stick diagram, what is the function ?
Or I could give you the function and ask about the stick diagram
Or I could give you schematic and ask for stick diagram

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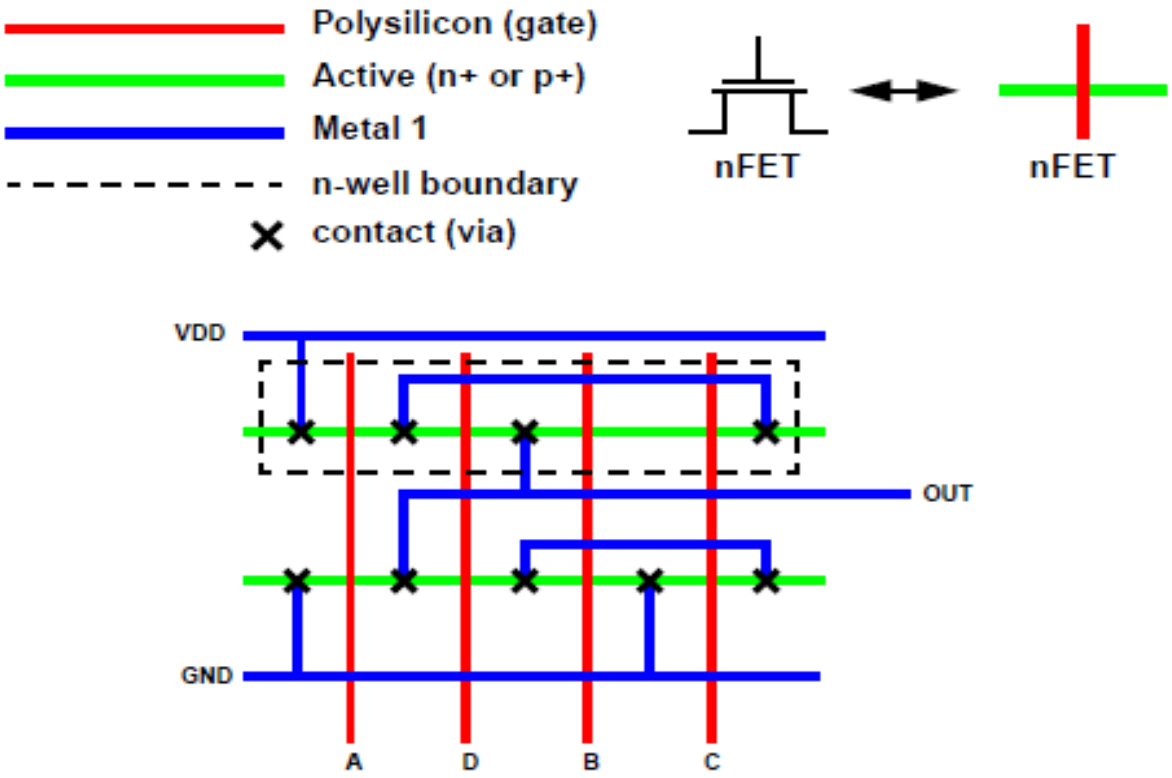

Proplem 6:
What is a design rule ? is it the same for all process /technology ?
Who generate the design rules ? is it the circuit designer or process engineer ?

Problem 7:
Draw detail inverter layout and mark/name all metal1, contact, pdif, ….a as in lect6

Problem 8:
How do you estimate size of cell like

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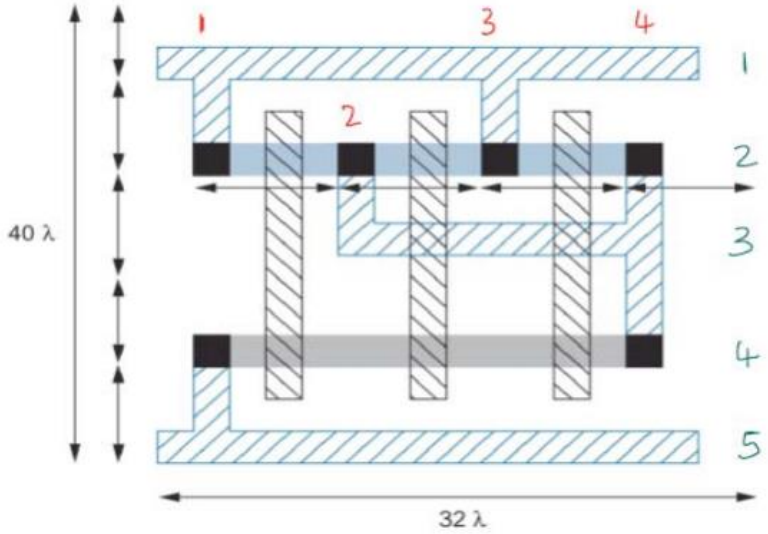
Area Estimation

Horizontal
4×8 = 32
Vertical
5×8 = 40

- Estimate area by counting wiring tracks
  - Multiply by 8 to express in λ



Problem 9:

As in slides, Draw stick diagram for this cell /function

Proplem 10

Sketch the corresponding schematic for the following layout. Make sure the body connections of the MOSFETs are clearly seen in your schematic.

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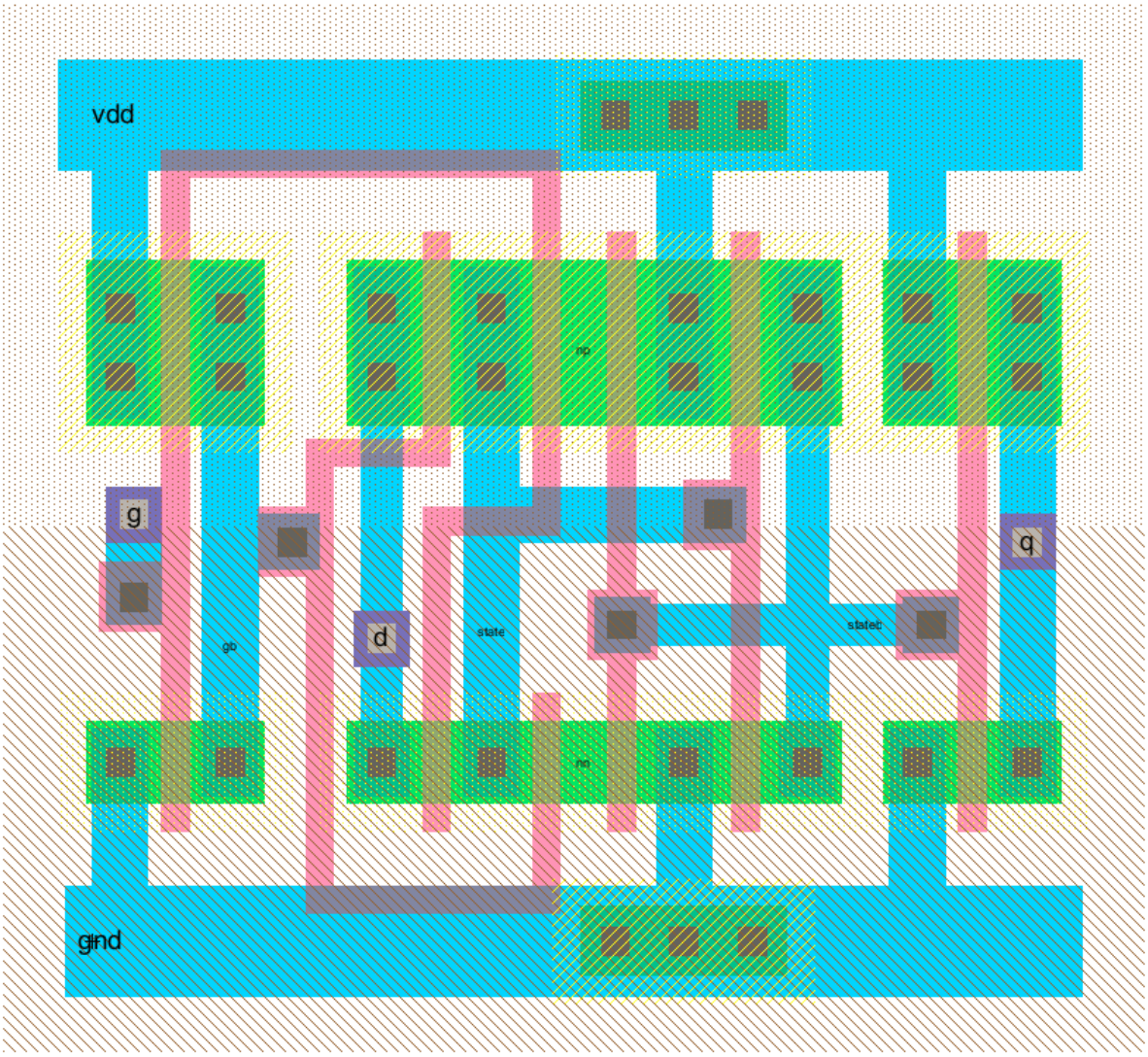

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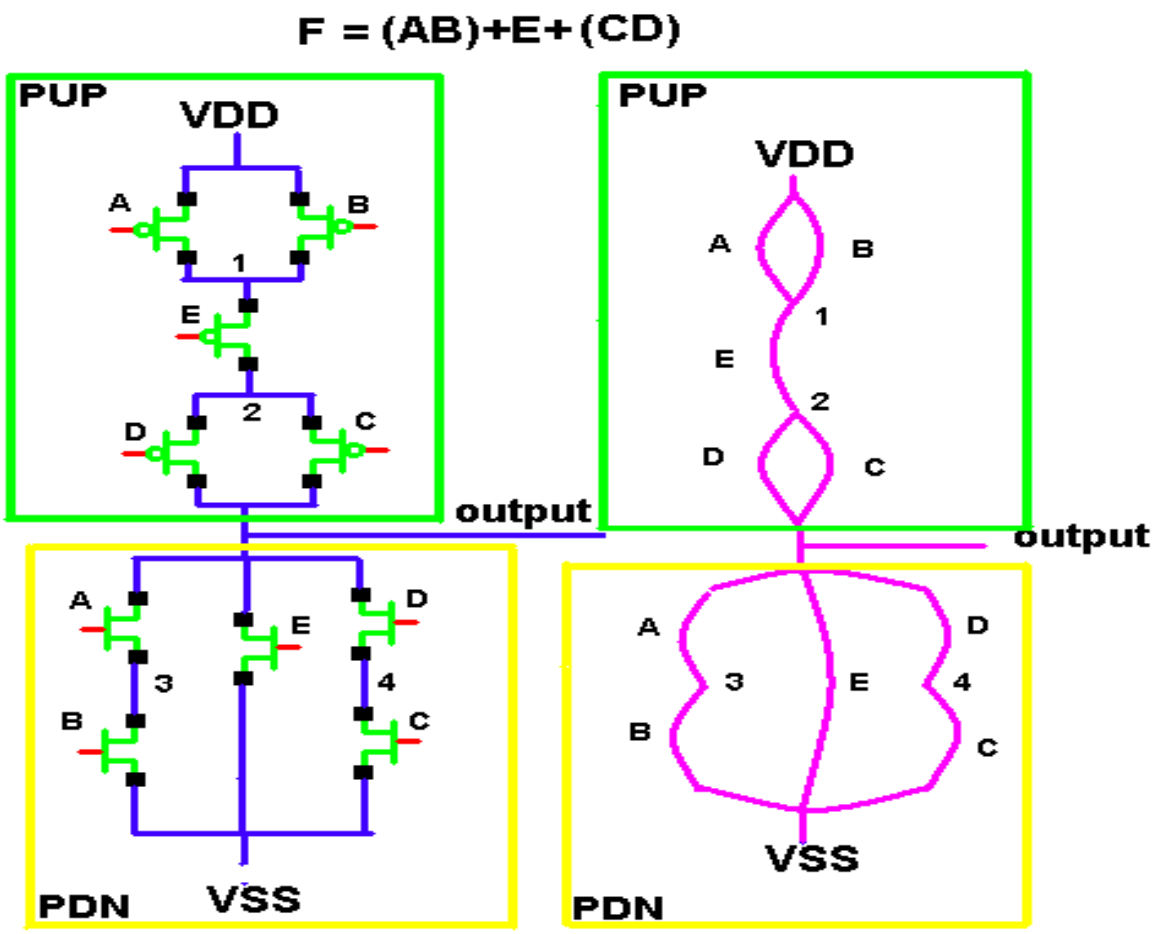

Problem 10

1. Why NMOS technology is preferred more than PMOS technology?

N- channel transistors has greater switching speed when compared tp PMOS transistors.

2.What is Stick Diagram?

It is used to convey information through the use of color code. Also it is the cartoon of a chip layout.

27.What are the uses of Stick diagram?

_ It can be drawn much easier and faster than a complex layout.

_ These are especially important tools for layout built from large cells.

28.Give the various color coding used in stick diagram?

_ Green – n-diffusion

_ Red- polysilicon

_ Blue –metal

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_ Yellow- implant

_ Black-contact areas.

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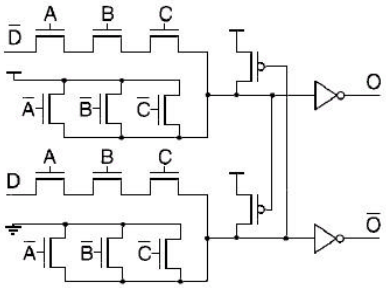
1. What is the logic function of the following gate?



O=ABCD

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FORMULAS AND EQUATIONS

Diode

$$I_D = I_S(e^{V_D/\phi_T} - 1) = Q_D/\tau_T$$

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} \times [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

MOS Transistor

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \text{ (sat)}$$

$$I_D = \upsilon_{sat} C_{ox} W\left(V_{GS} - V_T - \frac{V_{DSAT}}{2}\right)(1 + \lambda V_{DS}) \text{ (velocity sat)}$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right) \text{ (triode)}$$

$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}}\left(1 - e^{-\frac{V_{DS}}{kT/q}}\right) \text{ (subthreshold)}$$

Deep Submicron MOS Unified Model

$$I_D = 0 \text{ for } V_{GT} \le 0$$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$

and $V_{GT} = V_{GS} - V_T$

MOS Switch Model

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

Inverter

$$V_{OH} = f(V_{OL})$$

$$V_{OL} = f(V_{OH})$$

$$V_M = f(V_M)$$

$$t_p = 0.69 R_{eq} C_L = \frac{C_L(V_{swing}/2)}{I_{avg}}$$

$$P_{dyn} = C_L V_{DD} V_{swing} f$$

$$P_{stat} = V_{DD} I_{DD}$$

Static CMOS Inverter

$$V_{OH} = V_{DD}$$

$$V_{OL} = GND$$

$$V_M \approx \frac{rV_{DD}}{1+r} \quad \text{with} \quad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$\text{with } g \approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L\left(\frac{R_{eqn} + R_{eqp}}{2}\right)$$

$$P_{av} = C_L V_{DD}^2 f$$

Interconnect

Lumped *RC*: $t_p = 0.69\ RC$

Distributed *RC*: $t_p = 0.38\ RC$

RC-chain:

$$\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$$

Transmission line reflection:

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_o}$$

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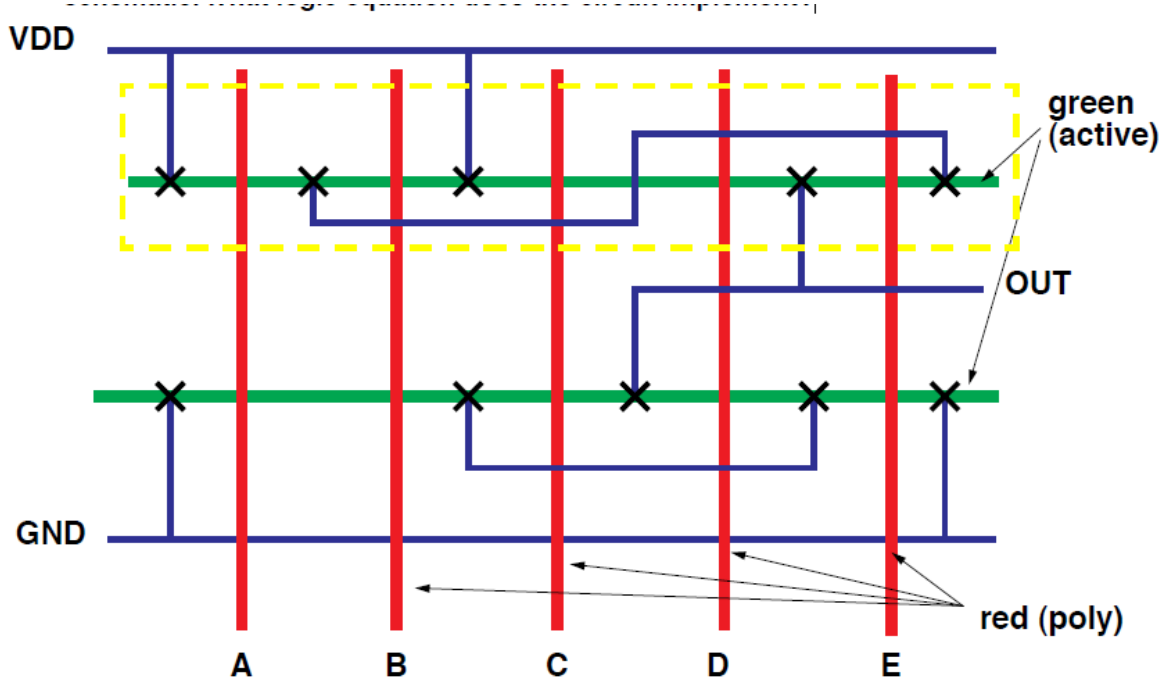
2. Consider the following stick diagram. Draw the electrically equivalent transistor-level Schematic. What logic equation does the circuit implement?



O=~(AB+E).(C+D)

3. Consider the logical expression

out= ~((a+b) • (c+d))

. Convert this to a schematic diagram for static CMOS logic, then convert it to a stick-diagram layout (as in question 1).

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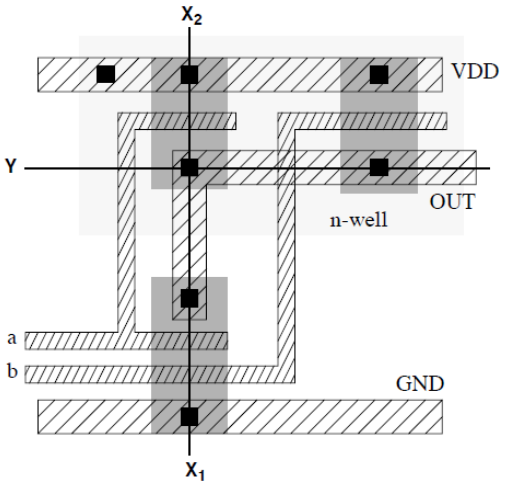
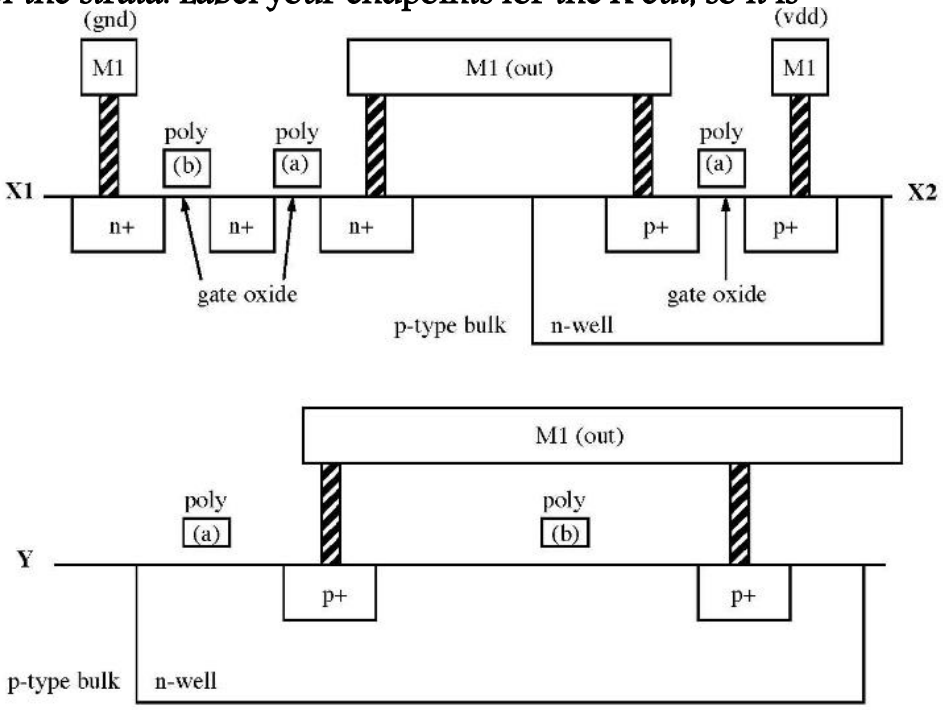
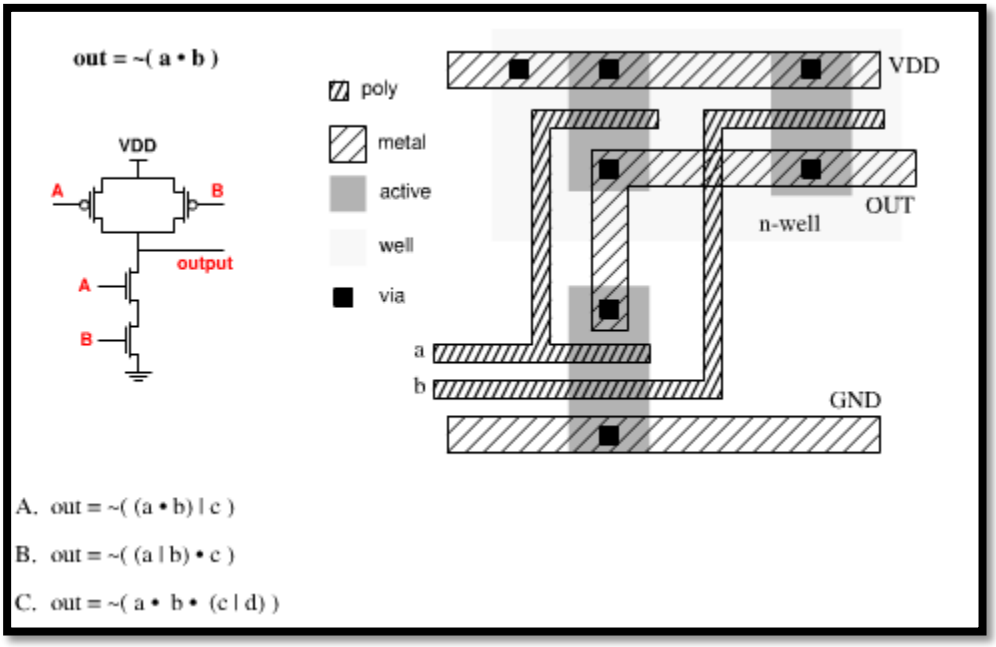
4. Provide a side-view diagram for each of the cuts X and Y through the layout below. Be sure to label each of the strata. Label your endpoints for the X cut, so it is clear which end is which.







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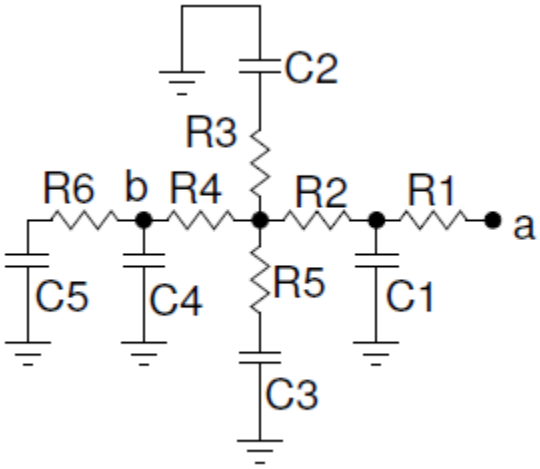
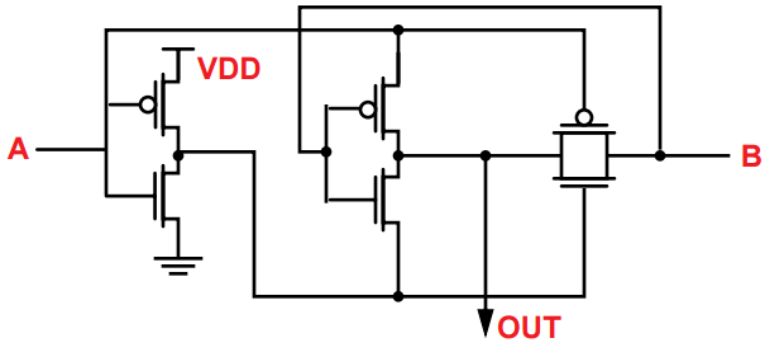
5. Determine the Elmore delay from Node a to Node b in the following circuit.

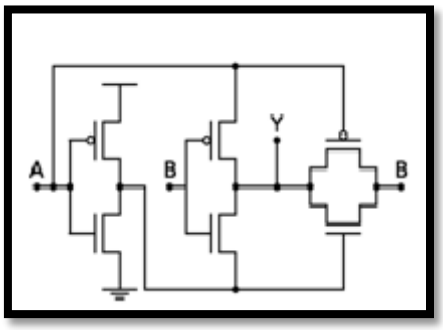


$$\tau_{ab} = R1(C1+C2+C3+C4+C5)+R2(C2+C3+C4+C5)+R4(C4+C5)$$

6. What is the output function of the following circuit?



XOR



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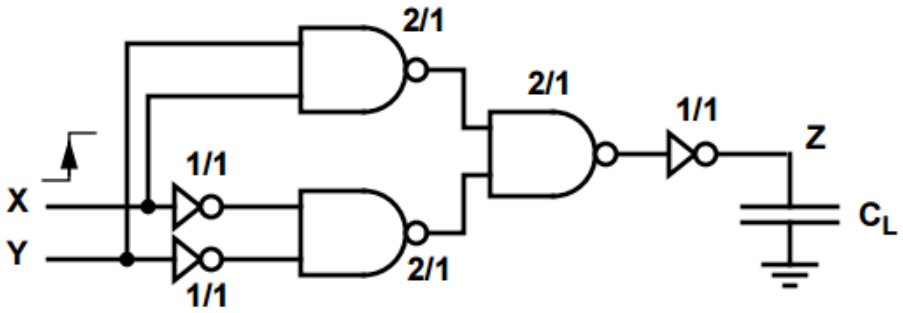
7. Consider the CMOS circuit shown below In the figure, the W/L ratios for each gate apply to both NMOS and PMOS transistors. We want to determine the delay from a rising transition (0 → 1) ……

A. Assuming that the rise and fall times are good approximations of the propagation delay, determine the delay from X to Z, in terms of τ, when Y = 0.

B. Now, assume that Y = 1. What is the new value for the propagation delay from X to Z? Can you comment on this?



2. $T = RC_n$

A| • transition in bottom NAND 0 to 1 $t_{PLH} = 0.69 \times \frac{2R_n}{1} \times C_n = 0.69 R_n C_n$ ④

• no transition in top NAND stays 1

• transition in top NOT from 1 to 0 $t_p = 0.69 R_n C_n$ ③

• no transition in bottom NOT

• last NAND 1 to 0 $t_{PHL} = 0.69 \times \frac{R_n}{2} \times C_n = 0.345 R_n C_n$ ②

• last NOT 0 to 1 $t_p = 0.69 R_n C_n \cdot 10 = 6.9 R_n C_n$ ①

total = $R_n C_n \left(6.9^{①} + 0.345^{②} + 0.69^{③} + 0.69^{④}\right) = \boxed{8.625 R_n C_n}$

B| • transition in top NAND from 1 to 0 $t_{PHL} = 0.345 R_n C_n$ ②

• no change in bottom NAND, so we can ignore transition in top NOT

• last NAND 0 to 1 $t_{PLH} = 0.69 \times 2R_n/2 \cdot C_n = 0.69 R_n C_n$ ①

• last NOT 1 to 0 $t_p = 6.9 R_n C_n$

total = $R_n C_n \left(6.9^{①} + 0.69^{③} + 0.345^{②}\right) = \boxed{7.935 R_n C_n}$

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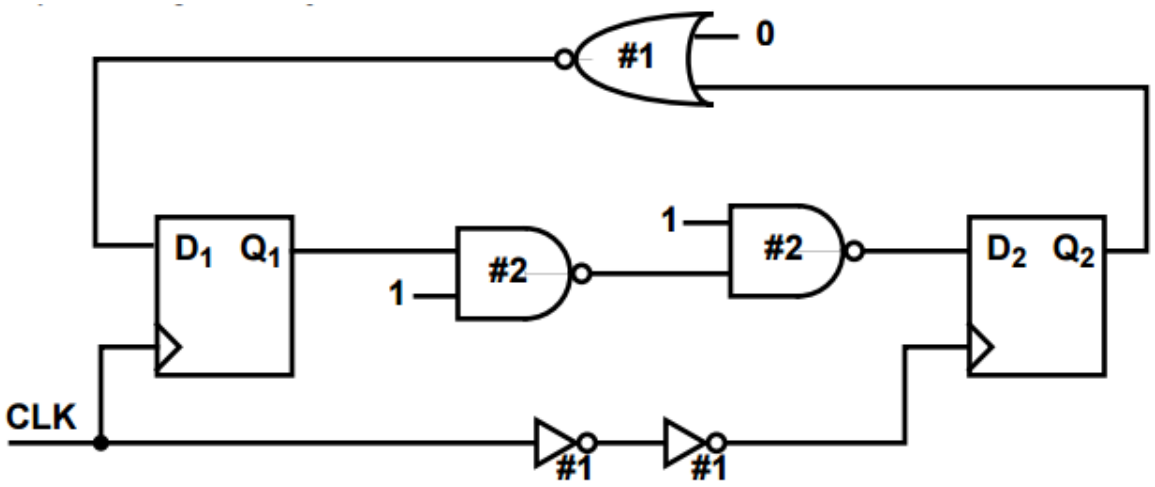
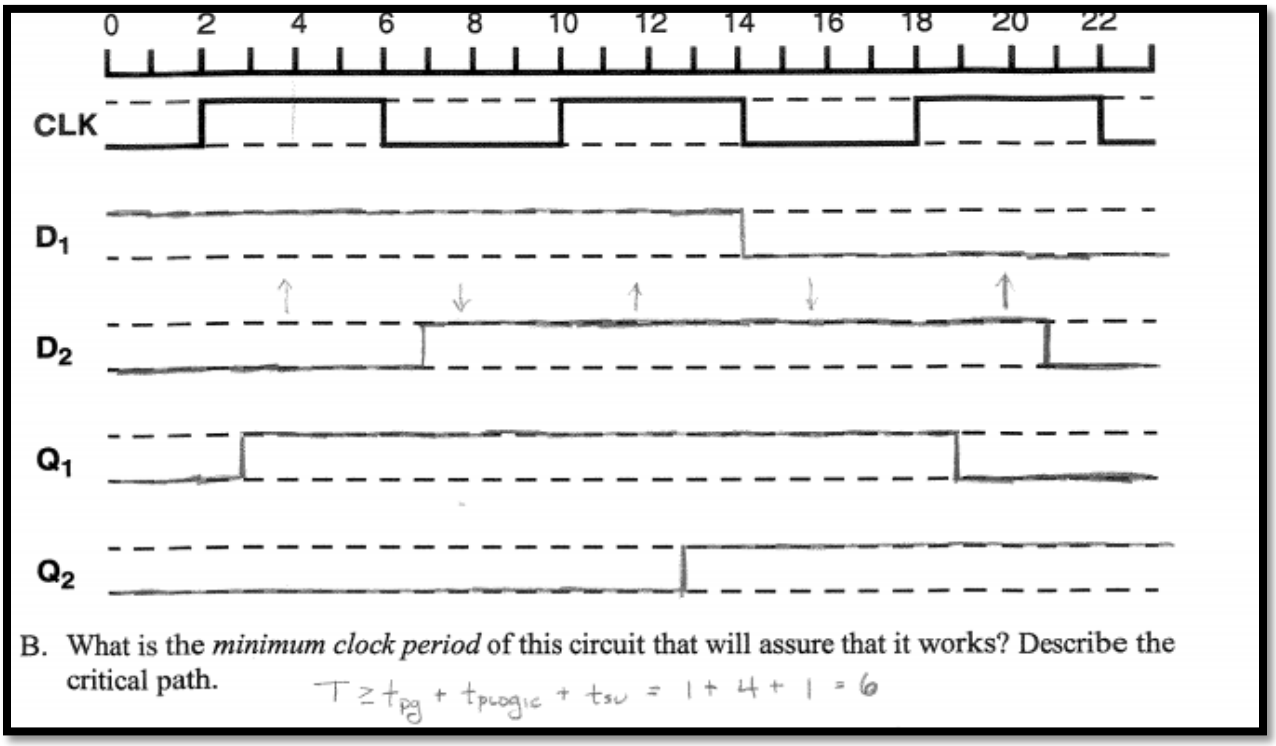
8. The circuit shown below uses two identical rising edge triggered Flip-Flops. Assume that for both Flip-Flops, ……



A.Complete the following timing diagram for the circuit. Assume the initial states of Q1 and Q2 are 0, and have remained at 0 for a long time (but no clock edge has come along yet to latch the 1 value at D1).



B. What is the *minimum clock period* of this circuit that will assure that it works? Describe the critical path. $T \geq t_{pg} + t_{pcogic} + t_{su} = 1 + 4 + 1 = 6$

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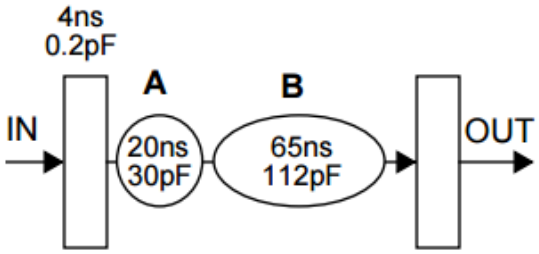
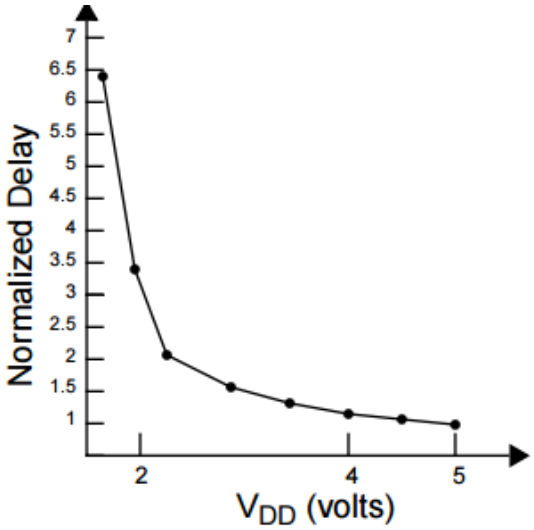
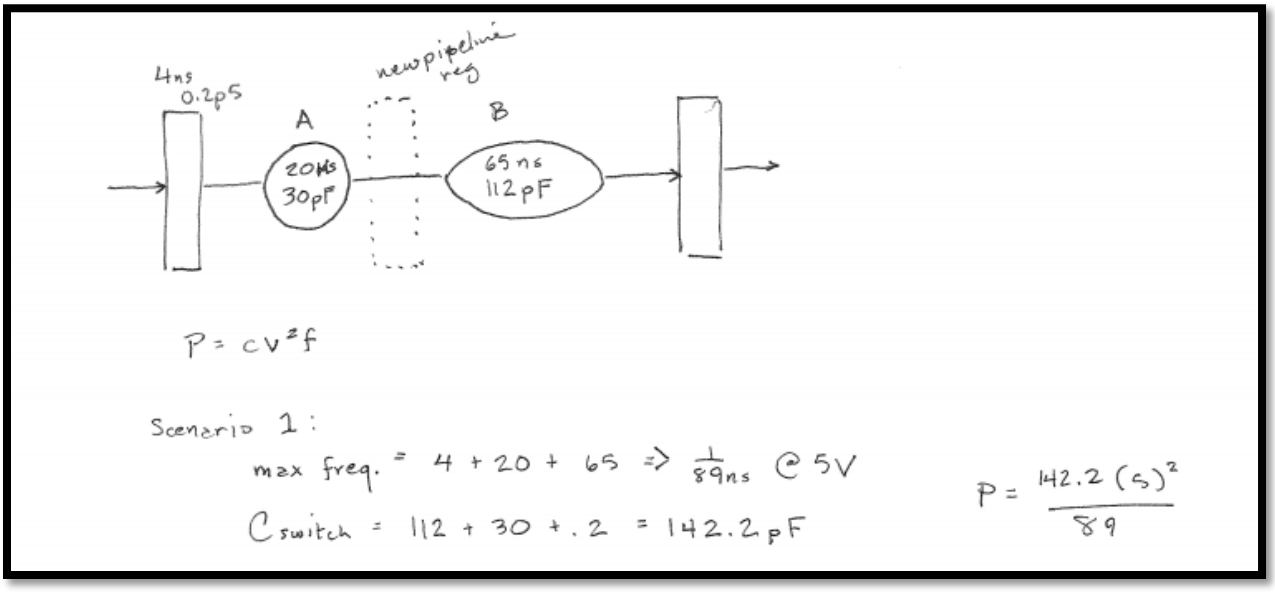
B. What is the minimum clock period of this circuit that will assure that it works? Describe the critical path.

Above

9. **Consider the circuit below, left. Modules A and B have a delay of 20nsec and 65nsec at 5V and switch 30pF and 112pF, …..**







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Scenario 2:

max freq. = 4 + 65 (new pipeline reg, B) $\Rightarrow \frac{1}{69ns}$ @ 5V

but we will still be running @ $\frac{1}{89}$ ns, so voltage can change

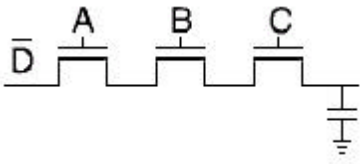
$C_{switch} = 112 + 30 + .2 + .2 = 142.4pF$

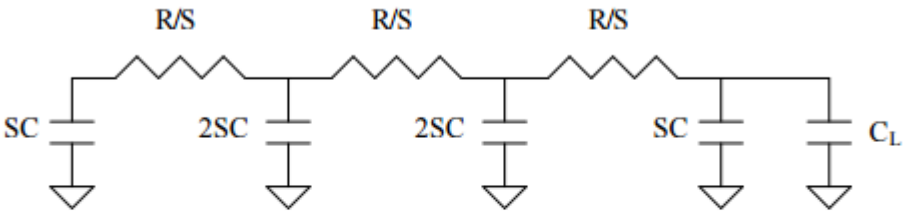
$P = \frac{142.4 (V^2)}{89}$ $\quad V \approx 5 \cdot \frac{69}{89}$

Compared: Scenario 2 / Scenario 1 $\approx$ $\frac{24.04}{39.94} \approx 60\%$

40% power saving

10. The serial NMOS transistors in the logic section of the CPL gate shown below are clearly on the critical path. We have extracted that critical path in the figure shown below. …..





The RC network under worst case input pattern can be modeled as above.

$T_p = 0.69*((R/S)*(2SC) + (2R/S)*(2SC) + (3R/S)*(SC+C_L))$
$= 0.69 * (9RC + 3RC_L/S)$

Size the transistors large to reduce delay.

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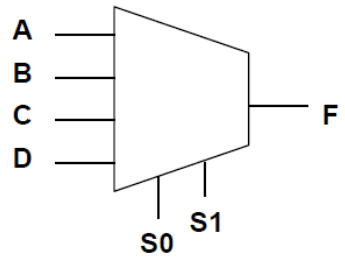
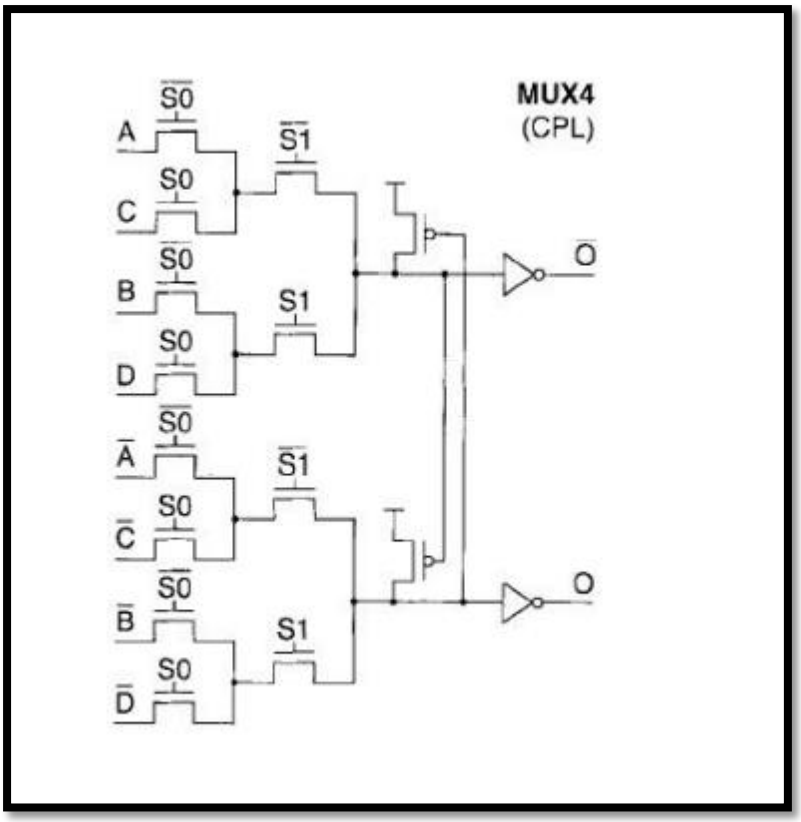
11. Design a 4 input multiplexer (see the truth-table below for its fuction) in the complementary pass-transistor logic style using a minimum number of transistors.

S0	S1	Output
0	0	A
0	1	B
1	0	C
1	1	D





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1) You have a carry-bypass adder with 4 bits per stage but you find that it is too slow
for large total number of bits. Being lazy to go for a different design, you pipeline the
adder. A 12-bit section of your circuit is shown in Fig. 4. Answer the questions (a)-(b)
in terms of the total number of bits, *N*, and the following one-bit delays:

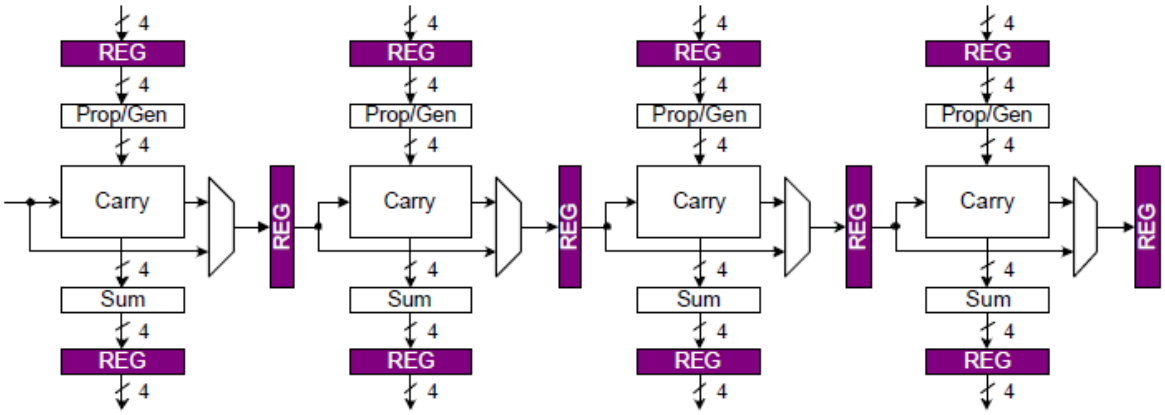
tppg delay through the propagate/generate block = 0.6ns

tpcarry delay of a single carry bit = 1ns

tpsum delay of a single sum bit = 2ns

tpmux delay of the multiplexer = 0.4ns

tpreg delay of the register = 0.5ns



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a) (4 pts) What is the minimum clock period you can use for your N-bit adder? (i.e.

The worst-case scenario occurs in the first block, where input carry is not available and needs to be generated.

The worst-case carry propagation delay is:

$$tp(carry) = tp_{reg} + tp_{pg} + 4tp_{carry} + tp_{mux} = 5.5ns$$

The worst-case sum propagation delay is:

$$tp(sum) = tp_{reg} + tp_{pg} + 3tp_{carry} + tp_{sum} = 6.1ns$$

The minimum clock period is therefore:

$$T_{Clk}^{min} = \max\{tp(carry), tp(sum)\} = 6.1ns$$

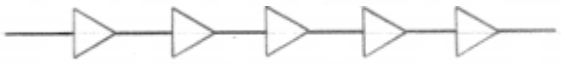
The clock period does not depend on the number of bits

b) (3 pts) How many clock cycles does it take for the first N-bit addition to complete?

There are total of $B_{tot} = (N/4 - 1)$ blocks needed for an N-bit addition. Each block computes with inputs of the preceding blocks. Therefore, it takes $N/4 - 1$ clock cycles to complete N-bit addition.

The latency is linearly dependent on the number of bits.

11.16 Consider a ring oscillator consisting of five inverters, each having $t_{PLH} = 60$ ns and $t_{PHL} = 40$ ns. Sketch one of the output waveforms, and specify its frequency and the percentage of the cycle during which the output is high.



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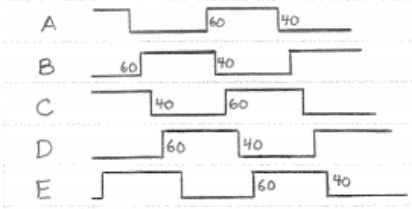
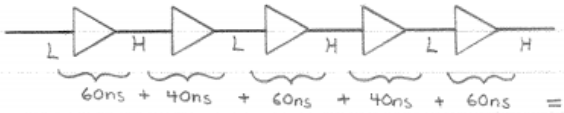


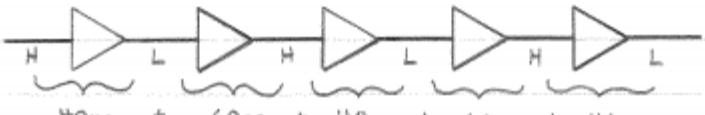
$t_{PLH} = 60ns$
$t_{PHL} = 40ns$

When output is high,



60ns + 40ns + 60ns + 40ns + 60ns = 260ns

When output is low,



40ns + 60ns + 40ns + 60ns + 40ns = 240ns

Period = (240ns + 260ns) = 500ns
Frequency = 1/Period = 2MHz

% of cycle for which the output is high

$\frac{260ns}{500ns} = .52$ or 52%

11.17 A ring-of-eleven oscillator is found to oscillate at 20 MHz. Find the propagation delay of the inverter.

For 11 inverters, there are 2(11) = 22 transitions whose average length is

$t_p = \left[\frac{1}{20 \times 10^6}\right]\left(\frac{1}{22}\right) = 2.27ns$

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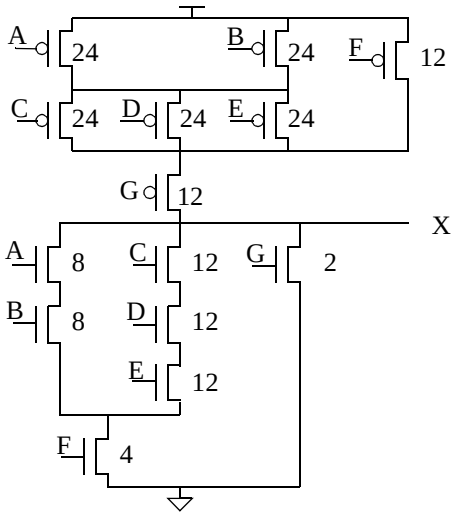
Chapter 6
PROBLEMS

1. [E, None, 4.2] Implement the equation $X = ((\overline{A} + \overline{B})(\overline{C} + \overline{D} + \overline{E}) + \overline{F})\,\overline{G}$ using complementary CMOS. Size the devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 2$ and PMOS $W/L = 6$. Which input pattern(s) would give the worst and best equivalent pull-up or pull-down resistance?

Solution

Rewriting the output expression in the form $X = ((\overline{A} + \overline{B})(\overline{C} + \overline{D} + \overline{E}) + \overline{F})\,\overline{G} = \overline{((AB + CDE)F) + G}$ allows us to build the pulldown network by inspection (parallel devices implement an OR, and series devices implement an AND). The pullup network is the dual of the pulldown network.



The plot shows sizes that meet the requirement - in the worst case, the output resistance of the circuit matches the output resistance of an inverter with NMOS W/L=2 and PMOS W/L=6.

The worst case pull-up resistance occurs whenever a single path exists from the output node to Vdd. Examples of vectors for the worst case are ABCDEFG=1111100 and 0101110. The best case pull-up resistance occurs when ABCDEFG=0000000.

The worst case pull-down resistance occurs whenever a single path exists from the output node to GND. Examples of vectors for the worst case are ABCDEFG=0000001 and 0011110.

The best case pull-down resistance occurs when ABCDEFG=1111111.

2. Implement the following expression in a full static CMOS logic fashion using no more than 10 transistors:

$$\overline{Y} = (A \cdot B) + (A \cdot C \cdot E) + (D \cdot E) + (D \cdot C \cdot B)$$

Solution

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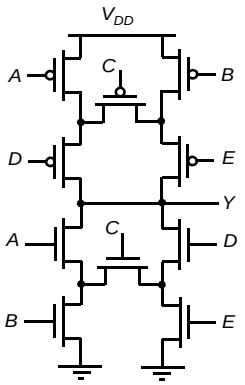
The circuit is given in the next figure.



3. Consider the circuit of Figure 6.1.

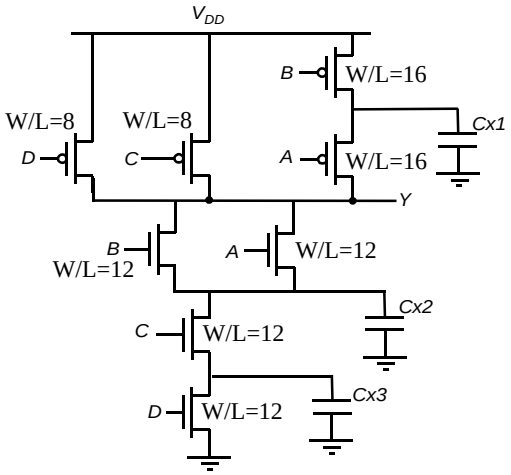


Figure 6.1 CMOS combinational logic gate.

a. What is the logic function implemented by the CMOS transistor network? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 4$ and PMOS $W/L = 8$.

Solution

The logic function is $: Y = \overline{(A + B)CD}$. The transistor sizes are given in the figure above.

b. What are the input patterns that give the worst case t_{pHL} and t_{pLH}. State clearly what are the initial input patterns and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.

Solution

The worst case t_{pHL} happens when the internal node capacitances (*Cx2* and *Cx3*) are charged before the high to low transition. The initial states that can cause this are: ABCD=[1010, 1110, 0110]. The final state is one of: ABCD=[1011, 0111].

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The worst case t_{pLH} happens when *Cx1* is charged before the low to high transition. The input pattern that can cause this is: ABCD=[0111] =>[0011].

c. Verify part (b) with SPICE. Assume all transistors have minimum gate length (0.25μm).

Solution

The two cases are shown below.

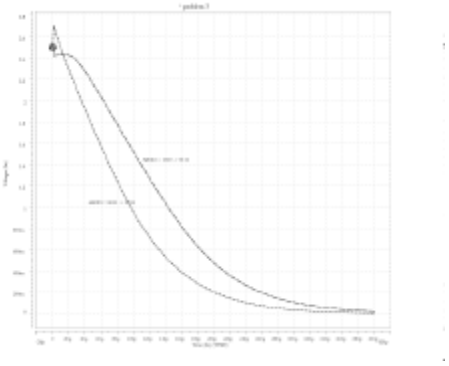

Figure 6.2 Best and worst t_{pHL}.

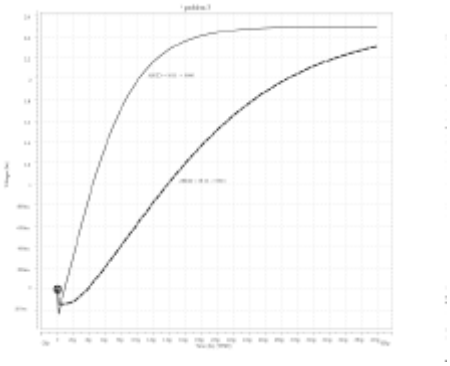

Figure 6.3 Best and worst t_{pLH}.

d. If P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.3 and P(D=1)=1, determine the power dissipation in the logic gate. Assume V_{DD}=2.5V, C_{out}=30fF and f_{clk}=250MHz.

Solution

Since D is always 1, the circuit implements the following function $Y = \overline{(A + B)C}$.

$P_{(A+B)=1} = P_{A=0}.P_B = 0 = 0.5*(1-0.2) = 0.4$,

$P_{(A+B)=0} = 1 - 0.4 = 0.6$,

$P_{Y = 0} = P_{(A+B) = 1}.P_C = 1 = 0.6*0.3 = 0.18$

$P_{Y = 1} = 1 - 0.18 = 0.82$

$P_{Y = 0 =>1}= 0.18*0.82 = 0.1476$

So $Pdyn = P_{Y = 0 =>1} C_{out} V_{DD}^2 f_{clk}$ = $(0.1476)(30.10^{-15})(2.5^2)(250.10^6) = 6.92\,\mu W$.

4. [M, None, 4.2] CMOS Logic

a. Do the following two circuits (Figure 6.4) implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits.

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Solution

Yes, they implement the same logic function :

$F = (\overline{ABCD + E}) = (\overline{A} + \overline{B} + \overline{C} + \overline{D}).\overline{E}$

b. Will these two circuits' output resistances always be equal to each other?

Solution

No

c. Will these two circuits' rise and fall times always be equal to each other? Why or why not?

Solution

No. Circuit B appears optimized for the case where the transistor with input E is on the critical path since it is closer to the output node than in circuit A. Therefore, if input E arrives later, circuit B will be faster than circuit A since the internal node will already be charged and only the output capacitance needs to be switched. Even if we assume, all inputs arrive at the same time, however, the two circuits rise and fall times will not be equal to each other. Consider an input combination where E,A,B,C,D are all low. Circuit A has only one body-affected device while circuit B has four. Since the associated rise in V_t and fall in output resistance affects only one resistor in circuit A, but four parallel resistors in circuit B, we expect a difference in the timing waveforms.

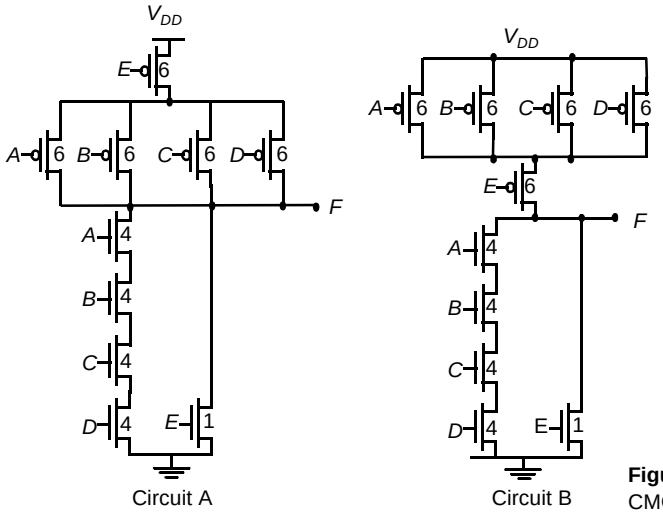

Figure 6.4 Two static CMOS gates.

5. [E, None, 4.2] The transistors in the circuits of the preceding problem have been sized to give an output resistance of 13 kΩ for the worst-case input pattern. This output resistance can vary, however, if other patterns are applied.

a. What input patterns (*A*–*E*) give the lowest output resistance when the output is low? What is the value of that resistance?

Solution

The lowest output resistance is obtained when all inputs (A, B, C, D and E) are equal to 1. In that case, the output resistance is the parallel of the resistance of a nMOS of width 1, with a series of four equal nMOS of width 4. Both combinations have the same resistance, equal to the worst-case output resistance, 13 $k\Omega$. Then the output resistance, in this case, is half this value, 6.5 $k\Omega$.

b. What input patterns (*A*–*E*) give the lowest output resistance when the output is high? What is the value of that resistance?

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Solution

The lowest output resistance is obtained when all inputs are equal to zero. Each of the pMOS have the same width, so all of them have the same resistance. The worst case resistance happens when only one of the inputs (A, B, C or D) is equal to 0 while all the rest are equal to 1. The output resistance in that case is the series of the resistance of two of the pMOS and it is equal to 13 kΩ . Then, each of the pMOS has an output resistance equal to 6.5 kΩ . The output resistance is equal to the series of one of these resistance with the parallel of four of the same resistnaces. Then, the minimum output resistance is 6.5 kΩ + 6.5 kΩ /4 = 8.125 kΩ .

6. [E, None, 4.2] What is the logic function of circuits A and B in Figure 6.5? Which one is a dual network and which one is not? Is the nondual network still a valid static logic gate? Explain. List any advantages of one configuration over the other.

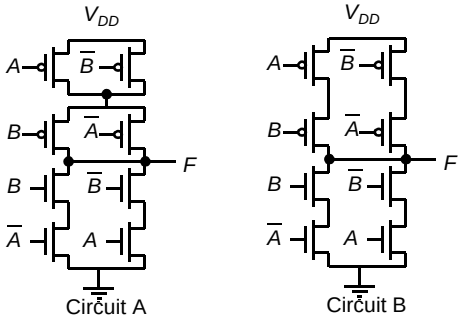

Figure 6.5 Two logic functions.

Solution

Both circuits A and B implement the XOR logic function. Circuit A is a dual network because the pull up network is dual with the pull down network.

However, circuit B is still a valid static logic gate, because for any combination of the inputs, there is either a low resistance path from V_{DD} or ground to the output. Circuit B has an extra advantage. The internal node capacitances are less compared to Circuit A, which make it faster than Circuit A.

7. [E, None, 4.2] Compute the following for the pseudo-NMOS inverter shown in Figure 6.6:

a. V_{OL} and V_{OH}

Solution

To find V_{OH}, set V_{in} to 0, because V_{OL} is likely to be below V_{T0} for the NMOS. If V_{in}=0, then M_1 is off, so the PMOS pulls the output all the way to the rail. So, $V_{OH}=V_{DD}$=2.5V.

To find V_{OL}, set $V_{in} = V_{OH}$ = 2.5V. The NMOS is all the way on, but so is the PMOS. To find V_{OL}, we can write a current balancing equation at the output node: $I_{DP}+I_{DN}=0$. First, we must determine the region of operation for each device. We can assume that $V_{DS} = V_{OL}$ for the NMOS is less than V_{DSAT}, so the NMOS is in the linear region. V_{DS} for the PMOS will be more negative than V_{DSAT}, and V_{GTp} = -2.1, so the PMOS is velocity saturated. The equation is therefore:

$$k'_p \cdot \frac{W}{L} \cdot V_{DSAT} \cdot (V_{GT} - 0.5V_{DSAT}) \cdot (1 + \lambda V_{DS}) + k'_n \cdot \frac{W}{L} \cdot V_o \cdot (V_{GT} - 0.5V_o) \cdot (1 + \lambda V_o) = 0$$

Plugging in numbers (process parameters such as V_{DSAT} appear in tables in previous chapters) gives:

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$$-30 \cdot 2 \cdot -1 \cdot (-1.6) \cdot (1 - 0.1(V_o - 2.5)) + 115(16) \cdot V_o \cdot (2.07 - 0.5V_o) \cdot (1 + 0.06V_o) = 0$$

Solving for V_o gives VOL = 31.6mV.

b. NM_L and NM_H

Solution

Rather than calculating the derivative of the current, we will estimate V_{IL} and V_{IH} from the simulated VTC. This approach estimates that the noise margin low is about 0.47Vand the noise margin high is about 1.67V.

c. The power dissipation: (1) for V_{in} low, and (2) for V_{in} high

Solution

For Vin low, the NMOS is off, so the power dissipation is 0W. For Vin high, P=VI=2.5*I_{DP}. We saw in part a) the equation for I_{DP}. Plugging in the value for V_{OL}, we get P=VI=2.5*120µ A=300µ W.

d. For an output load of 1 pF, calculate t_{pLH}, t_{pHL}, and t_p. Are the rising and falling delays equal? Why or why not?

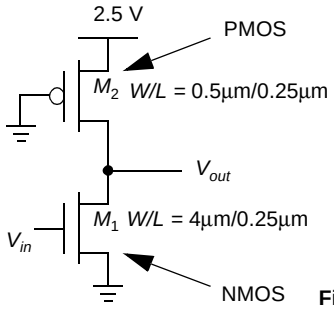

Figure 6.6 Pseudo-NMOS inverter.

Solution

We cannot use the estimate of resistance from the I-V curve for the HL transition because the PMOS is still on. Therefore, we will use the average current method for estimating delay. The average current for the HL transition through the PMOS is 0.5($I_{VDD=2.5}$ + $I_{VDD=1.25}$). $I_{VDD=2.5}$ = 0. $I_{VDD=1.25}$ = -30(2)(-1)(-2.1+0.5) *(1+0.1(1.25)) = 108uA. Thus, Iavg for the PMOS is 54uA.

For the NMOS, $I_{VDD=2.5}$ = 115(16)(0.63)(2.07-.63/2)(1+0.06*2.5)=2.4mA and $I_{VDD=1.25}$ = 115 (16) (0.63) *(2.07-.63/2)(1+0.06*1.25) = 2.2mA. So, Iavg for the NMOS is 2.3mA. The average current discharging the capacitor is then 2.3mA-54uA = 2.25mA. Then t_{pHL} = C*delV/I_{avg} = 556ps.

For t_{pLH}, the NMOS is off, so we can use equivalent resistance to find the transistion time. From the table of resistances in the text, we can calculate R_{EQ} = 31kΩ/(W/Lp) = 15.5kΩ. Then t_{pLH} = 0.69*C*R_{EQ}. So t_{pLH} = 10.7ns.

t_p = (t_{pLH} + t_{pHL})/2 = 5.6ns. The rising delay is much longer because the PMOS is very weak relative to the NMOS.

8. [M, SPICE, 4.2] Consider the circuit of Figure 6.7.

a. What is the output voltage if only one input is high? If all four inputs are high?

Solution

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$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{min} - \frac{V_{min}^2}{2} \right) \cdot (1 + \lambda \cdot V_{DS})$$

Consider a case when one input is high: A = V_{DD} and B = C = D = 0 V. Assume that V_{out} is small enough that $V_{min} = V_{DSAT}$ for the PMOS device, and $V_{min} = V_{DS} = V_{out}$ for the NMOS devices. Solve for V_{out} by setting the drain currents in the PMOS and NMOS equal to each other, $|I_{DP}| = |I_{DN}|$, where the drain currents are functions of V_{out}, V_{DD}, and the device parameters.

V_{out} = 102 mV, and I_D = 35.7 µA.

Now verify that the assumptions for V_{min} are correct. For the PMOS: V_{DS} = -2.34 V, V_{DSAT} = -1 V, V_{GT} = -2.1 V, therefore $V_{min} = V_{DSAT}$. For the NMOS: V_{DS} = 102mV, V_{DSAT} = 630mV, V_{GT} = 2.07 V, therefore $V_{min} = V_{DS}$.

Consider the case when all inputs are high: A = B = C = D = V_{DD}. For these hand calculations, this is numerically equivalent to a circuit with a single NMOS device with W/L = 4*1.5 and its gate tied to V_{DD}. Now, the analysis used above for the case when one device is on can be reused, replacing W/L of the NMOS with 6, and using the same assumptions for V_{min}. V_{out} = 25 mV, and I_D = 35.9 µA. The assumptions for V_{min} are correct.

b. What is the average static power consumption if, at any time, each input turns on with an (independent) probability of 0.5? 0.1?

Solution

Notice in part a) that the drain current in the PMOS is 35.7 µA with one NMOS on and 35.9 µA with four NMOS devices on. The current in the PMOS can be approximated as 35.8 µA when any number of NMOS devices are on and 0 µA when all four are off. The probability that all four NMOS devices are off is $(1-\rho)^4$ where ρ is the probability an input is high. Therefore,

$$P_{AVG} = P_{OFF} \cdot (1-\rho)^4 + P_{ON} \cdot \left[1 - (1-\rho)^4\right]$$

where P_{OFF} = 0 W, and P_{ON} = 89.5 µW. P_{AVG} = 83.9 µW when ρ = 0.5 and P_{AVG} = 30.7 µW when ρ = 0.5.

c. Compare your analytically obtained results to a SPICE simulation.

Solution

From SPICE: V_{out} = 98.7 mV, and I_D = 38.2 µA with one NMOS device on and V_{out} = 23.5 mV, and I_D = 38.3 µA with all NMOS devices on.

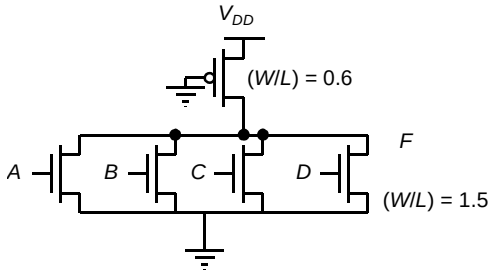

Figure 6.7 Pseudo-NMOS gate.

9. [M, None, 4.2] Implement $F = A\overline{BC} + \overline{A}CD$ (and $\overline{F}$) in DCVSL. Assume *A, B, C, D,* and their complements are available as inputs. Use the minimum number of transistors.

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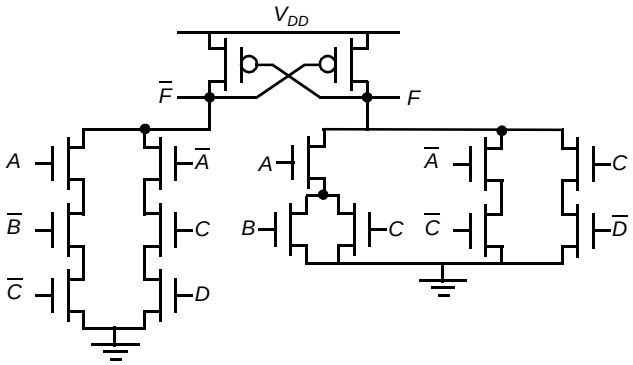
Solution



10. [E, Layout, 4.2] A complex logic gate is shown in Figure 6.8.

a. Write the Boolean equations for outputs *F* and *G*. What function does this circuit implement?

Solution

G=A(XOR)B
F=A(XNOR)B

b. What logic family does this circuit belong to?

Solution

It belongs to the DCVSL logic family.

c. Assuming *W/L* = 0.5u/0.25u for *all nmos* transistors and *W/L* = 2u/0.25u for the *pmos* transistors, produce a layout of the gate using Magic. Your layout should conform to the following datapath style: (1) Inputs should enter the layout from the left in polysilicon; (2) The outputs should exit the layout at the right in polysilicon (since the outputs would probably be driving transistor gate inputs of the next cell to the right); (3) Power and ground lines should run vertically in metal 1.

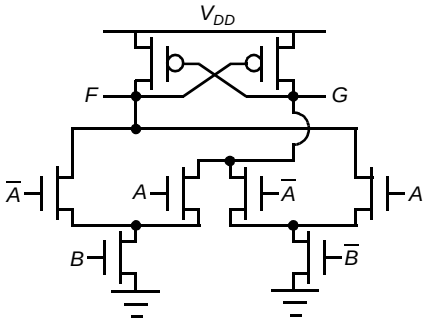


Figure 6.8 Two-input complex logic gate.

d. Extract and netlist the layout. Load both outputs (F,G) with a 30fF capacitance and simulate the circuit. Does the gate function properly? If not, explain why and resize the transistors so that it does. Change the sizes (and areas and perimeters) in the HSPICE netlist.

Solution

The gate doesn't function properly, because the PMOS devices are strong and the NMOS pull down network can not switch the output nodes .

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If you decrease the PMOS sizes to W=0.5um, then the logic gate will function properly.

11. Design and simulate a circuit that generates an optimal differential signal as shown in Figure 6.9. Make sure the rise and fall times are equal.

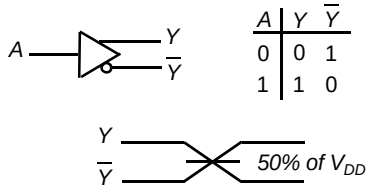
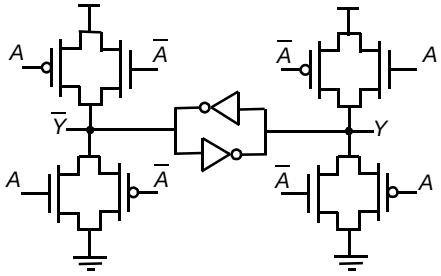


Figure 6.9 Differential Buffer.

Solution

The circuit is shown below.



If the inverters are sized for equal rise and fall times then you can achieve equal rise and fall times on the differential outputs, as long as the other FETs are sized symmetrically.

12. What is the function of the circuit in Figure 6.10?

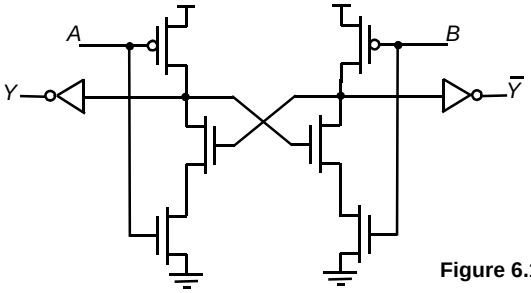


Figure 6.10 Gate.

Solution

The circuit implements an S-R latch. Set is A and Reset is B. The invalid state is when both A and B are 0.

13. Implement the function $S = ABC + A\overline{BC} + \overline{A}BC + \overline{A}B\overline{C}$, which gives the sum of two inputs with a carry bit, using NMOS pass transistor logic. Design a DCVSL gate which implements the same function. Assume *A*, *B*, *C*, and their complements are available as inputs.

Solution

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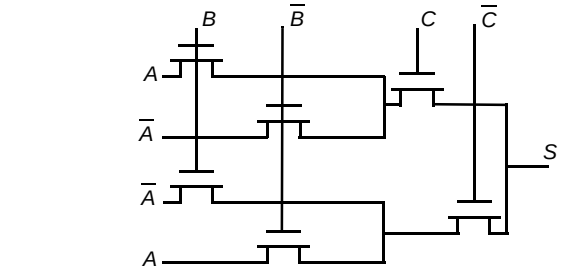
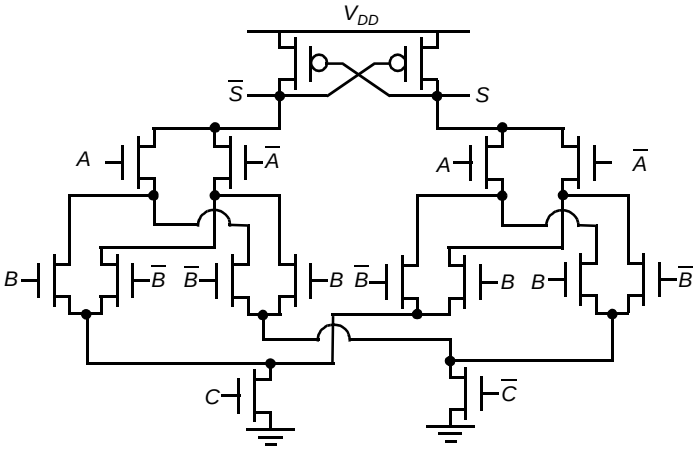
The two cases are shown in the figure below.



Pass Gate Implementation



DCVSL Implementation

14. Describe the logic function computed by the circuit in Figure 6.11. Note that all transistors (except for the middle inverters) are NMOS. Size and simulate the circuit so that it achieves a 100 ps delay (50-50) using 0.25μm devices, while driving a 100 fF load on both differential outputs. (V_{DD} = 2.5V). Assume *A*, *B* and their complements are available as inputs.

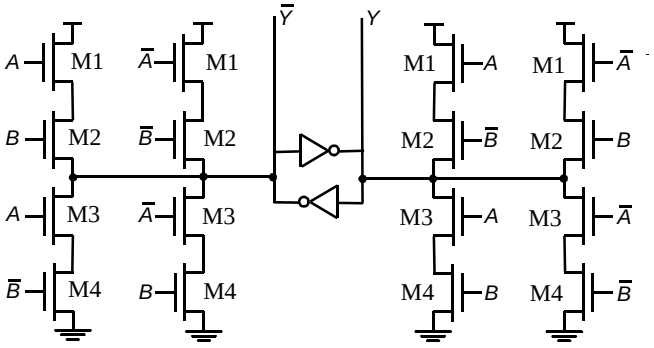


Figure 6.11 Cascoded Logic Styles.

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For the drain and source perimeters and areas you can use the following approximations: AS=AD=W*0.625u and PS=PD=W+1.25u.

15.

Solution

The circuit implements an XOR. The sizes of the transistors are M1: 28u/0.25u, M2: 28u/0.25u, M3: 10u/0.25u, M4: 10u/0.25u. M_{Pinv}: 4u/0.25, M_{Ninv}: 0.375u/10u

16. [M, None. 4.2] Figure 6.12 contains a pass-gate logic network.

a. Determine the truth table for the circuit. What logic function does it implement?

Solution

The truth table is shown below

AB	Out
00	1
01	0
10	0
11	1

The circuit implements an XNOR.

b. Assuming 0 and 2.5 V inputs, size the PMOS transistor to achieve a V_{OL} = 0.3 V.

Solution

The PMOS device will be velocity saturated and the NMOS passgate will be in the linear region. $I_{DN}+I_{DP}=0$, so

$$k'_p \cdot \frac{W}{L} \cdot V_{DSAT} \cdot (V_{GT} - 0.5V_{DSAT}) \cdot (1 + \lambda V_{DS}) + k'_n \cdot \frac{W}{L} \cdot V_o \cdot (V_{GT} - 0.5V_o) \cdot (1 + \lambda V_o) = 0$$

We know that V_o=0.3V, so we can plug in numbers and solve for W/L for the PMOS is 7. Let the PMOS be 1.75/0.25.

c. If the PMOS were removed, would the circuit still function correctly? Does the PMOS transistor serve any useful purpose?

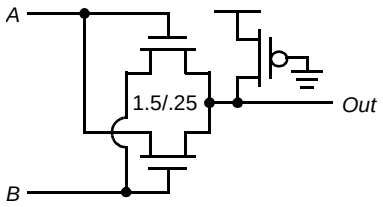

Figure 6.12 Pass-gate network.

Solution

No. If the PMOS were removed, the output node could remain low when AB=00 because it would be floating. The PMOS device pulls the output node high when it would otherwise be in a high impedence state.

17. [M, None, 4.2] This problem considers the effects of process scaling on pass-gate logic.

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a. If a process has a t_{buf} of 0.4 ns, R_{eq} of 8 kΩ, and C of 12 fF, what is the optimal number of stages between buffers in a pass-gate chain?

Solution

$$m_{opt} = 1.7\sqrt{t_p/(R_{eq} \cdot C)} = 3.47 \approx 3 \text{ gates between buffers.}$$

b. Suppose that, if the dimension of this process are shrunk by a factor S, R_{eq} scales as $1/S^2$, C scales as $1/S$, and t_{buf} scales as $1/S^2$. What is the expression for the optimal number of buffers as a function of S? What is this value if $S = 2$?

Solution

$$m_{opt} = 1.7\sqrt{\frac{t_p/S^2}{R_{eq}/S^2 \cdot C/S}} = 1.7\sqrt{\frac{S \cdot t_p}{R_{eq} \cdot C}} = 4.9 \approx 5 \text{ gates between buffers.}$$

18. [C, None, 4.2] Consider the circuit of Figure 6.13. Let C_x = 50 fF, M_r has W/L = 0.375/0.375, M_n has W/L_{eff} = 0.375/0.25. Assume the output inverter doesn't switch until its input equals $V_{DD}/2$.

a. How long will it take M_n to pull down node x from 2.5 V to 1.25 V if In is at 0 V and B is at 2.5V?

Solution

To determine the time required for these transitions, we will find the average currents in the FETs M_r and M_n. The equivalent resistance method will not suffice since it does not account for both devices being on.

For M_r, $I_{VDD=2.5}$ = 0 since V_{DS} = 0. For the other case, the PMOS device is velocity saturated, so:

$I_{VDD=1.25}$ = (-30)(1)(-1)(-2.1+0.5)(1+0.1*1.25) = -54uA. The average current in the PMOS is -27uA.

M_n is in the velocity saturation region for both endpoints of the transition. The two currents are therefore:

$I_{VDD=2.5}$ = (115)(1.5)(0.63)(2.07-0.63/2)(1+0.06*2.5) = 219uA.
$I_{VDD=1.25}$ = (115)(1.5)(0.63)(2.07-0.63/2)(1+0.06*2.5) = 205uA.
And the average current in the NMOS is 212uA.
The total current DISCHARGING the capacitor is 211uA - 27uA = 185uA.
The time for the transition is then

$$t = \frac{C \times \Delta V}{I_{avg}} = \frac{50fF \times 1.25V}{185\mu A} = 338ps.$$

b. How long will it take M_n to pull up node x from 0 V to 1.25 V if V_{In} is 2.5 V and V_B is 2.5 V?

Solution

For the LH transition, the PMOS "keeper" is off. The NMOS Mn is the only FET that is on for this transition. We present both methods for finding the pull-up time.

Equivalent Resistance: We need to perform a different sweep for this measurement than the regular I_D vs V_{DS} sweep. In this case, V_{DS} is changing because the *source node* of the FET is rising. Since the source voltage is changing, V_{GS} also is reducing as node x rises. This effectively "turns down" the current the NMOS can sustain. Performing the appropriate sweep and measuring R_{EQ} gives $R_{EQ} = (11.3k\Omega + 34.7k\Omega)/2 = 23k\Omega$. Thus,
$t = 0.69*C*R_{EQ} = 0.69*50fF*23k\Omega = 794ps$.

Average Current: When x = 0, the pass transistor has a V_{GS} = 2.5 and a V_{DS} = 2.5, so it is velocity saturated.

$I_{x=0}$ = (115)(1.5)(0.63)(2.07-0.63/2)(1+0.06*2.5) = 219uA.

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When x = 1.25, the pass transistor has V_{DS} = 1.25 and V_{GS} = 1.25. It is still velocity saturated, but notice that V_{GS} has decreased. Thus,

$I_{x=1.25}$ = (115)(1.5)(0.63)(1.25-0.43-0.63/2)(1+0.06*1.25) = 59uA.

The average current is then I_{avg} = 139uA.

$$t = \frac{C \times \Delta V}{I_{avg}} = \frac{50fF \times 1.25V}{139\mu A} = 450ps.$$

Clearly, the two solutions are not very close together. The actual **simulated transition time is about 644ps**. The I_{avg} approximation underestimates the solution because the true average current in this case is not close to the average of the endpoints. In a typical inverter (PMOS pullup and NMOS pulldown), V_{GS} doesn't change over the transition, so the current is reasonably linear with V_{DS}. For that case, the average current is close to the average of the endpoints. In this problem, the pinch-off of V_{GS}-V_T in the pass transistor means the average is closer to the smaller value. Numerical calculation of the average current from an HSPICE sim gives I_{avg} = 93uA which would give a transition time of **t = 672ps**, which is much closer to the actual value.

c. What is the minimum value of V_B necessary to pull down V_x to 1.25 V when V_{In} = 0 V?

Solution

In order for M_n to pull node *x* low, the current in M_r must equal or exceed the current that charges up the capacitor at every point in the transition. The maximum current in M_r occurs when x = 1.25 V, and it is (from part a) I_{Mr} = -54uA. We can write a current equation for M_n at this point in the transition and solve for V_B:

Note that M_n is velocity saturated at this point: 54 = 115(1.5)(0.63)(VB-0.43-0.63/2)(1+0.06*1.25).

Solving gives V_B = 1.207V.

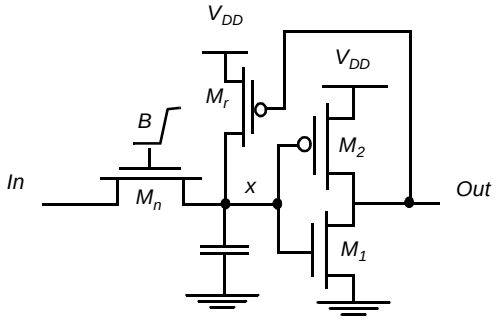

Figure 6.13 Level restorer.

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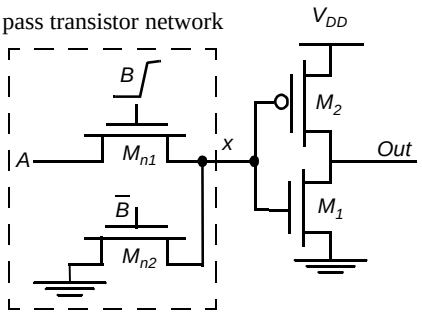
19. Pass Transistor Logic



V_{DD} = 2.5V
$(W/L)_2$ = 1.5um/0.25um
$(W/L)_1$ = 0.5um/0.25um
$(W/L)_{ni}$ = 0.5um/0.25um

k_n' = 115uA/V^2, kp' = -30uA/V^2
V_{tN} = 0.43V, V_{tP} = -0.4V

Figure 6.14 Level restoring circuit.

Consider the circuit of Figure 6.14. Assume the inverter switches ideally at $V_{DD}/2$, neglect body effect, channel length modulation and all parasitic capacitance throughout this problem.

a. What is the logic function performed by this circuit?

Solution

The circuit is a NAND gate.

b. Explain why this circuit has non-zero static dissipation.

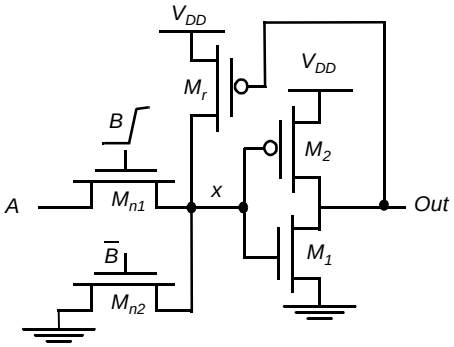
Solution

When A=B= V_{DD}, the voltage at node x is $V_X=V_{DD}-V_{tN}$. This causes static power dissipation at the inverter the pass transistor network is driving.

c. Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.

Solution

The modified circuit is shown in the next figure.



The size of M_r should be chosen so that when one of the inputs A or B equals 0, either M_{n1} or M_{n2}, would be able to pull node X to $V_{DD}/2$ or less.

d. Implement the same circuit using transmission gates.

Solution

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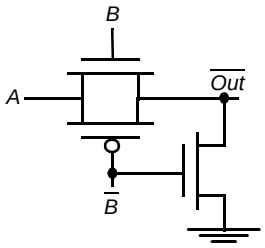
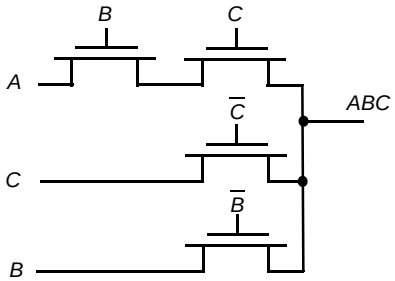
The circuit is shown below.



e. Replace the pass-transistor network in Figure 6.14 with a pass transistor network that computes the following function: $x = ABC$ at the node x. Assume you have the true and complementary versions of the three inputs A,B and C.

Solution

One possible implementation is shown.



20. [M, None, 4.3] Sketch the waveforms at *x*, *y*, and *z* for the given inputs (Figure 6.15). You may approximate the time scale, but be sure to compute the voltage levels. Assume that $V_T = 0.5$ V when body effect is a factor.

21. [E, None, 4.3] Consider the circuit of Figure 6.16.

a. Give the logic function of *x* and *y* in terms of *A, B,* and *C*. Sketch the waveforms at *x* and *y* for the given inputs. Do *x* and *y* evaluate to the values you expected from their logic functions? Explain.

Solution

$$x = \overline{AB} \text{ and } y = AB\overline{C}$$

The circuit does not correctly implement the desired logic function. This stems from the fact that x is pre-charged high, and thus node y is discharged as soon as the evaluation phase starts. Although x is eventually discharged by the first stage, y cannot be charged high again since it is a dynamic node with no low-impedance path to Vdd (during evaluate). Common solutions to this problem areto either place an inverter between the two stages (thus allowing only 0-to-1 transitions on the inputs to each stage during evaluate) as in Domino logic or employing np-CMOS. The latter is presented in (b).

b. Redesign the gates using *np*-CMOS to eliminate any race conditions. Sketch the waveforms at *x* and *y* for your new circuit.

Solution

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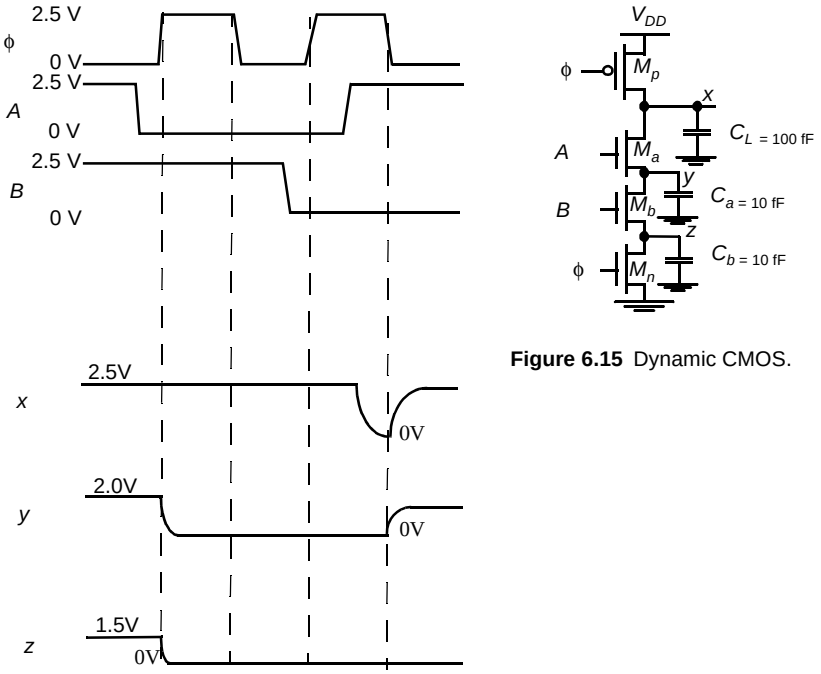


Figure 6.15 Dynamic CMOS.

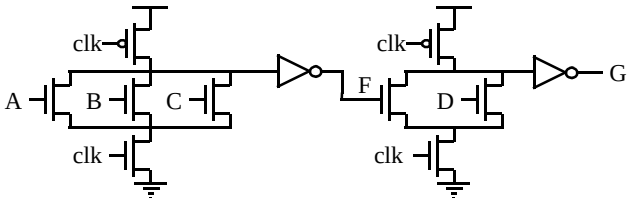
The modified circuit using np-CMOS is shown below together with the waveforms at x and y. The desired logic function is now correctly implemented

22. [M, None, 4.3] Suppose we wish to implement the two logic functions given by $F = A + B + C$ and $G = A + B + C + D$. Assume both true and complementary signals are available.

a. Implement these functions in dynamic CMOS as cascaded ϕ stages so as to minimize the total transistor count.

Solution

Dynamic gates with NMOS pull-down networks cannot be directly cascaded. This solution uses a domino logic approach.



b. Design an *np*-CMOS implementation of the same logic functions.

Solution

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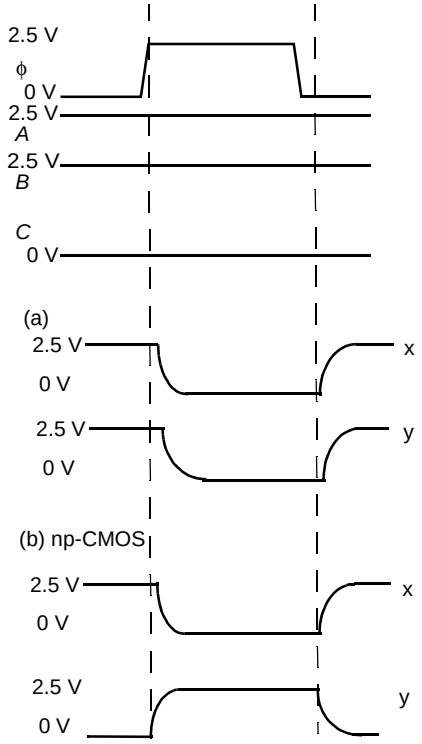


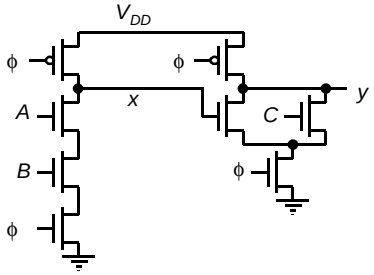
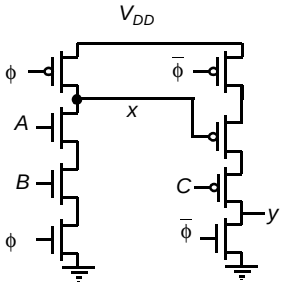
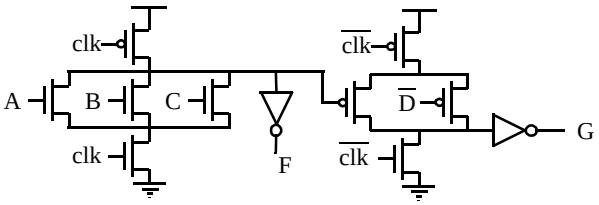


Figure 6.16 Cascaded dynamic gates.



The circuit is shown below



23. Consider a conventional 4-stage Domino logic circuit as shown in Figure 6.17 in which all precharge and evaluate devices are clocked using a common clock ϕ. For this entire problem, assume that the pulldown network is simply a single NMOS device, so that each Domino stage consists of a dynamic inverter followed by a static inverter. Assume that the precharge

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time, evaluate time, and propagation delay of the static inverter are all *T*/2. Assume that the transitions are ideal (zero rise/fall times).

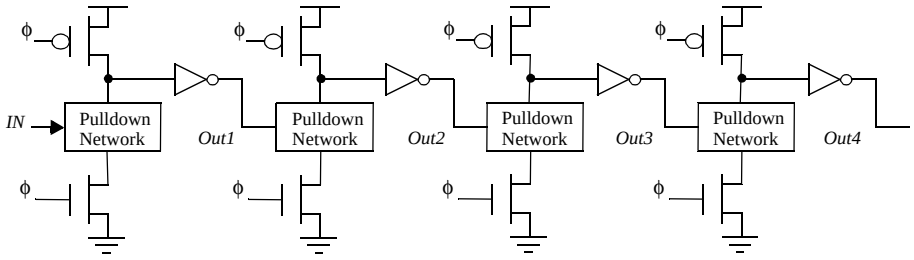
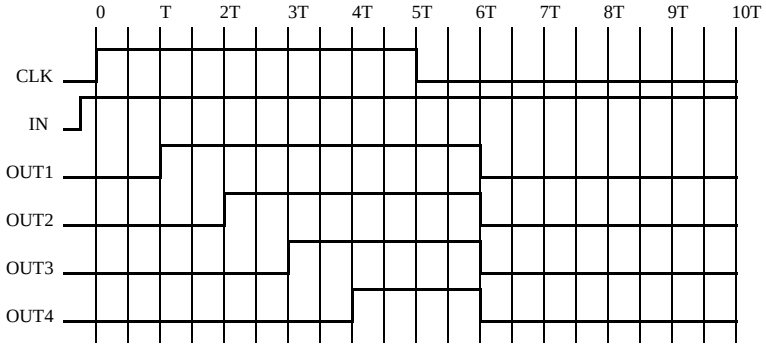


Figure 6.17 Conventional DOMINO Dynamic Logic.

a. Complete the timing diagram for signals Out_1, Out_2, Out_3 and Out_4, when the *IN* signal goes high before the rising edge of the clock ϕ. Assume that the clock period is 10 T time units.

Solution

The timing diagram is shown below.



b. Suppose that there are no evaluate switches at the 3 latter stages. Assume that the clock ϕ is initially in the precharge state (ϕ=0 with all nodes settled to the correct precharge states), and the block enters the evaluate period (ϕ=1). Is there a problem during the evaluate period, or is there a benefit? Explain.

Solution

There is no problem during the evaluate stage. The precharged nodes remain charged until a signal propogates through the logic, activating the pull-down network and discharging the node. In fact, this topology improves the circuit's robustness in terms of charge sharing affecting the output for any generic pull-down network, and reduces the body effect in the pull-down network.

c. Assume that the clock ϕ is initially in the evaluate state (ϕ=1), and the block enters the precharge state (ϕ = 0). Is there a problem, or is there any benefit, if the last three evaluate switches are removed? Explain.

Solution

There is a problem during the precharge stage. If all precharged nodes are discharged during the evaluate stage, when the precharge FETs simultaneously turn on, the pull-down

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networks will initially remain on, creating a short circuit. This continues in each gate until the previous gate charges, disabling its pull-down network.

24. [C, Spice, 4.3] Figure 6.18 shows a dynamic CMOS circuit in Domino logic. In determining source and drain areas and perimeters, you may use the following approximations: $AD = AS = W \times 0.625\mu m$ and $PD = PS = W + 1.25\mu m$. Assume 0.1 ns rise/fall times for all inputs, including the clock. Furthermore, you may assume that all the inputs and their complements are available, and that all inputs change during the precharge phase of the clock cycle.

a. What Boolean functions are implemented at outputs *F* and *G*? If *A* and *B* are interpreted as two-bit binary words, $A = A_1A_0$ and $B = B_1B_0$, then what interpretation can be applied to output *G*?

Solution

$$F = A_0B_0 + \overline{A}_1\overline{B}_1,\ G = F(A_0B_0 + \overline{A}_1\overline{B}_1)$$

If *A* and *B* are interpreted as two-bit binary words, output *G* is high if *A* = *B*: a comparator

b. Which gate (1 or 2) has the highest potential for harmful charge sharing and why? What sequence of inputs (spanning two clock cycles) results in the worst-case charge-sharing scenario? Using SPICE, determine the extent to which charge sharing affects the circuit for this worst case.

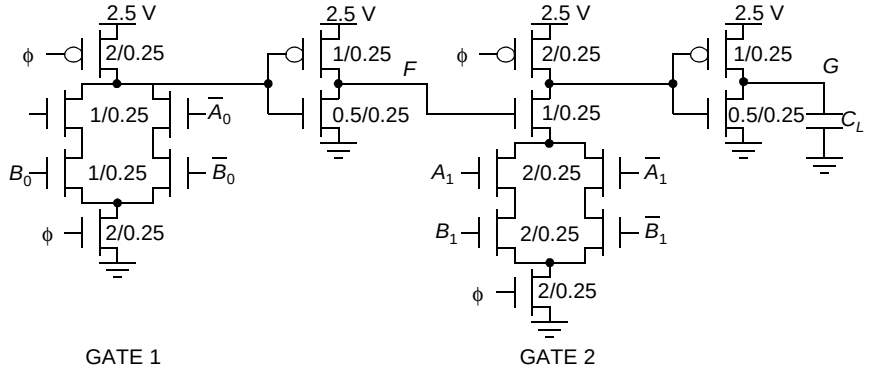

Figure 6.18 DOMINO logic circuit.

Solution

Gate 2 has the higher potential for harmful charge sharing because the capacitance that contributes to charge sharing is larger than in gate 1.

The sequence of inputs resulting in the worst-case charge sharing is $A_0 = B_0$ and $A_1 = B_1$ for the first cycle. Then $A_0 = B_0$ and $A_1 \neq B_1$ for the second cycle such that $A_1/\overline{A}_1$ transistor that is on during the second cycle is the same as in the first cycle. For example, $A_0 = B_0 = A_1 = B_1 = V_{DD}$ in cycle 1 and $A_0 = B_0 = A_1 = V_{DD}$, $B_1 = 0$ V in cycle 2. This

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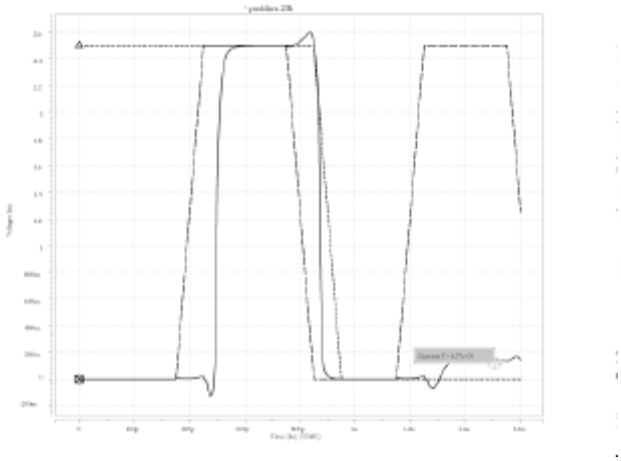
will cause the charge at the output of gate 2 to be shared with the total parasitic capacitance at the drains of the A_1, $\overline{A}_1$, and B_1 transistors.

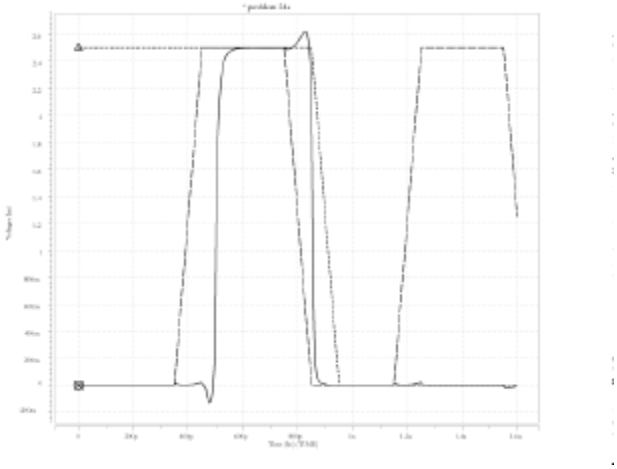


25. [M, Spice, 4.3] In this problem you will consider methods for eliminating charge sharing in the circuit of Figure 6.18. You will then determine the performance of the resulting circuit.

a. In problem 24 you determined which gate (1 or 2) suffers the most from charge sharing. Add a single 2/0.25 PMOS precharge transistor (with its gate driven by the clock ϕ and its source connected to V_{DD}) to one of the nodes in that gate to maximally reduce the charge-sharing effect. What effect (if any) will this addition have on the gate delay? Use SPICE to demonstrate that the additional transistor has eliminated charge sharing for the previously determined worst-case sequence of inputs.

Solution

The additional precharge transistor should charge the node that is shared by the A_1 and $\overline{A}_1$ transistor drains and the F transistor source. Assuming the gate delay is dominated by the precharge stage, this will reduce the gate delay by briefly aiding the precharging of gate 2. SPICE output with additional precharge transistor.



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b. For the new circuit (including additional precharge transistor), find the sequence of inputs (spanning two clock cycles) that results in the worst-case delay through the circuit. Remember that precharging is another factor that limits the maximum clocking frequency of the circuit, so your input sequence should address the worst-case precharging delay.

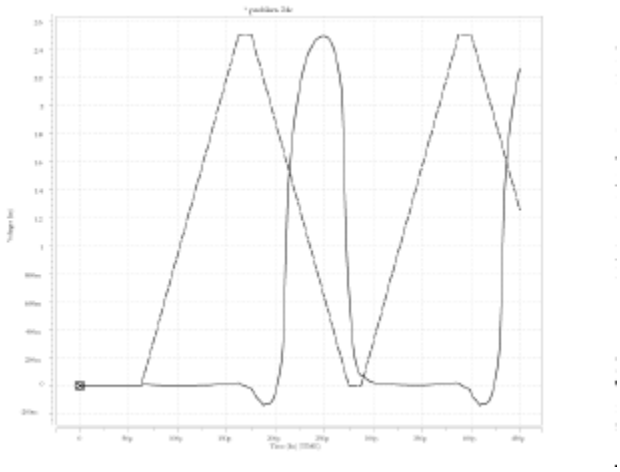
Solution

The worst-case delay results from $A = B$ for two consecutive cycles. This results in the maximum charging and discharging of the internal nodes

c. Using SPICE on the new circuit and applying the sequence of inputs found in part (b), find the maximum clock frequency for correct operation of the circuit. Remember that the precharge cycle must be long enough to allow all precharged nodes to reach ~90% of their final values before evaluation begins. Also, recall that the inputs (*A*, *B* and their complements) should not begin changing until the clock signal has reached 0 V (precharge phase), and they should reach their final values before the circuit enters the evaluation phase.

Solution

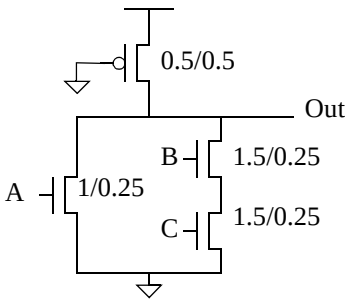
The maximum clock frequency is ~4.4 GHz.



26. [C, None, 4.2–3] For this problem, refer to the layout of Figure 6.19.

a. Draw the schematic corresponding to the layout. Include transistor sizes.

Solution



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b. What logic function does the circuit implement? To which logic family does the circuit belong?

Solution

The circuit implements Out = $\overline{A+BC}$. It is in the pseudo NMOS family.

c. Does the circuit have any advantages over fully complementary CMOS?

Solution

The circuit uses less area than a fully complementary CMOS implementation.

d. Calculate the worst-case V_{OL} and V_{OH}.

Solution

$V_{OH} = V_{DD} = 2.5V$. To find V_{OL}, assume that we can combine M_B and M_C into one NMOS with W/L = 0.75/0.25. Then the worst case V_{OL} occurs when A=0 and the combined BC NMOS is on. Assume that V_{OL} is less than V_{DSATn}. Then the NMOS device is in the linear region. The PMOS device will be velocity saturated. Equating the currents at the output gives:

$$k'_p \cdot \frac{W}{L} \cdot V_{DSAT} \cdot (V_{GT} - 0.5V_{DSAT}) \cdot (1 + \lambda V_{DS}) + k'_n \cdot \frac{W}{L} \cdot V_o \cdot (V_{GT} - 0.5V_o) \cdot (1 + \lambda V_o) = 0$$

The only unknown in this 3rd order polynomial is V_o. Solving for V_o gives V_{OL}= 51.2mV

e. Write the expresions for the area and perimeter of the drain and source for all of the FETs in terms of λ. Assume that the capacitance of shared diffuusions divides evenly between the sharing devices. Copy the layout into Magic, extract and simulate to find the worst-case t_{pHL} time. For what input transition(s) does this occur? Name all of the parasitic capacitances that you would need to know to calculate this delay by habd (you do not need to perform the calculation).

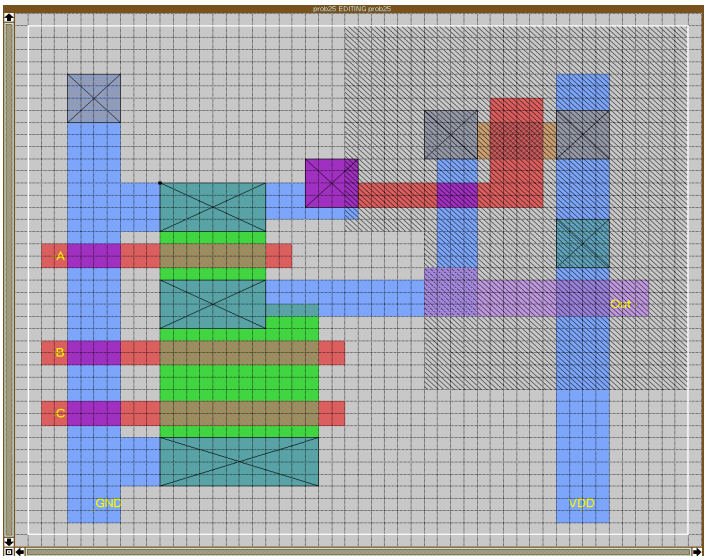

Figure 6.19 Layout of complex gate.

Solution

Call the PMOS device P, and name the other devices by their input signal.
$AD_P = AS_P = 19\lambda^2$. $PD_P = PS_P = 15\lambda$.
$AS_A = 40\lambda^2$. $PS_A = 18\lambda$.

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$AD_A = (3x8 + 3x12)\lambda^2 / 2 = 30\lambda^2$. $PD_A = 16\lambda/2 = 8\lambda$.
$AD_B = AD_A$. $PD_B = PD_A$.
$AS_B = 36\lambda^2/2 = 18\lambda^2$. $PS_B = 6\lambda/2 = 3\lambda$.
$AD_C = AS_B$. $PD_C = PS_C$.
$AS_C = 60\lambda^2$. $PS_C = 22\lambda$.

We can narrow the number of transitions to look at for determining the worst case t_{pHL}. The worst case capacitance occurs when the internal node between M_B and M_C is charged up to V_{DD}. Then the worst case delay will occur when either M_A or the M_B, M_C pair discharges this capacitance. If the series devices are doing the discharging, we need to consider the case where M_B is initially on and where M_B is initially off.

The simulation shows that the worst-case transition occurs over three cycles: ABC = 010 to 000 to 011 produces the worst-case t_{pHL}. This is worse than when MA discharges the node (ABC = 010 to 110) or when MB is initially on (ABC = 010 to 011).

We could calculate t_{pHL} using either the equivalent resistance method or the average current method. In either case, C_L would include the following parasitic capacitances:

$C_{GDPMOS} + C_{DBPMOS} + C_{GDA}$(no Miller effect b/c input not changing) + $C_{DBA} + C_{GDB} + C_{DBB} + C_{GSB} + C_{GDC} + C_{DBC}$.

27. [E, None, 4.4] Derive the truth table, state transition graph, and output transition probabilities for a three-input XOR gate with independent, identically distributed, uniform white-noise inputs.

Solution

The truth table of a three-input XOR gate is:

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table 1: Truth table

As the inputs are independent, identically distribute, uniform white noise, each of the possible combinations of three input values, has a probability equal to 1/8. From the table, the probabiliy of having the output equal to 0 is $p_0 = 0.5$. In the same way

28. [C, None, 4.4] Figure 6.20 shows a two-input multiplexer. For this problem, assume independent, identically-distributed uniform white noise inputs.

a. Does this schematic contain reconvergent fan-out? Explain your answer.

Solution

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This schematic has reconvergent fan-out because both inputs of the or gate depend on the value of S.

b. Find the exact signal (P_1) and transition ($P_{0\to1}$) formulas for nodes *X*, *Y*, and *Z* for: (1) a static, fully complementary CMOS implementation, and (2) a dynamic CMOS implementation.

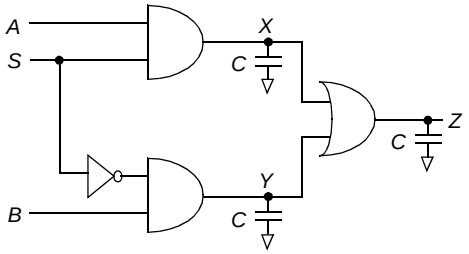

Figure 6.20 Two-input multiplexer

Solution

Assuming a fully complementary CMOS implementation:

X is the output of an AND gate with independent, identically-distributed uniform white noise inputs. As only when both inputs are equal to 1 the output is 1, $P_1 = 0.25$. On the other hand $P_{0\to1} = P_0P_1 = 0.25(1-0.25) = 0.1875$.

Y is also the output of an AND gate with independent, identically distributed uniform white noise inputs. The analysis is the same as with X.

If we represent the truth table of the schematic we will see that $P_1 = 0.5$. Then $P_{0\to1} = P_0P_1 = 0.5(1-0.5) = 0.25$.

Assuming a dynamic CMOS implementation:

In the same way as before, for X, $P_1 = 0.25$. In order to obtain the transition probability, an n-tree dynamic gate will be assumed. In this case: $P_{0\to1} = P_0 = 0.75$.

The analisys for Y is equal to the analysis for X.

For Z, using the truth table of the schematic we obtain, again , $P_1 = 0.5$. For the transition probability, it will be assumed that a np-CMOS structure is used.. Then, Z is the output of a p-tree dynamic gate. Then: $P_{0\to1} = P_1 = 0.5$.

29. [M, None, 4.4] Compute the switching power consumed by the multiplexer of Figure 6.20, assuming that all significant capacitances have been lumped into the three capacitors shown in the figure, where C = 0.3 pF. Assume that V_{DD} = 2.5 V and independent, identically-distributed uniform white noise inputs, with events occuring at a frequency of 100 MHz. Perform this calculation for the following:

a. A static, fully-complementary CMOS implementation

Solution

Switching power is:

$$P_{SW} = \alpha \cdot f \cdot C \cdot V_{DD}^2 = (\alpha_{X0\to1} + \alpha_{Y0\to1} + \alpha_{Z0\to1}) \cdot f \cdot C \cdot V_{DD}^2$$

We calculated in Problem 27 the probabilities of a 0->1 transistion for each node: $P_{0\to1}$ for X and Y is 0.1875 and $P_{0\to1}$ for Z is 0.25.
Thus, P_{SW} = (2*0.1875+0.25)*100MHz*0.3pF*2.5^2 = 117.2uW.

b. A dynamic CMOS implementation

Solution

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In Problem 27 for a dynamic np-CMOS gate, we calculated the probabilities: $P_{0\to 1}$ for X and Y is 0.75 and $P_{0\to 1}$ for Z is 0.5. Thus, P_{SW} = (2*0.75+0.5)*100MHz*0.3pF*2.5^2 = 375uW.

30. For the circuit shown Figure 6.21 ignore DIBL and S=100mV/decade.

a. What is the logic function implemented by this circuit? Assume that all devices (M1-M6) are 0.5µm/0.25µm.

Solution

$\overline{A(B+C)}$

b. Let the drain current for each device (NMOS and PMOS) be 1µA for NMOS at $V_{GS}= V_T$ and PMOS at $V_{SG}= V_T$. What input vectors cause the worst case leakage power for each output value? Explain (state all the vectors, but do not evaluate the leakage).

Solution

When the output is high, the worst-case leakage occurs when two transistors leak in parallel: ABC = 100.When the output is low, the worst-case leakage also occurs when two transistors leak in parallel: ABC = 110 or ABC = 101.

c. Suppose the circuit is active for a fraction of time *d* and idle for *(1-d)*. When the circuit is active, the inputs arrive at 100 MHz and are uniformly distributed ($Pr_{(A=1)}$ = 0.5, $Pr_{(B=1)}$ = 0.5, $Pr_{(C=1)}$ = 0.5) and independent. When the circuit is in the idle mode, the inputs are fixed to one you chose in part (b). What is the duty cycle *d* for which the active power is equal to the leakage power?

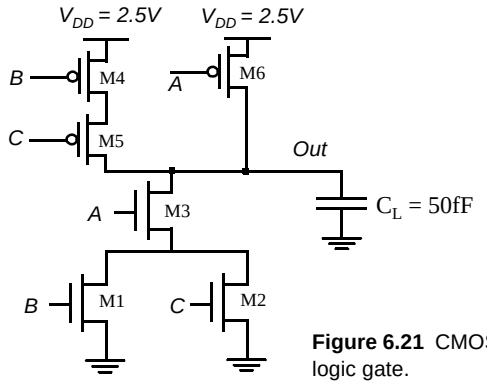

Figure 6.21 CMOS logic gate.

Solution

$d*P_{active} = (1-d)\ P_{leakage}$. $P_{active} = \alpha_{0->1}*f*C_L*V_{DD}^2$ = (3/8 * 5/8)*(100*10^6)*(50*10^{-15})*(2.5^2) = 7.3µ W.

$P_{leakage}$ (ABC = 100) = $V_{DD}*2*I_{leakM1}$ = 5* $I_o 10^{\frac{-V_T}{S}}$ = 5* 1$uA10^{\frac{-0.43}{0.1}}$ = 251pW.

Plugging the power numbers into the activity equation and solving for d gives d = 3.4*10^{-8}.

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DESIGN PROJECT

Design, lay out, and simulate a CMOS four-input XOR gate in the standard 0.25 micron CMOS process. You can choose any logic circuit style, and you are free to choose how many stages of logic to use: you could use one large logic gate or a combination of smaller logic gates. The supply voltage is set at 2.5 V! Your circuit must drive an external 20 fF load in addition to whatever internal parasitics are present in your circuit.

The primary design objective is to minimize the propagation delay of the worst-case transition for your circuit. The secondary objective is to minimize the area of the layout. At the very worst, your design must have a propagation delay of no more than 0.5 ns and occupy an area of no more than 500 square microns, but the faster and smaller your circuit, the better. Be aware that, when using dynamic logic, the precharge time should be made part of the delay.

The design will be graded on the magnitude of $A \times t_p^2$, the product of the area of your design and the square of the delay for the worst-case transition.

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