**Faculty of Engineering and Technology**
**Department of Electrical and Computer Engineering**

# ENCS3330 | Digital Integrated Circuits

## Course Syllabus

| Course Information | |
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| **Course Title** | **Digital Integrated Circuits** |
| **Course Number** | **ENCS3330** |
| **Prerequisites** | ENCS2340 and ENEE2360 |
| **Semester** | First Semester 2023/2024 |

| Instructors | | | | | |
|---|---|---|---|---|---|
| **Name** | **Email** | **Sections** | **Office Number** | **Office Hours** | **Class Time and Venue** |
| Dr. Khader Mohammad | khamadawwad@birzeit.edu | 1,2 | Masri218 | See Ritaj | See Ritaj |

## References

- Handouts /lectures notes
- Rabaey, Jan, Anantha Chandrakasan, and Bora Nikolic. Digital Integrated Circuits: A Design Perspective. 2nd ed. Upper Saddle River, NJ: Prentice-Hall, 2002. ISBN: 0130909963.
- Analysis and design of Digital Integrated Circuits: David Hodges et. al.
- Principles of CMOS VLSI Design by N. Weste and K. Eshraghian

## BZU Catalogue Course Description

Analysis and design of digital integrated circuits; MOS logic circuit families; logic gate construction, modeling MOS devices - equations and SPICE models, MOS invertors; voltage transfer characteristics; noise margin; propagation delay; MOS logic circuits; static logic; transfer gates; clocked static circuits; dynamic logic; Precharged logic; domino CMOS; buffer and I/O circuits; high capacitance drivers; semiconductor memories-DRAM, SRAM, ROM. A set of laboratory experiments will provide hands-on experience.

## Course Summary and Objectives

- In this course, we will study the fundamental structures of digital integrated circuit systems. We start by looking at the MOS transistors (n-channel and p-channel) and how we can use them to create the most basic structure—the digital switch. We can proceed to build a range of VLSI structures from this switch, including NAND/NOR gates, Multiplexers, Latches, and Registers. Continuing in a bottom-up fashion, we can examine the structure of more complex VLSI design components (those at Digital Logic and Register Transfer levels of abstraction) using these primitives.
- We will also learn about the processes associated with fabricating CMOS devices. Using CMOS as our technology, we examine the circuit level design rules associated with circuit geometries and their layout according to a set of process technology-specific design rules. We also look at factors affecting design: capacitance, resistance, clocking, delay, and power. Part of the course will tackle the issue of reliability and how an integrated circuit is qualified to meet user requirements and environmental issues.
- Students at the end of the course should be able to:
    - Use mathematical methods and circuit analysis models in the analysis of CMOS digital electronics circuits, including logic components, and interconnect.
    - Create models of moderately sized CMOS circuits that realize specified digital functions.
    - Apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and verify the functionality, timing, power, and parasitic effects.
    - Have an understanding of the characteristics of CMOS circuit construction

**ABET OUTCOMES**

B: Ability to design and conduct experiments, analyze and interpret data,

C: Ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, sustainability political, ethical, health and safety, manufacturability, and

K: Ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

| **Course Topics and Schedule** | |
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| **Week No.** | **Topic** |
| **W1-2** | **Introduction and Review: Basic R, L, and C** |
| **W3** | **IC Manufacturing and Design Metrics CMOS -Ch1 Sec 1.3, Ch2 Sec 2.2** |
| **W4** | **Design Flow** |
| **W5** | **Semiconductor material: PN-junction, NMOS, PMOS -Ch3** |
| **W6** | **Transistor Theory** |
| **W7** | **Transient Response I-V curves. Ch5.2 and ch5.3** |
| **W8** | **The CMOS Inverter- Ch3, Ch5**<br>**Basic Library cell layout: Inverter and basic gates ch2.3-ch7** |
| **W9** | **Logical Effort, Simulation and Timing Ch7.2-7.5** |
| **W10** | **Combinational Circuit Design**<br>**Combinational /static logic structures Ch6.1-2** |
| **W11** | **Sequential logic gates; Latches and Flip-Flops Ch7.4- Ch10.** |
| **W12** | **Clock/Wires/Interconnect Wire modeling - Ch4** |

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| **W13** | **Introduction to: Packaging, Power, & Clock**<br>**Introduction to: Design for Testability** |
| **W14** | **Adders** |
| **W15** | **SRAM** |
| **If time Allows** | **Datapath's**<br>**ROMs, CAMs, & PLAs**<br>**Scaling**<br>**Pitfalls & Reliability**<br>**I/O** |

| **Assessment Policy** | |
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| **Assessment Type** | **Weight** |
| Informative pup up Quizzes (3 QZ's) | 15% |
| Assignments ( Assignments) | 10% |
| Midterm Exam | 20% |
| Course Project/ | 15% |
| Final Exam | 40% |
| **Total** | **100%** |

| **Teaching and Learning Methods** |
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| • Lectures, assignments, in-class activities, exams, and term paper.<br>• Mixture of modern learning methods, such as, inductive learning, flipped classroom, learning by project, etc. |

| **Additional Notes** | |
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| **Assignments** | No late assignments |
| **Exams** | Comprehensive exams |
| **Makeup Exams** | **No makeup exam** |
| **Drop Date** | TBA |
| **Attendance** | Your attendances is very important |
| **Key to a good grade** | Reading the **TEXTBOOK and HANDOUT + DOING the PROJECTS** |
| **Participation** | Students are highly encouraged to participate and ask questions in the class |
| **Office Hours** | Students are highly encouraged to utilize the instructor's office hours |
| **Honor Code** | Students are expected to abide by Birzeit University honor code on all aspects of their academic work. Please review that on Ritaj. Additionally, |

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| | students are expected to follow the code of conduct for the course appended to this course outline. |
| **Code of Conduct** | By enrolling in this course, students agree to abide by a code of conduct that helps all participants gain the best results in a healthy and pleasant environment, This includes the following rules:<br>• Mutual respect is a must<br>• Students are expected to be in class on time<br>• Cell phones should be switched off<br>• Classroom should be very quiet<br>• Students are expected to stay in the classroom focusing and quiet, and not leaving the class room without asking the instructor's permission |