BIRZEIT UNIVERSITY

DEPARTMENT OF COMPUTER SYSTEM ENGINEERING

Digital Integrated Circuits - ENCS333

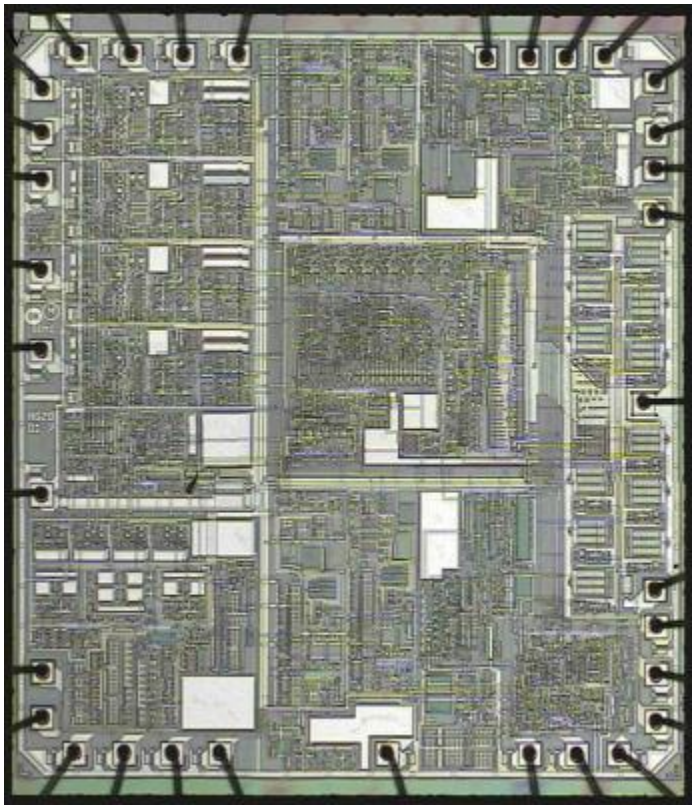
Dr. Khader Mohammad

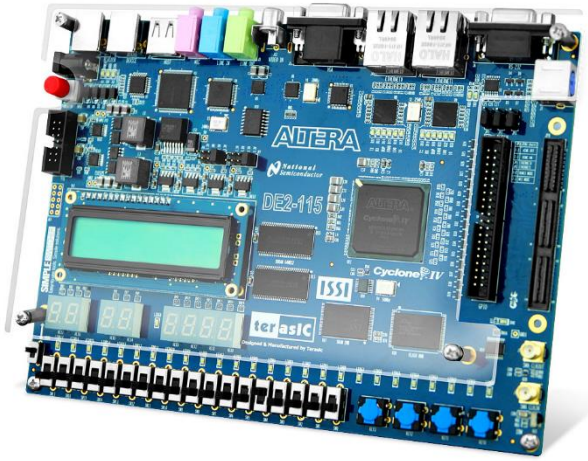
Lecture #0- Introduction

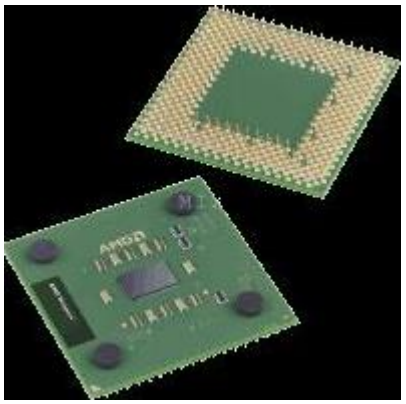
Integrated-Circuit Devices and Modeling

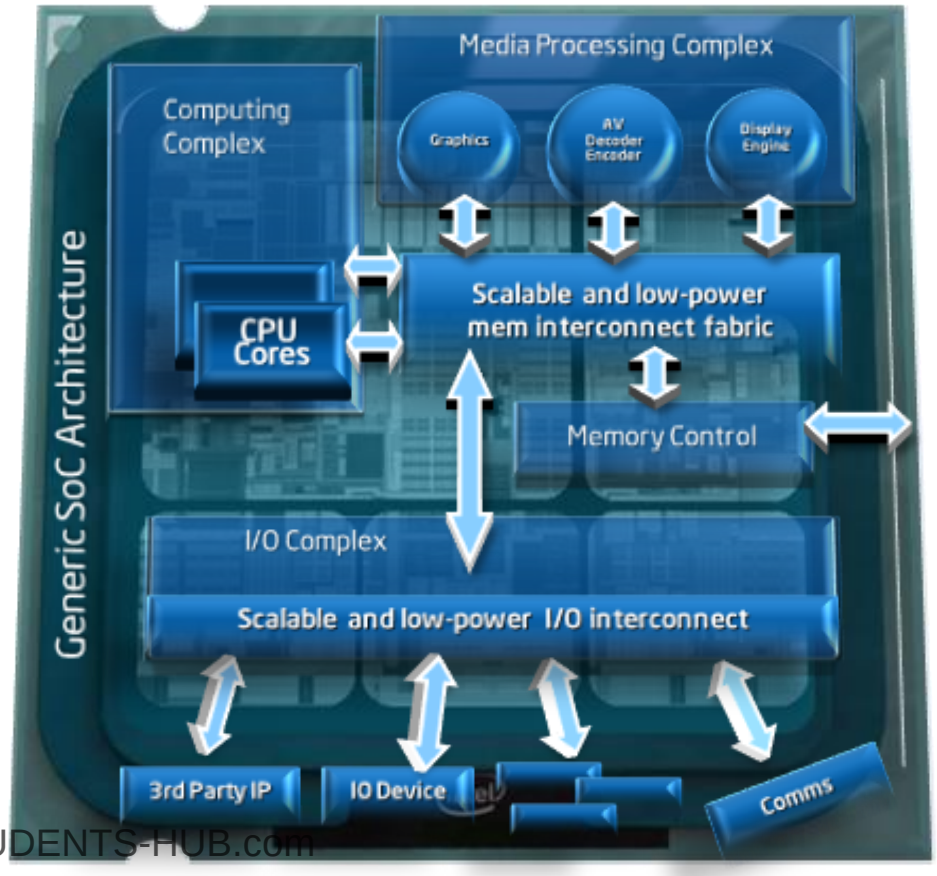
Integrated circuits (ICs)

- Integrated circuits (ICs) are a keystone of modern electronics
- IC is a collection of electronic components – resistors, transistors, capacitors
- All stuffed into a tiny chip, and connected together to achieve a common goal
- Inside the IC : “The real “meat” to an IC is a complex layering of semiconductor wafers, copper, and other materials, which interconnect to form transistors, resistors or other components in a circuit.”
- IC Packages : The package is what encapsulates the integrated circuit die and splays it out into a device we can more easily connect to.

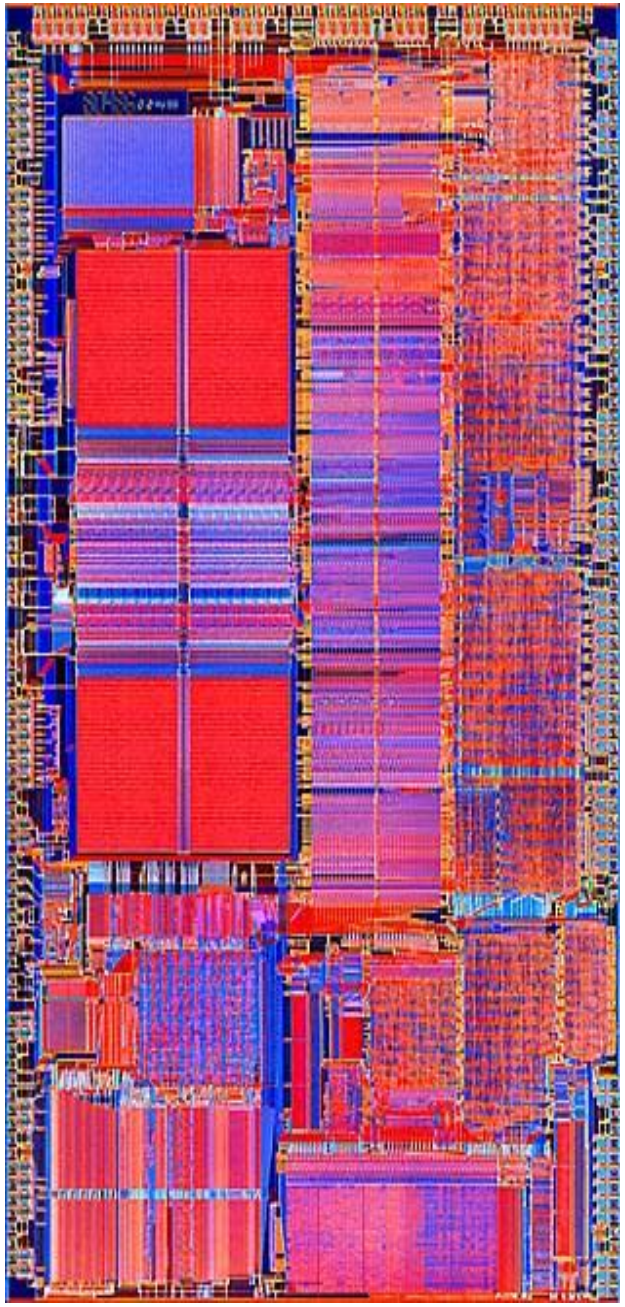




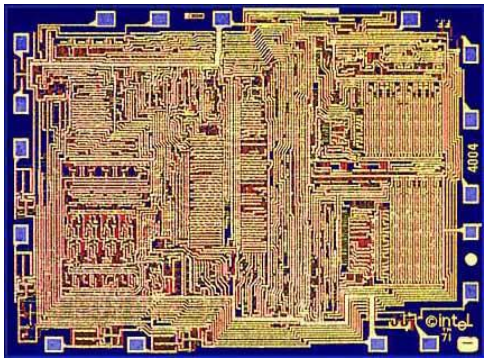




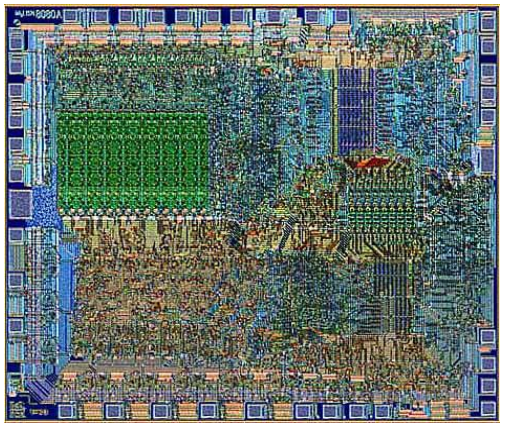
Intel 8486



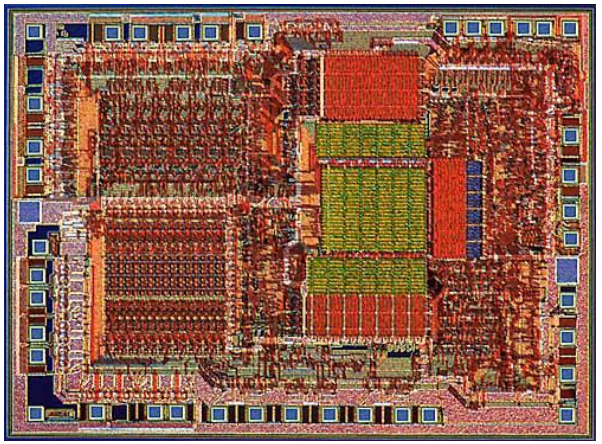
Technology Evolution: Intel CPU Chips



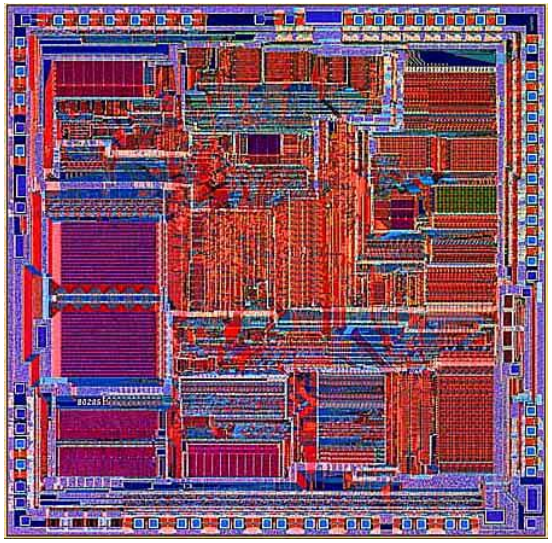
Intel 4004 (‘71)



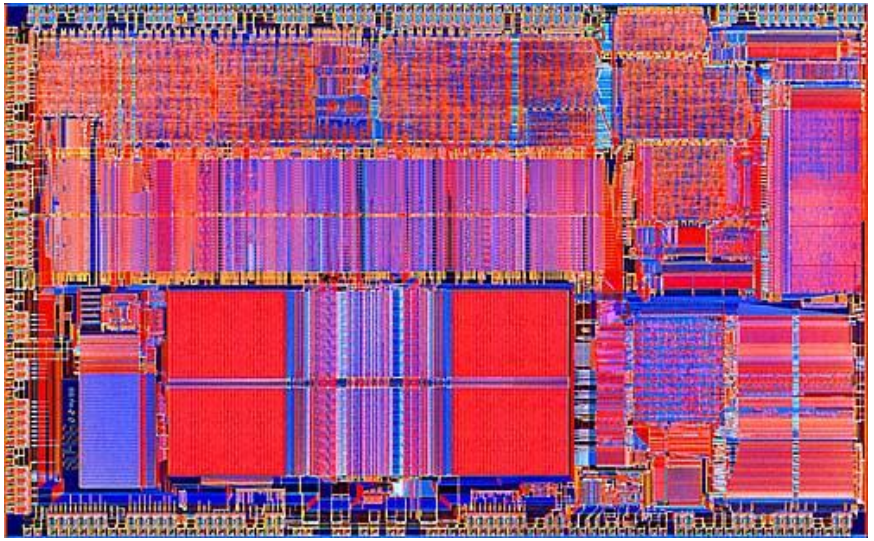
Intel 8080



Intel 8085

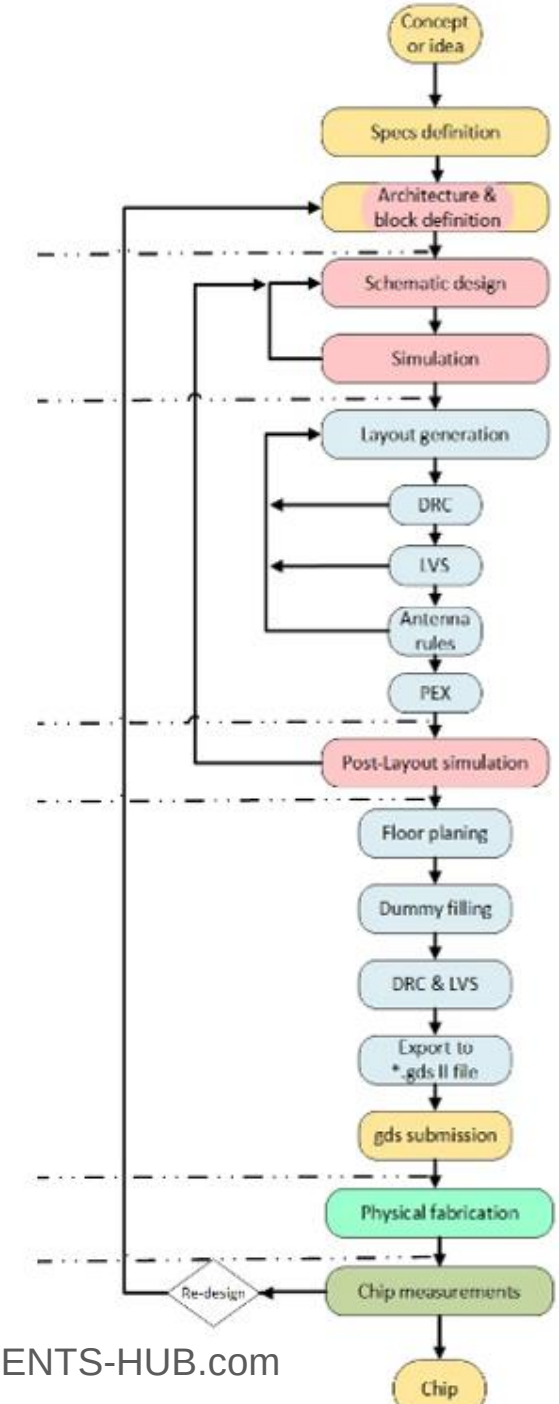


Intel 8286



Intel 8486

Courtesy Intel



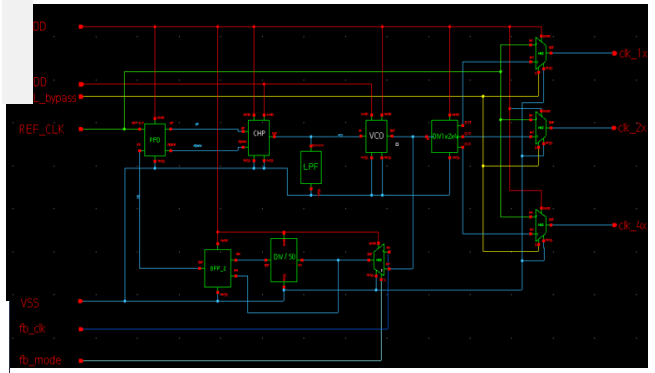
1. Multi-Core Technology
2. CPU Sockets
3. Chipsets
4. Frequency (Clock Rate)

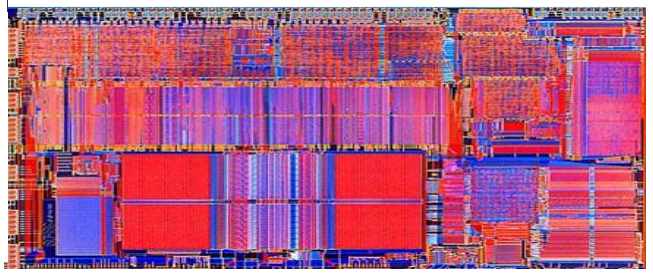
Verilog code for data memory:

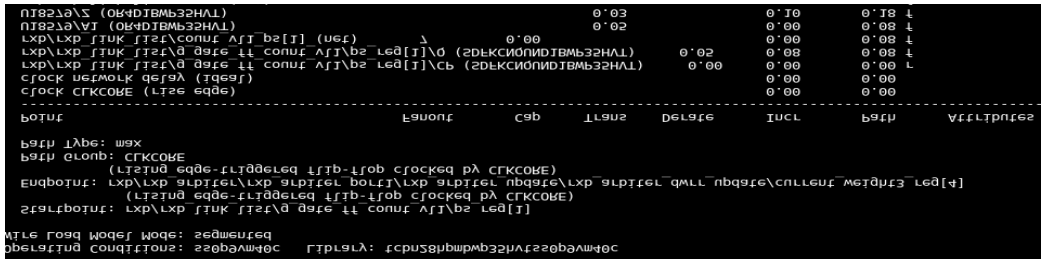
```
//fpga4student.com: FPGA projects, Verilog projects, VHDL projects
// Verilog project: Verilog code for 16-bit MIPS Processor
// Submodule: Data memory in Verilog
module data_memory
(
    input                clk,
    // address input, shared by read and write port
    input     [15:0]     mem_access_addr,
    // write port
    input     [15:0]     mem_write_data,
    input                mem_write_en,
    input mem_read,
    // read port
    output    [15:0]     mem_read_data
);
    integer i;
    reg [15:0] ram [255:0];
    wire [7 : 0] ram_addr = mem_access_addr[8 : 1];
    initial begin
        for(i=0;i<256;i=i+1)
            ram[i] <= 16'd0;
    end
    always @(posedge clk) begin
        if (mem_write_en)
            ram[ram_addr] <= mem_write_data;
    end
    assign mem_read_data = (mem_read==1'b1) ? ram[ram_addr]: 16'd0;
endmodule
```

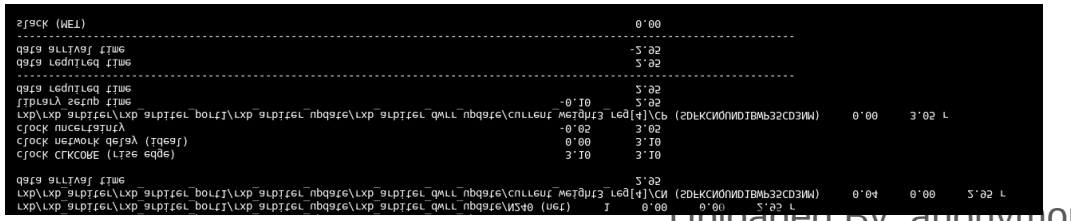
Verilog code for ALU Control unit:

```
//fpga4student.com: FPGA projects, Verilog projects, VHDL projects
// Verilog project: Verilog code for 16-bit MIPS Processor
// Submodule: ALU Control Unit in Verilog
module ALUControl( ALU_Control, ALUOp, Function);
output reg[2:0] ALU_Control;
input [1:0] ALUOp;
input [3:0] Function;
wire [5:0] ALUControlIn;
assign ALUControlIn = {ALUOp,Function};
always @(ALUControlIn)
casex (ALUControlIn)
 6'b11xxxx: ALU_Control=3'b000;
 6'b10xxxx: ALU_Control=3'b100;
 6'b01xxxx: ALU_Control=3'b001;
 6'b000000: ALU_Control=3'b000;
 6'b000001: ALU_Control=3'b001;
 6'b000010: ALU_Control=3'b010;
 6'b000011: ALU_Control=3'b011;
 6'b000100: ALU_Control=3'b100;
 default: ALU_Control=3'b000;
 endcase
endmodule
// Verilog code for JR control unit
module JR_Control( input[1:0] alu_op,
      input [3:0] funct,
      output JRControl
    );
assign JRControl = ({alu_op,funct}==6'b001000) ? 1'b1 : 1'b0;
endmodule
```









Course Content

Lecture 0: Introduction

Lecture 1: Circuits & Layout

- Review: Basic R, L, and C
- IC Manufacturing and Design Metrics CMOS **-Ch1 Sec 1.3, Ch2 Sec 2.2**

Lecture 2: Design Flow AND Cad Tools

Lecture 3,4:

- **Transistor Theory**
- Semiconductor material: PN-junction, NMOS, PMOS **-Ch3**

Lecture 5:

- **DC & Transient Response**
- Device modeling parameterization from I-V curves. **Ch5.2 and ch5.3**

Lecture 6: Logical Effort

Lecture 7: Power

Lecture 8: Simulation and Timing **Ch7.2-7.5**

SPICE models and parameters

Lecture 9: Combinational Circuit Design

- The CMOS inverter- **Ch3, Ch5**
- The layout of an Inverter and basic gates **ch2.3-ch7**
- Combinational /static logic structures **Ch6.1-2**

Lecture 10: Circuit /Logic Families

Lecture 11: Sequential Circuit Design

- Sequential logic gates; Latches and Flip-Flops **ch7.4- Ch10.3**

Lecture 12: Clock/Wires/Interconnect Wire modeling - Ch4

Lecture 13: Introduction to: Packaging, Power, & Clock

Lecture 14: Introduction to: Design for Testability

Lecture 15: Datapaths , Adders , SRAM

Lecture 16: ROMs, CAMs, & PLAs

Lecture 17: Scaling , Pitfalls & Reliability

Lecture 22: I/O

References

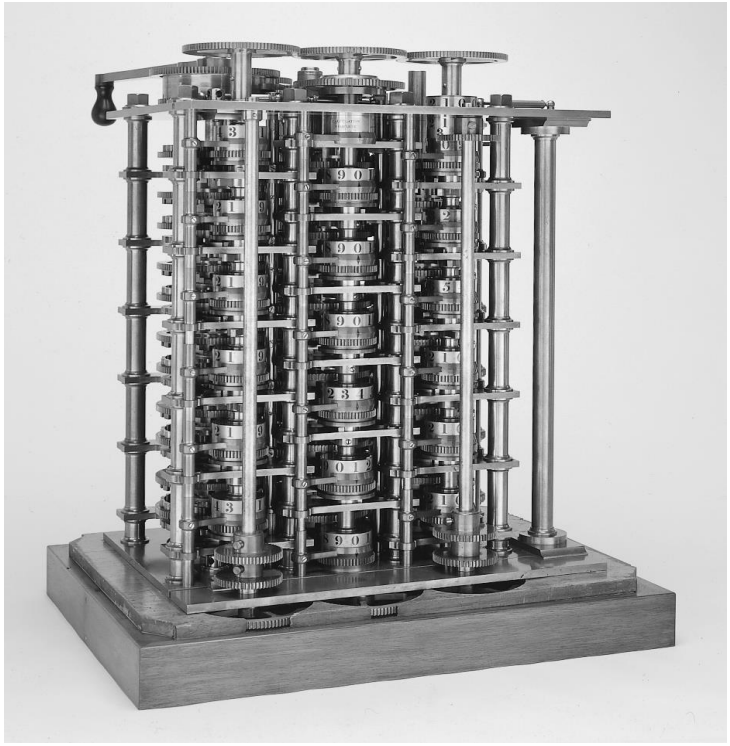
- **Some Good video to watch :**
  - **What is Integrated circuit :**
    - **https://www.youtube.com/watch?v=UWPxa6N7VvA**
  - **Evolution of the Microchip)**
    - **https://www.youtube.com/watch?v=XA8TLOF010w**
  - **Google's Chip Designing AI**
    - https://www.youtube.com/watch?v=zR9IusOpEzk
  - **How are chips made?**
    - https://www.youtube.com/watch?v=g8Qav3vIv9s
  - **Watch Nvidia Reveal H100 AI Chip**
    - **How does AI apply to chip design Nvidia did it in this way？**
      - https://www.youtube.com/watch?v=BD25ZW1HaQw
    - https://www.youtube.com/watch?v=n_oXA7Xe3ZM
  - **BZU student Vedio:**
    https://www.youtube.com/watch?v=YKL_KD6nE6A&feature=youtu.be&fbclid=IwAR3ONoaCT5ULm_xQ145kgZ6m4qYS1ebOR5tCxTwhULjMshNxs_s4HM260dM

The First Computer

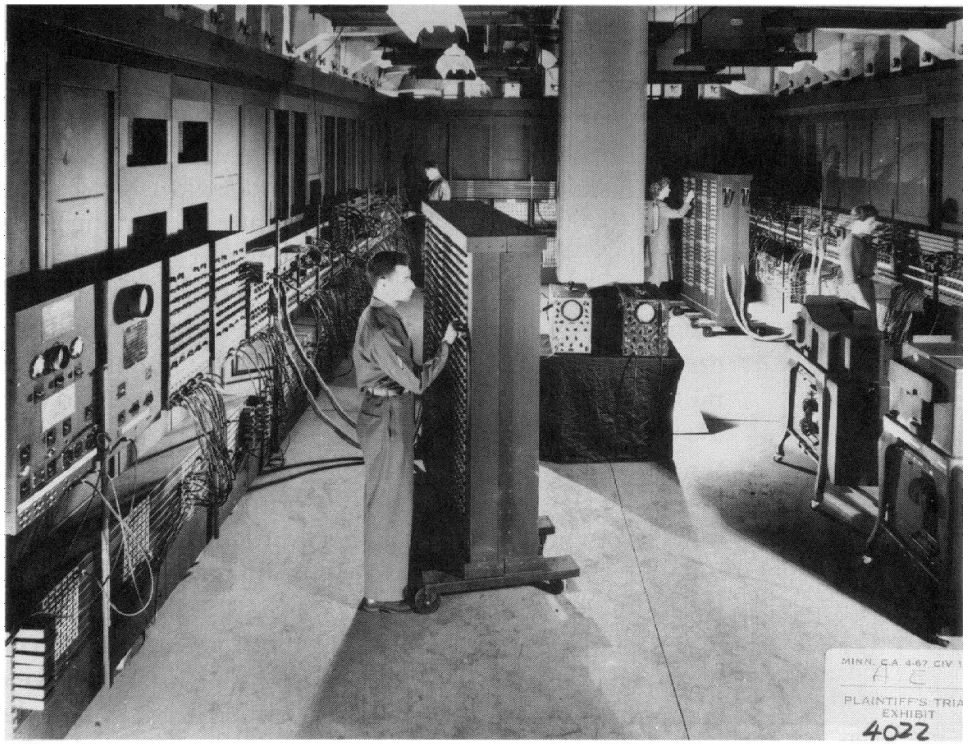
The Babbage Difference Engine (1832)

25,000 parts

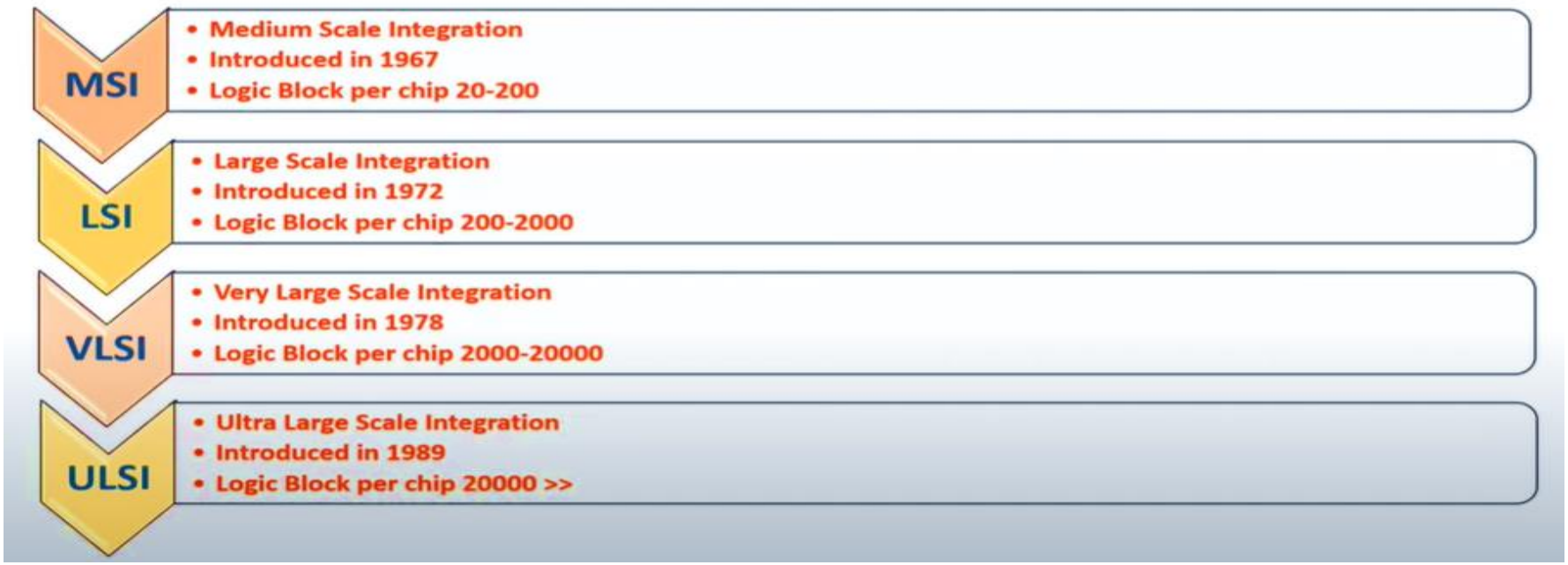
cost: £17,470



ENIAC - The first electronic computer (1946)



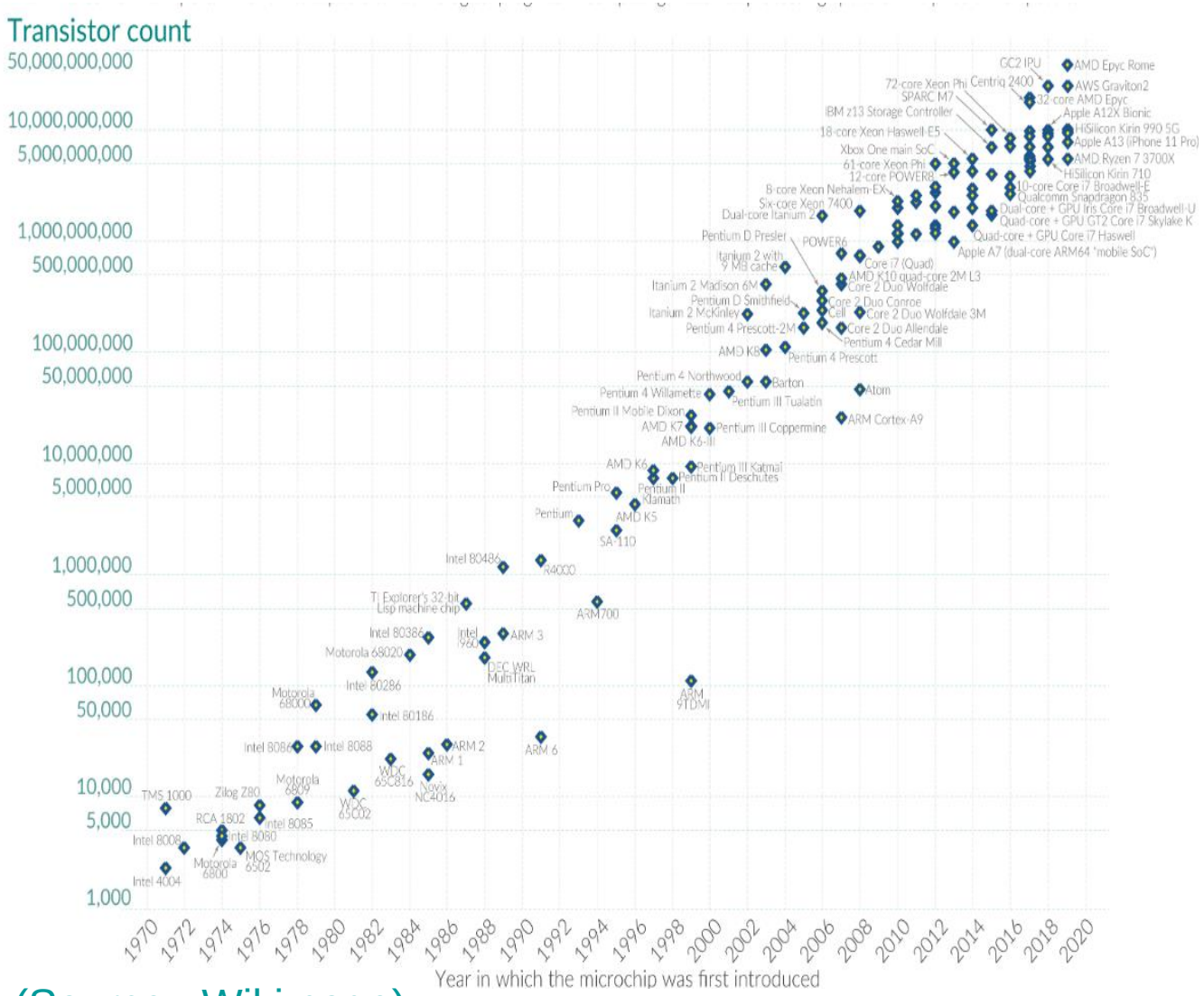
History - Evolution in Complexity



Year	Component	Name	Number of MOSFETs (in billions)
2022	microprocessor (commercial)	M1 Ultra	114 (dual-die SoC; entire M1 Ultra is a multi-chip module)
2022	GPU	Nvidia H100	80
2020	DLP	Colossus Mk2 GC200	59.4
2020	any IC chip	Wafer Scale Engine 2	2600 (wafer-scale design consisting of 84 exposed fields (dies))
2022	Flash memory	Micron's V-NAND chip	5333 (stacked package of 16 232-layer 3D NAND dies)

Source : https://en.wikipedia.org/wiki/Transistor_count

Evolution in Transistor Count



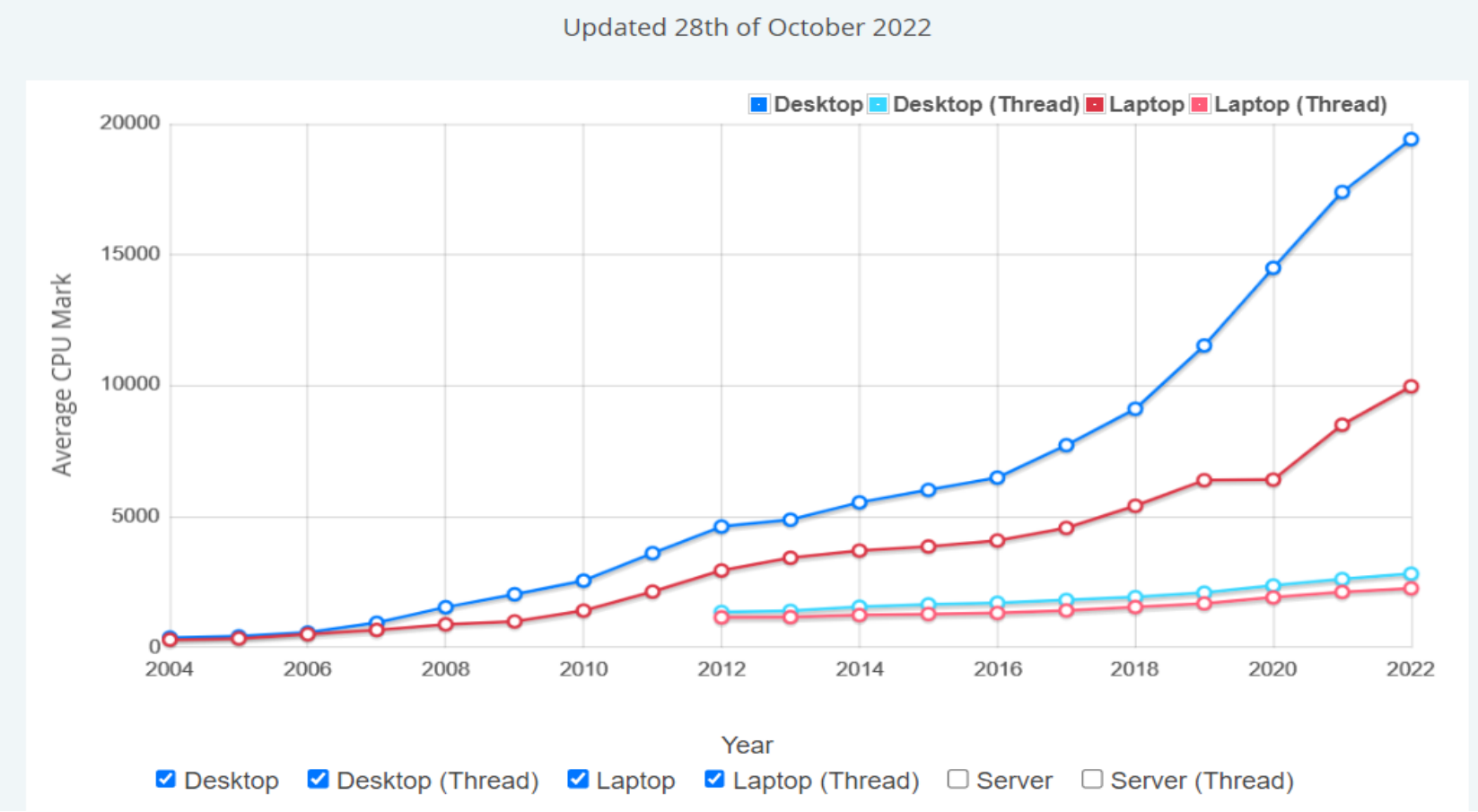
- [Process :10 µm](#) – 1971
- [6 µm](#) – 1974
- [3 µm](#) – 1977
- [1.5 µm](#) – 1981
- [1 µm](#) – 1984
- [800 nm](#) – 1987
- [600 nm](#) – 1990
- [350 nm](#) – 1993
- [250 nm](#) – 1996
- [180 nm](#) – 1999
- [130 nm](#) – 2001
- [90 nm](#) – 2003
- [65 nm](#) – 2005
- [45 nm](#) – 2007
- [32 nm](#) – 2009
- [22 nm](#) – 2012
- [14 nm](#) – 2014
- [10 nm](#) – 2016
- [7 nm](#) – 2018
- [5 nm](#) – 2020
- [3 nm](#) – 2022

- Future[2 nm](#) ~ 2024

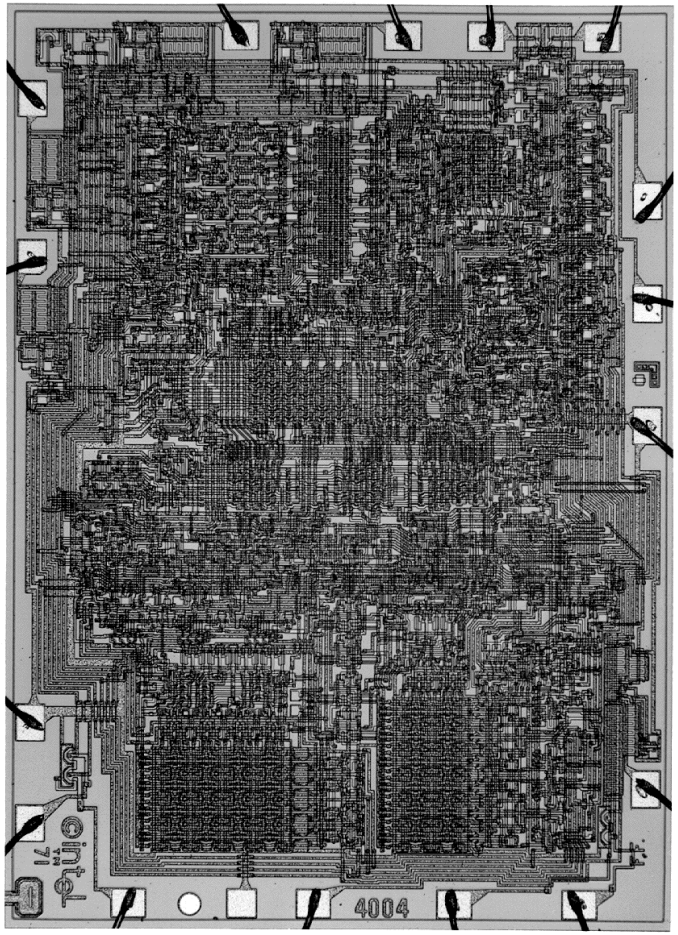
- [(Source : Wiki page)](#)

Evolution in Speed/Performance

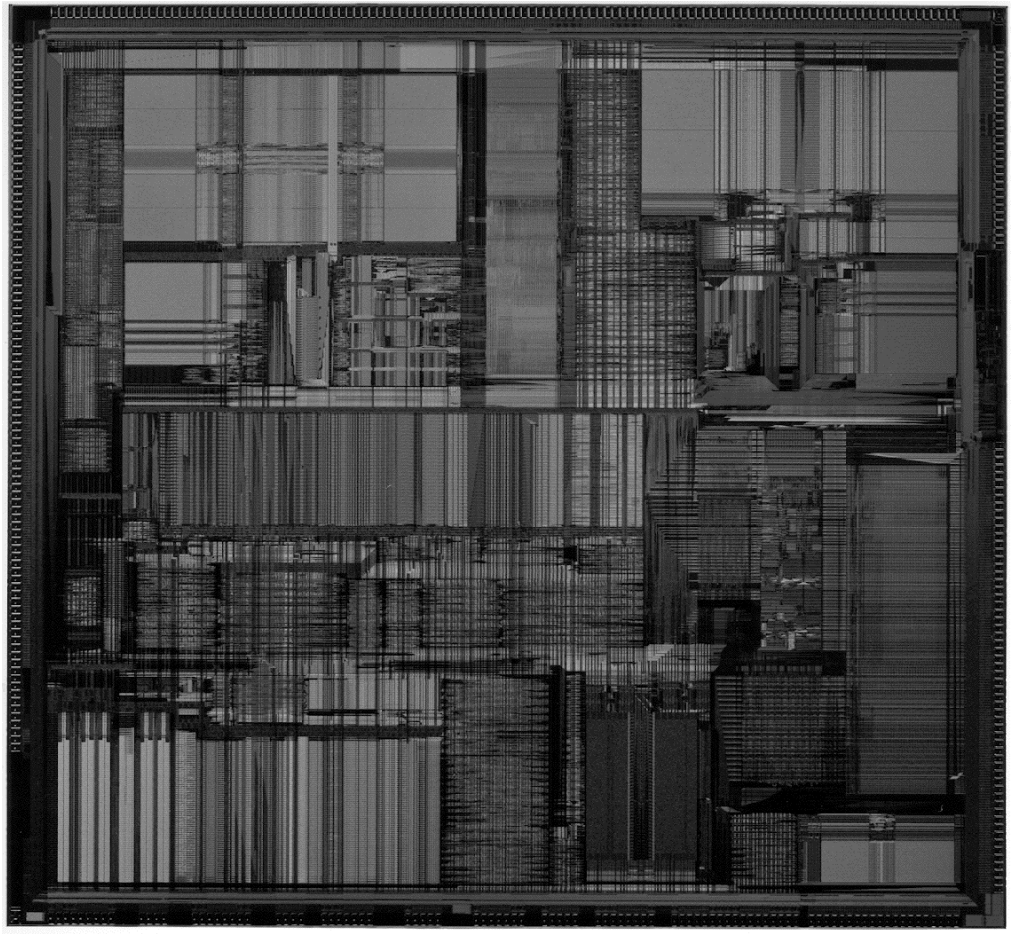
Year on Year Performance Of Intel CPU Benchmark:
https://www.cpubenchmark.net/year-on-year.html



Intel 4004 Micro-Processor



Intel Pentium (II) microprocessor

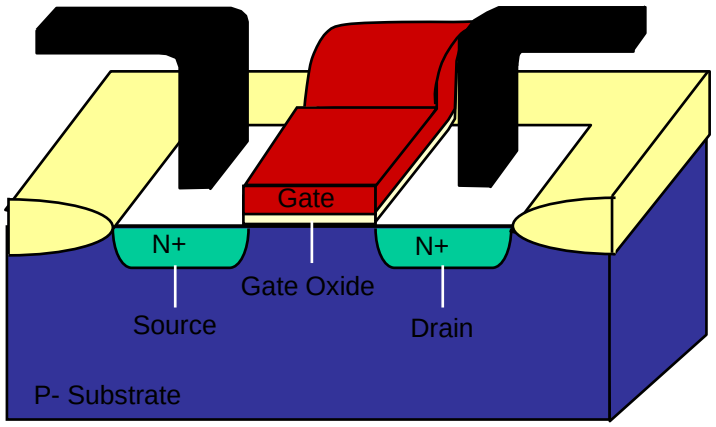


Digital Chips & Integrated Circuits)

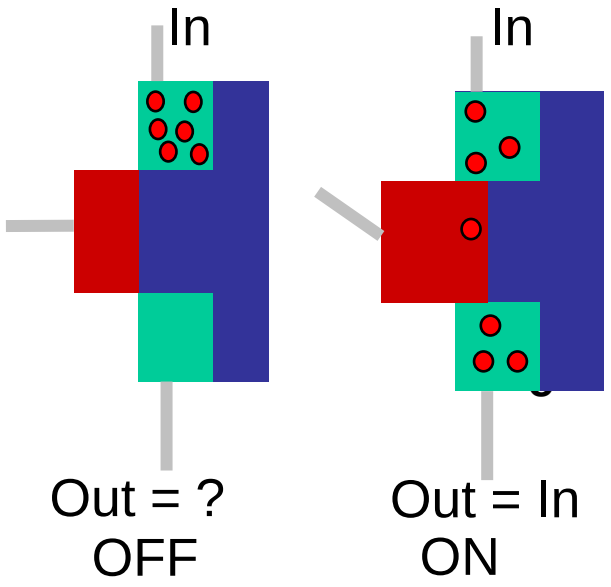
- Chips are used everywhere:
  - Computers
  - Cellular phones
  - iPADs
  - iPhones
  - Gaming systems
  - DVD players, TVs
  - Watches
  - Cars
  - Medical devices
  - Pacemakers and coffee pots
  - Space stations
  - Greeting cards
  - . . .

Basic Element

- CMOS Transistor is a switch

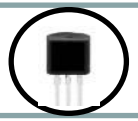
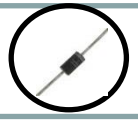
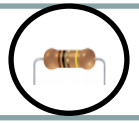


Cross section



Symbol view

Basic Elements of Electronic Circuits

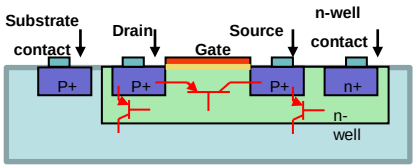
Transistor – is the switch		
Diode – is the rectifier		
Resistor - slows down electricity		
Capacitor - stores electricity		
Inductor - determines the magnitude of the electromagnetic force		
Connecting them with interconnects, an IC is obtained.		

*The elements, being prepared by discrete technology, are shown.

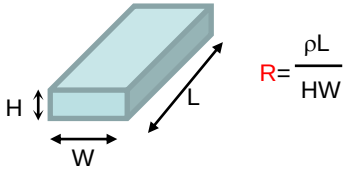
Types of IC Elements

Useful

Parasitic

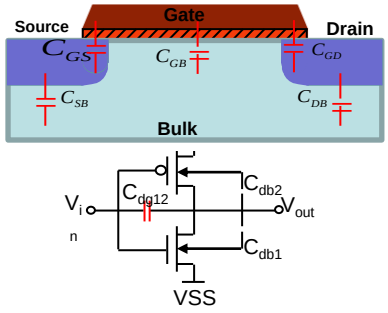


Bipolar Transistors



$$R = \frac{\rho L}{HW}$$

Resistances



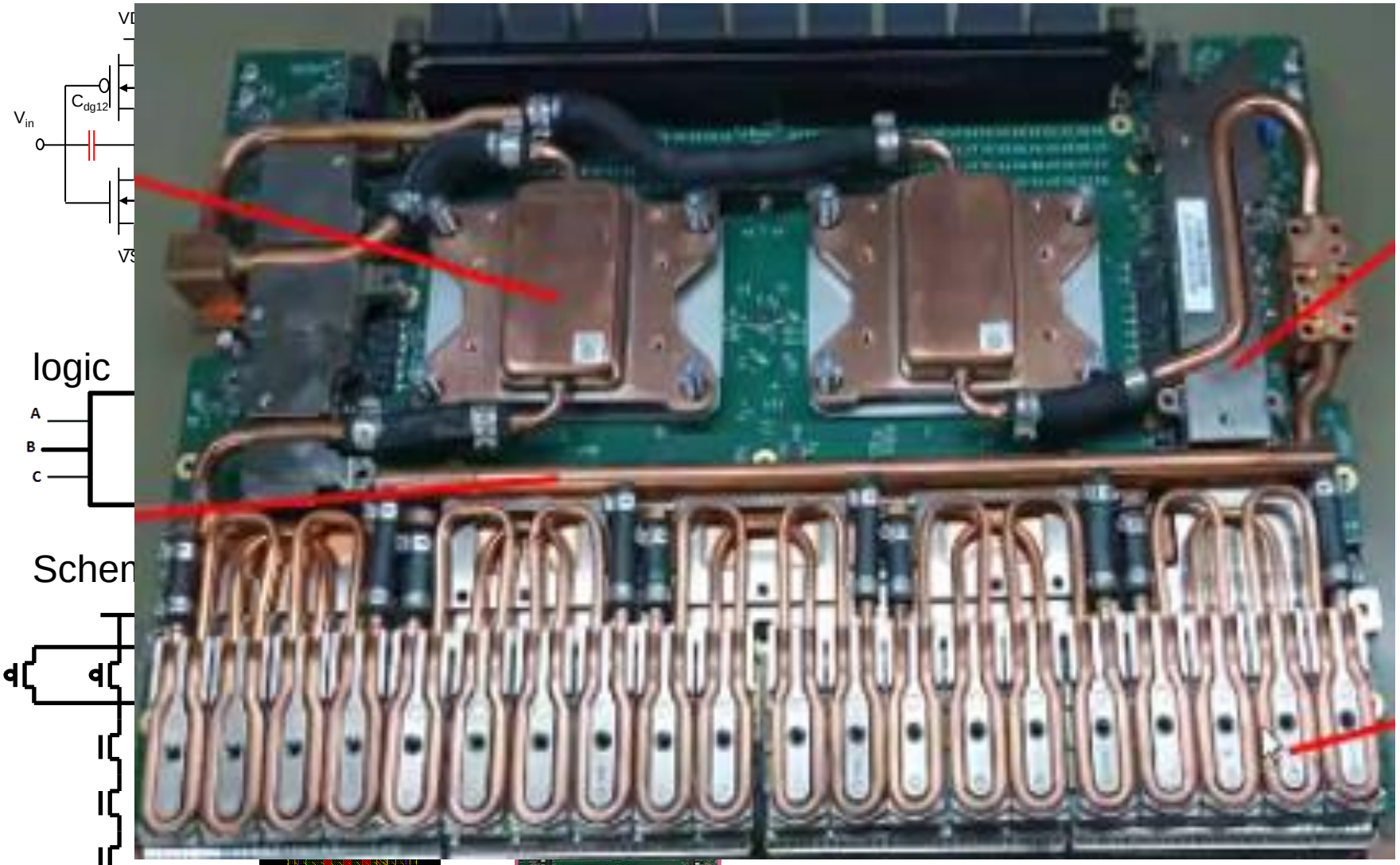
Capacitances

$$L_{ij} = \frac{\mu}{4\pi} \cdot \frac{1}{a_i a_j} \cdot \frac{1}{l_i l_j} \oint_{loop_i} \int_{a_i} \oint_{loop_j} \int_{a_j} \frac{1}{r_{ij}} dl_i dl_j da_i da_j$$

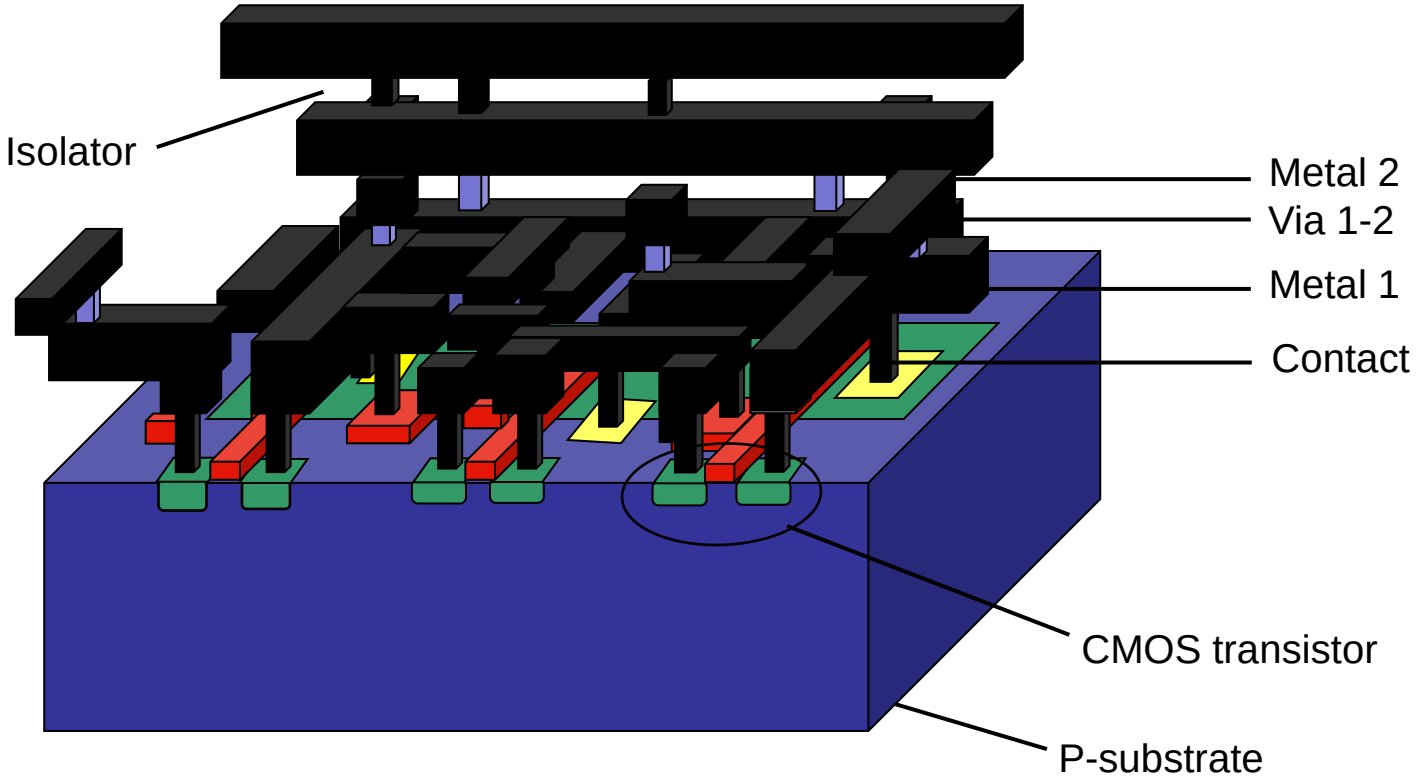
Inductances

Elements in IC

sec1

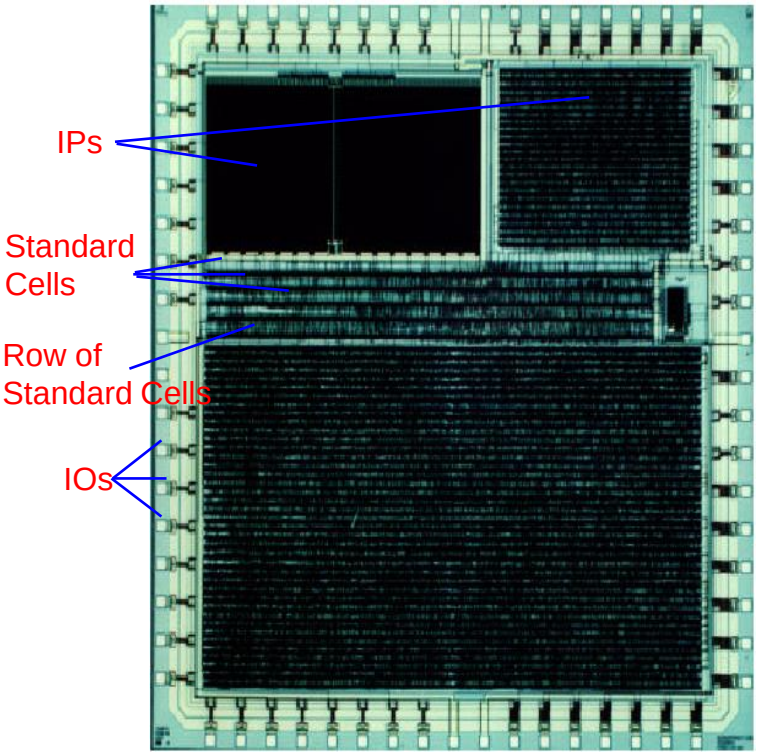


IC as a Multi Layer Structure



IC Component Types

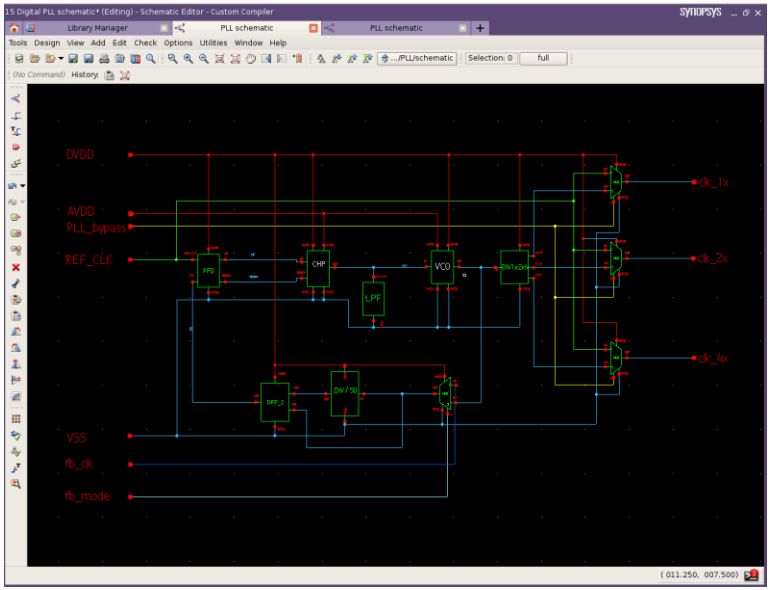
- Digital Standard Cells
  - Basic cells performing simplest functions (e.g. AND, OR, etc.) or more complex functions (Multiplexers, Latches, Flip-Flops, etc.) used as building blocks for large digital circuits
- Intellectual Property (IP) Blocks
  - Large blocks performing completed functions (DAC, ADC, PLL, etc), used in large designs
- Input/Output (I/O) Cells
  - Implement the connection between IC inner circuitry and external environment (PCB)
- Digital ICs
  - Large ICs (e.g. processor, GPU, etc.), distributed to end-users



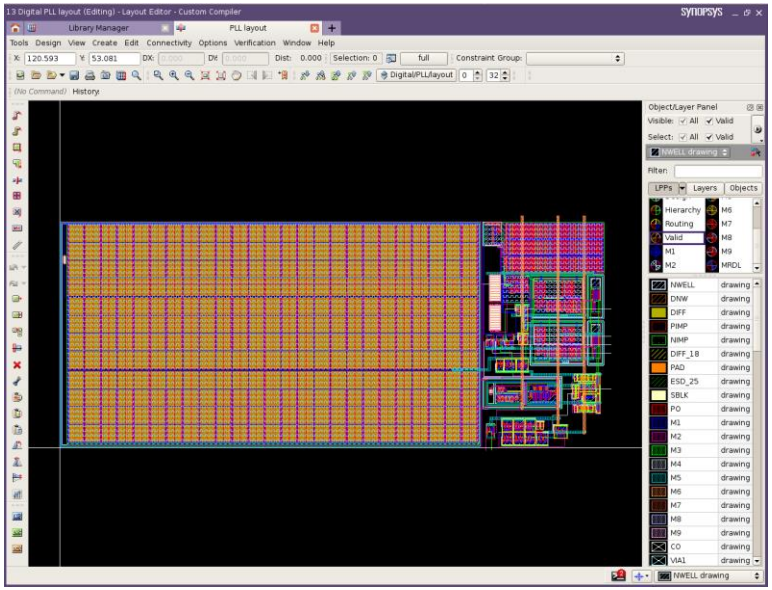
IP Example

2

PLL



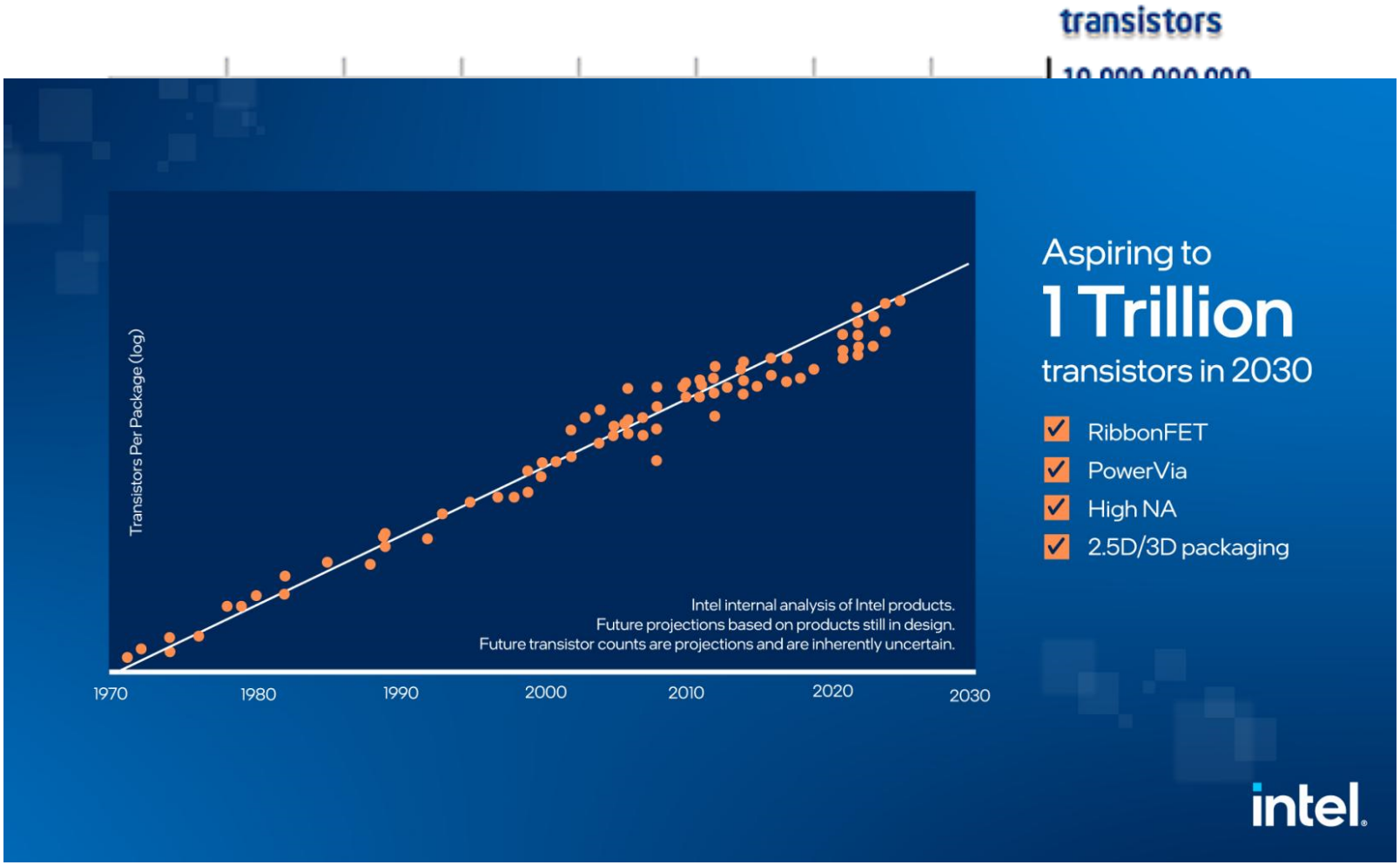
Circuit



Layout

Technology Scaling: Moore's Law

https://www.intel.com/content/www/us/en/silicon-innovations/moores-law-technology.html



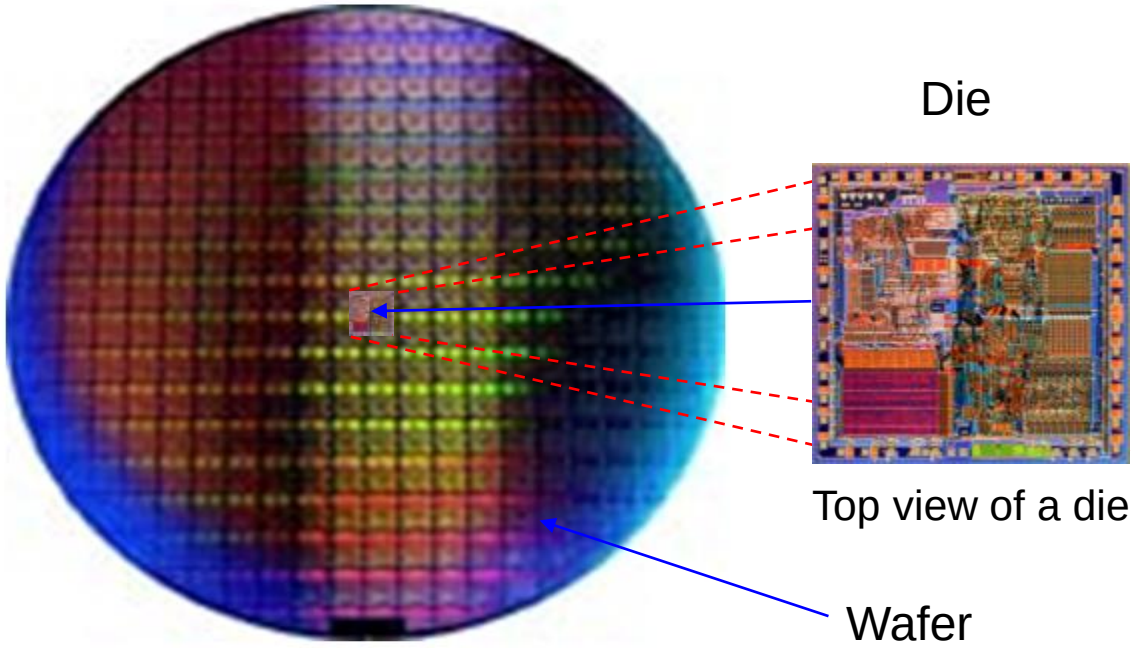
Courtesy Intel

Wafer and Die

- CMOS ICs are fabricated on circular slices of silicon called wafers.
  - Wafer contains various identical dies.

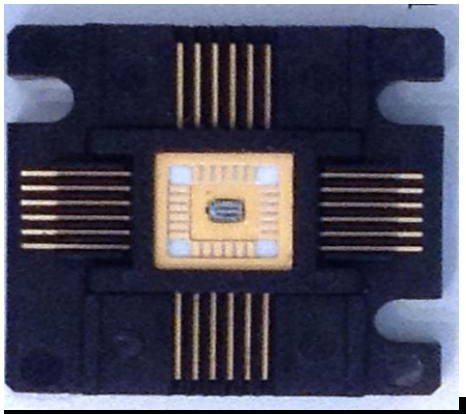
https://www.youtube.com/watch?v=aWVywhzuHnQ

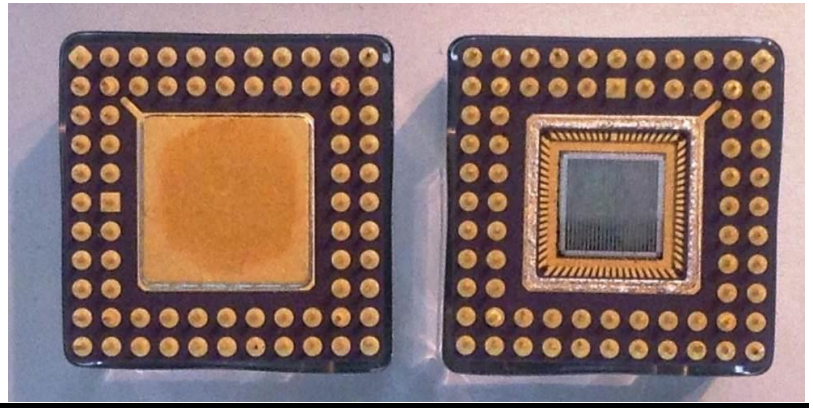
Side view of a Wafer

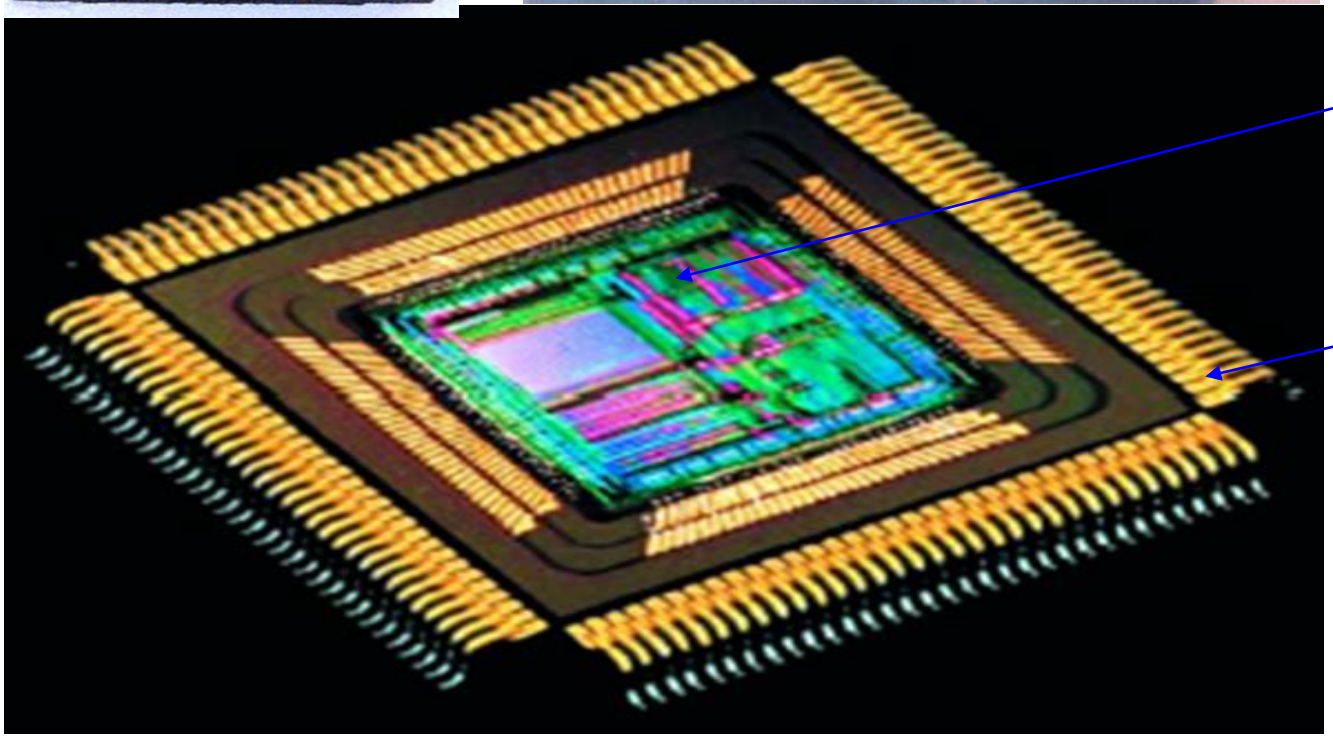


Die and Package

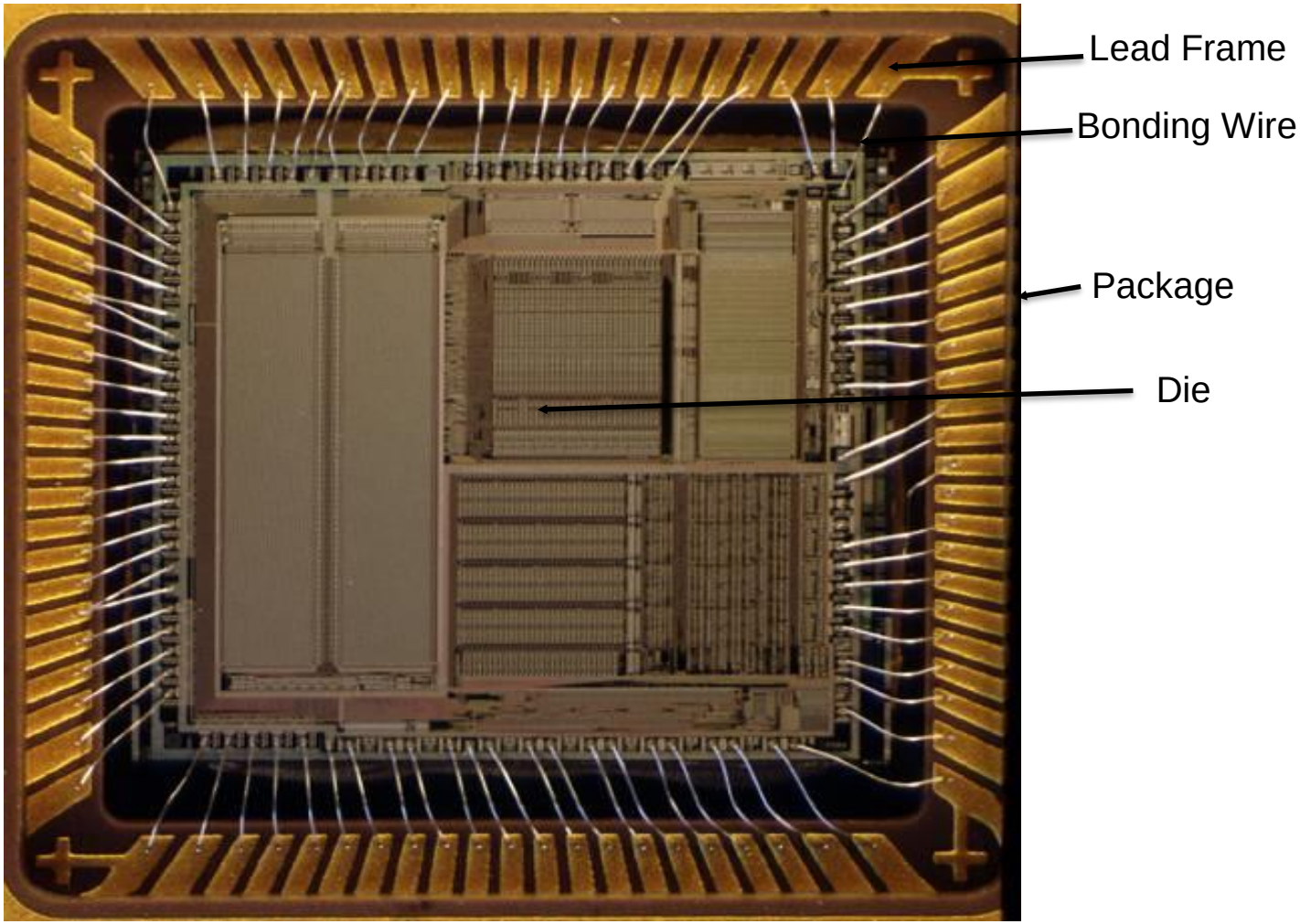
Chip Package







Packaging of Real IC



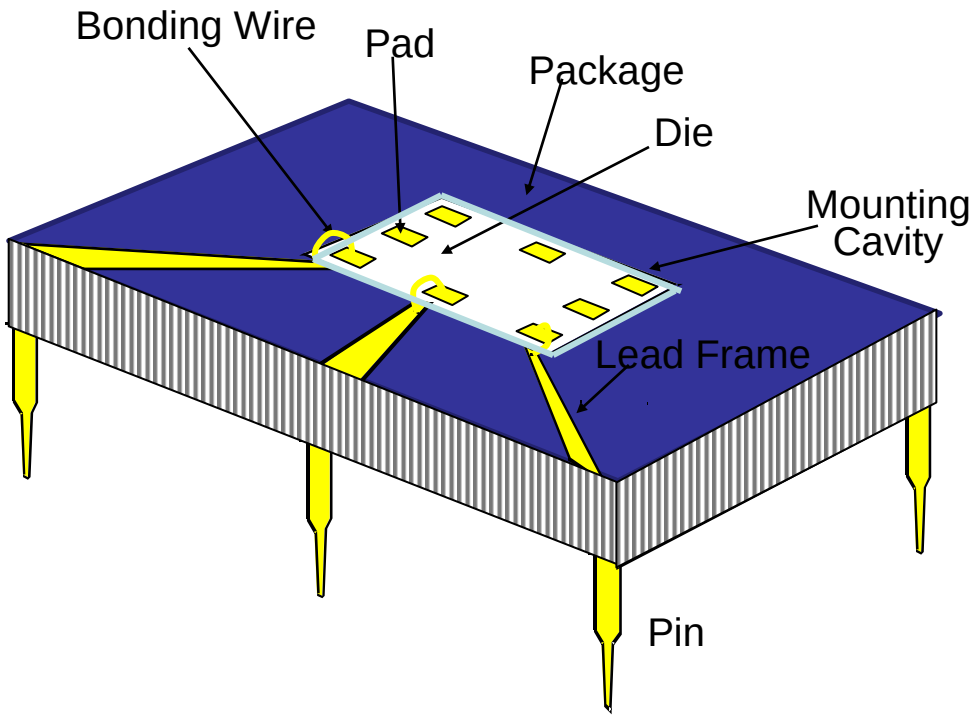
https://www.tipranks.com/news/intel-presents-new-transistor-technology-to-boost-chip-performance-by-20/?ref=blog

US chipmaker Intel Corp. last week revealed a new technology for making transistors which is said to improve the performance of its next round of processors by as much as 20%.

Intel (**INTC**) disclosed the so-called SuperFin technology for its existing 10-nanometer (nm) chip process node, describing it as its largest single, intra-node enhancement in the company's history, which promises to deliver performance improvement comparable to a full-node transition. The 10nm SuperFin technology combines Intel's FinFET transistors with Super metal insulator metal capacitor, the company said.

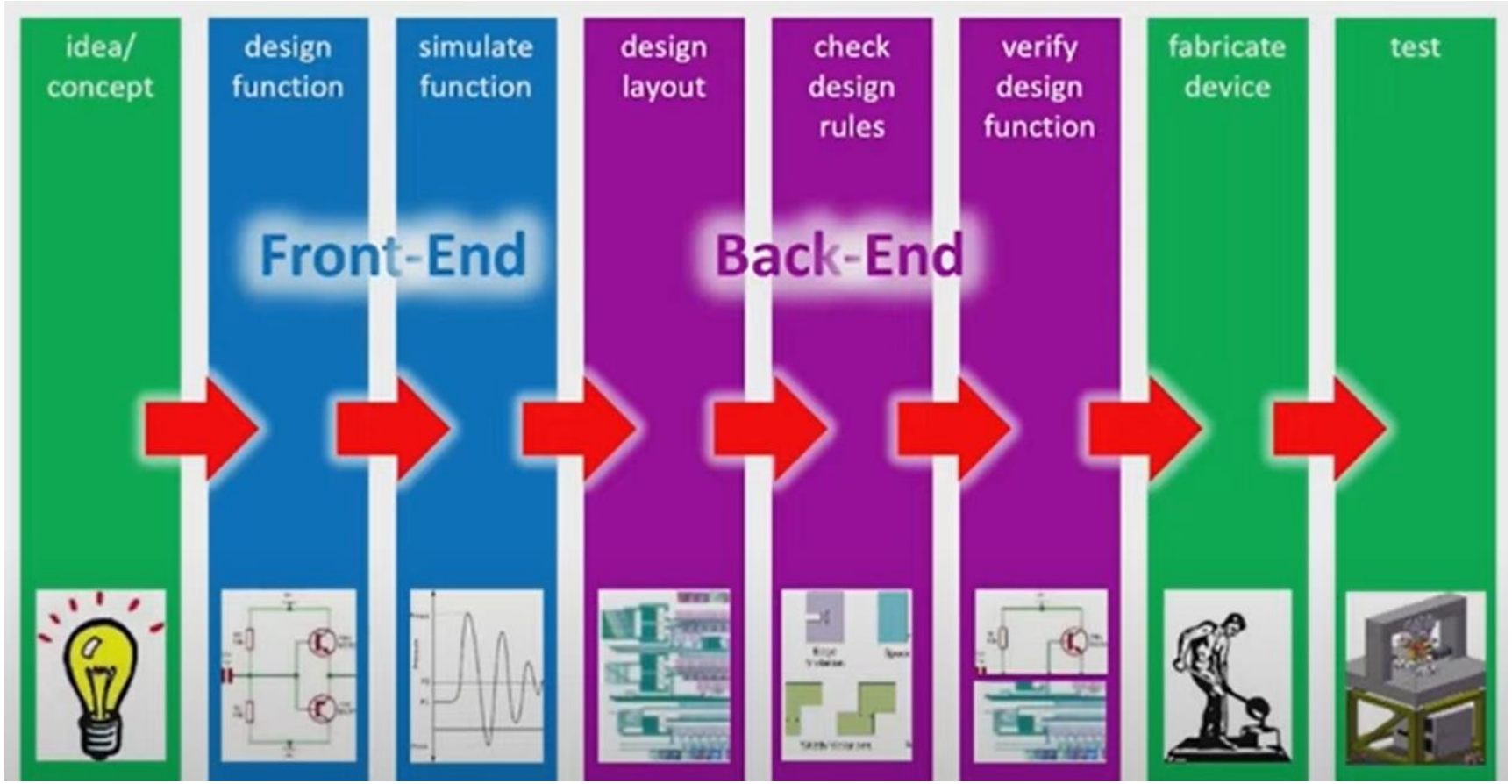
Chip Packaging

- Bonding wires connect the package to the chip.
- Pads are arranged in a frame around the chip.



Chip, PCB

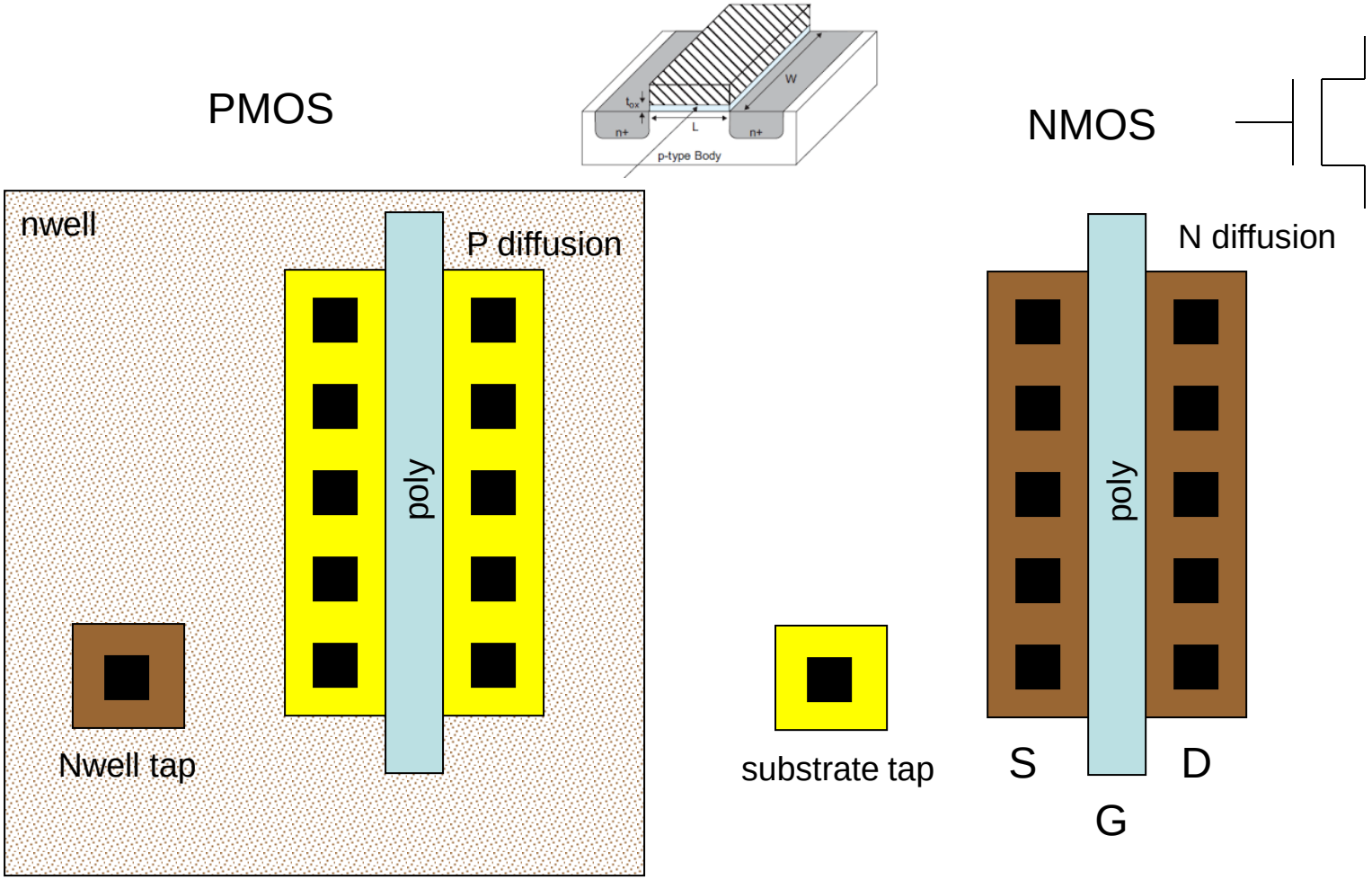
Design Flow



Source :**Photonic Integrated Circuit Design - PhotonHUB Europe Online Course 2022**
https://www.youtube.com/watch?v=Zcle3hNmblg

Layout

- Transistor defined as poly over diffusion



Suggested Reading

- What is a Circuit
- Polarity
- Semiconductor
- Resistors
- Diodes
- Capacitors
- Transistors